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S12SCIV4/D

# SCI
# Block Guide
# V04.00

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# Section 1 Introduction

## 1.1 Overview

The SCI allows asynchronous serial communications with peripheral devices and other CPUs.

## 1.2 Features

The SCI includes these distinctive features:

- Full-duplex or single-wire operation
- Standard mark/space non-return-to-zero (NRZ) format
- Selectable IrDA 1.4 return-to-zero-inverted (RZI) format with programmable pulse widths
- 13-bit baud rate selection
- Programmable 8-bit or 9-bit data format
- Separately enabled transmitter and receiver
- Programmable polarity for transmitter and receiver
- Programmable transmitter output parity
- Two receiver wakeup methods:
  - Idle line wakeup
  - Address mark wakeup
- Interrupt-driven operation with eight flags:
  - Transmitter empty
  - Transmission complete
  - Receiver full
  - Idle receiver input
  - Receiver overrun
  - Noise error
  - Framing error
  - Parity error
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection

## 1.3 Modes of Operation

The SCI functions the same in normal, special, and emulation modes. It has two low power modes, wait and stop modes.

- Run Mode
- Wait Mode
- Stop Mode





## 1.4 Block Diagram

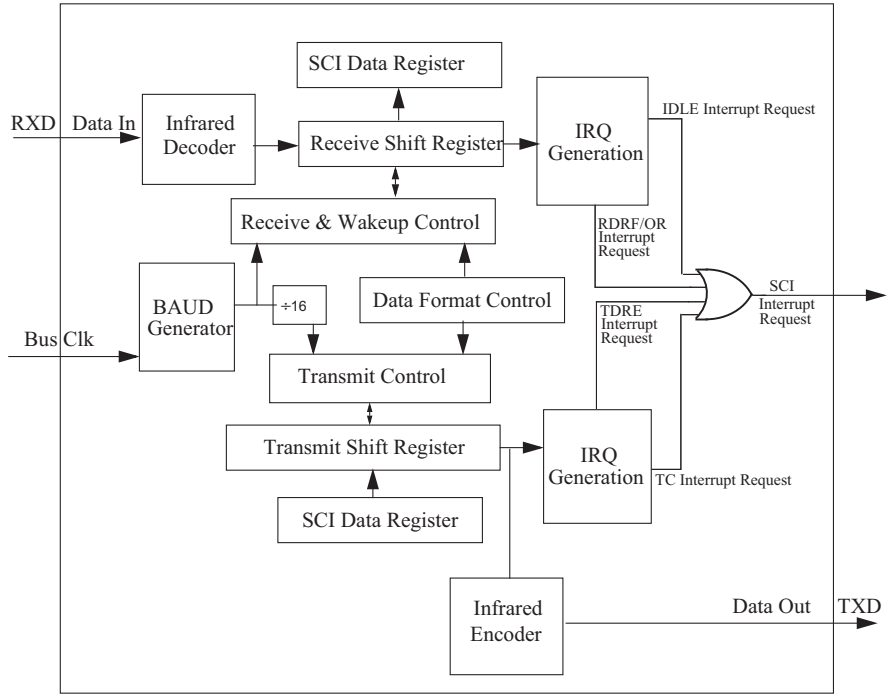


**Figure 1-1 SCI Block Diagram**

# Section 3 Memory Map and Registers

## 3.1 Overview

This section provides a detailed description of all the SCI registers.

## 3.2 Module Memory Map

The memory map for the SCI module is given below in **Table 3-1**. The Address listed for each register is the address offset. The total address for each register is the sum of the base address for the SCI module and the address offset for each register.

**Table 3-1 Module Memory Map**

| Offset | Name | Access |
|---|---|---|
| $_0 | SCI Baud Rate Register High (SCIBDH) | Read/Write |
| $_1 | SCI Baud Rate Register Low (SCIBDL) | Read/Write |
| $_2 | SCI Control Register1 (SCICR1) | Read/Write |
| $_3 | SCI Control Register 2 (SCICR2) | Read/Write |
| $_4 | SCI Status Register 1 (SCISR1) | Read |
| $_5 | SCI Status Register 2(SCISR2) | Read/Write |
| $_6 | SCI Data Register High (SCIDRH) | Read/Write |
| $_7 | SCI Data Register Low (SCIDRL) | Read/Write |





**Register Quick Reference**

| Register name | | Bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | Bit 0 | Addr. offset |
|---|---|---|---|---|---|---|---|---|---|---|
| SCIBDH | Read: | IREN | TNP1 | TNP0 | SBR12 | SBR11 | SBR10 | SBR9 | SBR8 | $_0 |
| | Write: | | | | | | | | | |
| SCIBDL | Read: | SBR7 | SBR6 | SBR5 | SBR4 | SBR3 | SBR2 | SBR1 | SBR0 | $_1 |
| | Write: | | | | | | | | | |
| SCICR1 | Read: | LOOPS | SCISWAI | RSRC | M | WAKE | ILT | PE | PT | $_2 |
| | Write: | | | | | | | | | |
| SCICR2 | Read: | TIE | TCIE | RIE | ILIE | TE | RE | RWU | SBK | $_3 |
| | Write: | | | | | | | | | |
| SCISR1 | Read: | TDRE | TC | RDRF | IDLE | OR | NF | FE | PF | $_4 |
| | Write: | | | | | | | | | |
| SCISR2 | Read: | 0 | 0 | 0 | TXPOL | RXPOL | BRK13 | TXDIR | RAF | $_5 |
| | Write: | | | | | | | | | |
| SCIDRH | Read: | R8 | T8 | 0 | 0 | 0 | 0 | 0 | 0 | $_6 |
| | Write: | | | | | | | | | |
| SCIDRL | Read: | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 | $_7 |
| | Write: | T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 | |

= Reserved or unimplemented

**Figure 3-1 SCI Register Quick Reference**

## 3.3 Register Descriptions

This section consists of register descriptions in address order. Each description includes a standard register diagram with an associated figure number. Writes to a reserved register locations do not have any effect and reads of these locations return a zero. Details of register bit and field function follow the register diagrams, in bit order.

### 3.3.1 SCI Baud Rate Registers (SCIBDH, SCIBDL)

**Register address: $_0**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Read<br>Write | IREN | TNP1 | TNP0 | SBR12 | SBR11 | SBR10 | SBR9 | SBR8 |
| RESET: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Register address: $_1**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Read<br>Write | SBR7 | SBR6 | SBR5 | SBR4 | SBR3 | SBR2 | SBR1 | SBR0 |
| RESET: | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

= Unimplemented or Reserved

**Figure 3-2 SCI Baud Rate Registers (SCI BDH/L)**

Read: anytime. If only SCIBDH is written to, a read will not return the correct data until SCIBDL is written to as well, following a write to SCIBDH.

Write: anytime

The SCI Baud Rate Register is used by to determine the baud rate of the SCI, and to control the infrared modulation/demodulation submodule.

IREN — Infrared Enable Bit

This bit enables/disables the infrared modulation/demodulation submodule.
1 = IR enabled
0 = IR disabled

TNP1,TNP0 - Transmitter Narrow Pulse Bits

These bits enable whether the SCI transmits a 1/16, 3/16, 1/32 or 1/4 narrow pulse.

**Table 3-2 IRSCI Transmit Pulse Width**

| TNP[1:0] | Narrow Pulse Width |
|---|---|
| 11 | 1/4 |
| 10 | 1/32 |
| 01 | 1/16 |
| 00 | 3/16 |

SBR[12:0] - SCI Baud Rate Bits

The baud rate for the SCI is determined by the bits in this register. The baud rate is calculated two different ways depending on the state of the IREN bit.

The formulas for calculating the baud rate are:

When IREN=0 then,

SCI baud rate = SCI module clock / (16 x SBR[12:0])

When IREN=1 then,

SCI baud rate = SCI module clock / (32 x SBR[12:1])





***NOTE:*** *The baud rate generator is disabled after reset and not started until the TE bit or the RE bit is set for the first time.. The baud rate generator is disabled when (SBR[12:0] = 0 and IREN = 0) or (SBR[12:1] = 0 and IREN = 1).*

***NOTE:*** *Writing to SCIBDH has no effect without writing to SCIBDL, since writing to SCIBDH puts the data in a temporary location until SCIBDL is written to.*

## 3.3.2 SCI Control Register 1 (SCICR1)

**Register address: $_2**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Read<br>Write | LOOPS | SCISWAI | RSRC | M | WAKE | ILT | PE | PT |
| RESET: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 3-3 SCI Control Register 1 (SCICR1)**

Read: anytime

Write: anytime

LOOPS - Loop Select Bit

LOOPS enables loop operation. In loop operation, the RXD pin is disconnected from the SCI and the transmitter output is internally connected to the receiver input. Both the transmitter and the receiver must be enabled to use the loop function.
1 = Loop operation enabled
0 = Normal operation enabled

The receiver input is determined by the RSRC bit.

SCISWAI — SCI Stop in Wait Mode Bit

SCISWAI disables the SCI in wait mode.
1 = SCI disabled in wait mode
0 = SCI enabled in wait mode

RSRC — Receiver Source Bit

When LOOPS = 1, the RSRC bit determines the source for the receiver shift register input.
1 = Receiver input connected externally to transmitter
0 = Receiver input internally connected to transmitter output

**Table 3-3 Loop Functions**

| LOOPS | RSRC | Function |
|---|---|---|
| 0 | x | Normal operation |
| 1 | 0 | Loop mode with transmitter output internally connected to receiver input |
| 1 | 1 | Single-wire mode with TXD pin connected to receiver input |

M — Data Format Mode Bit

MODE determines whether data characters are eight or nine bits long.
1 = One start bit, nine data bits, one stop bit
0 = One start bit, eight data bits, one stop bit

WAKE — Wakeup Condition Bit

WAKE determines which condition wakes up the SCI: a logic 1 (address mark) in the most significant bit position of a received data character or an idle condition on the RXD pin.
1 = Address mark wakeup
0 = Idle line wakeup

ILT — Idle Line Type Bit

ILT determines when the receiver starts counting logic 1s as idle character bits. The counting begins either after the start bit or after the stop bit. If the count begins after the start bit, then a string of logic 1s preceding the stop bit may cause false recognition of an idle character. Beginning the count after the stop bit avoids false idle character recognition, but requires properly synchronized transmissions.
1 = Idle character bit count begins after stop bit
0 = Idle character bit count begins after start bit

PE — Parity Enable Bit

PE enables the parity function. When enabled, the parity function inserts a parity bit in the most significant bit position.
1 = Parity function enabled
0 = Parity function disabled

PT — Parity Type Bit

PT determines whether the SCI generates and checks for even parity or odd parity. With even parity, an even number of 1s clears the parity bit and an odd number of 1s sets the parity bit. With odd parity, an odd number of 1s clears the parity bit and an even number of 1s sets the parity bit.
1 = Odd parity
0 = Even parity





## 3.3.3 SCI Control Register 2 (SCICR2)

**Register address: $_3**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Read<br>Write | TIE | TCIE | RIE | ILIE | TE | RE | RWU | SBK |
| RESET: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 3-4 SCI Control Register 2 (SCICR2)**

Read: anytime

Write: anytime

TIE — Transmitter Interrupt Enable Bit

TIE enables the transmit data register empty flag, TDRE, to generate interrupt requests.
1 = TDRE interrupt requests enabled
0 = TDRE interrupt requests disabled

TCIE — Transmission Complete Interrupt Enable Bit

TCIE enables the transmission complete flag, TC, to generate interrupt requests.
1 = TC interrupt requests enabled
0 = TC interrupt requests disabled

RIE — Receiver Full Interrupt Enable Bit

RIE enables the receive data register full flag, RDRF, or the overrun flag, OR, to generate interrupt requests.
1 = RDRF and OR interrupt requests enabled
0 = RDRF and OR interrupt requests disabled

ILIE — Idle Line Interrupt Enable Bit

ILIE enables the idle line flag, IDLE, to generate interrupt requests.
1 = IDLE interrupt requests enabled
0 = IDLE interrupt requests disabled

TE — Transmitter Enable Bit

TE enables the SCI transmitter and configures the TXD pin as being controlled by the SCI.. The TE bit can be used to queue an idle preamble.
1 = Transmitter enabled
0 = Transmitter disabled

RE — Receiver Enable Bit

RE enables the SCI receiver.
1 = Receiver enabled

0 = Receiver disabled

RWU — Receiver Wakeup Bit

Standby state

1 = RWU enables the wakeup function and inhibits further receiver interrupt requests. Normally, hardware wakes the receiver by automatically clearing RWU.

0 = Normal operation.

SBK — Send Break Bit

Toggling SBK sends one break character (10 or 11 logic 0s, respectively 13 or 14 logics 0s if BRK13 is set). Toggling implies clearing the SBK bit before the break character has finished transmitting. As long as SBK is set, the transmitter continues to send complete break characters (10 or 11 bits, respectively 13 or 14 bits).

1 = Transmit break characters

0 = No break characters

### 3.3.4 SCI Status Register 1 (SCISR1)

The SCISR1 and SCISR2 registers provides inputs to the MCU for generation of SCI interrupts. Also, these registers can be polled by the MCU to check the status of these bits. The flag-clearing procedures require that the status register be read followed by a read or write to the SCI Data Register.It is permissible to execute other instructions between the two steps as long as it does not compromise the handling of I/O, but the order of operations is important for flag clearing.

**Register address: $_4**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Read | TDRE | TC | RDRF | IDLE | OR | NF | FE | PF |
| Write | | | | | | | | |
| RESET: | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 3-5 SCI Status Register 1 (SCISR1)**

Read: anytime

Write: has no meaning or effect

TDRE — Transmit Data Register Empty Flag

TDRE is set when the transmit shift register receives a byte from the SCI data register. When TDRE is 1, the transmit data register (SCIDRH/L) is empty and can receive a new value to transmit.Clear TDRE by reading SCI status register 1 (SCISR1), with TDRE set and then writing to SCI data register low (SCIDRL).

1 = Byte transferred to transmit shift register; transmit data register empty

0 = No byte transferred to transmit shift register

TC — Transmit Complete Flag





TC is set low when there is a transmission in progress or when a preamble or break character is loaded. TC is set high when the TDRE flag is set and no data, preamble, or break character is being transmitted.When TC is set, the TXD pin becomes idle (logic 1). Clear TC by reading SCI status register 1 (SCISR1) with TC set and then writing to SCI data register low (SCIDRL). TC is cleared automatically when data, preamble, or break is queued and ready to be sent. TC is cleared in the event of a simultaneous set and clear of the TC flag (transmission not complete).

1 = No transmission in progress

0 = Transmission in progress

RDRF — Receive Data Register Full Flag

RDRF is set when the data in the receive shift register transfers to the SCI data register. Clear RDRF by reading SCI status register 1 (SCISR1) with RDRF set and then reading SCI data register low (SCIDRL).

1 = Received data available in SCI data register

0 = Data not available in SCI data register

IDLE — Idle Line Flag

IDLE is set when 10 consecutive logic 1s (if M=0) or 11 consecutive logic 1s (if M=1) appear on the receiver input.. Once the IDLE flag is cleared, a valid frame must again set the RDRF flag before an idle condition can set the IDLE flag.Clear IDLE by reading SCI status register 1 (SCISR1) with IDLE set and then reading SCI data register low (SCIDRL).

1 = Receiver input has become idle

0 = Receiver input is either active now or has never become active since the IDLE flag was last cleared

***NOTE:*** *When the receiver wakeup bit (RWU) is set, an idle line condition does not set the IDLE flag.*

OR — Overrun Flag

OR is set when software fails to read the SCI data register before the receive shift register receives the next frame. The OR bit is set immediately after the stop bit has been completely received for the second frame. The data in the shift register is lost, but the data already in the SCI data registers is not affected. Clear OR by reading SCI status register 1 (SCISR1) with OR set and then reading SCI data register low (SCIDRL).

1 = Overrun

0 = No overrun

NF — Noise Flag

NF is set when the SCI detects noise on the receiver input. NF bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. Clear NF by reading SCI status register 1(SCISR1), and then reading SCI data register low (SCIDRL).

1 = Noise

0 = No noise

FE — Framing Error Flag

FE is set when a logic 0 is accepted as the stop bit. FE bit is set during the same cycle as the RDRF flag but does not get set in the case of an overrun. FE inhibits further data reception until it is cleared. Clear FE by reading SCI status register 1 (SCISR1) with FE set and then reading the SCI data register low (SCIDRL).

1 = Framing error
0 = No framing error

PF — Parity Error Flag

PF is set when the parity enable bit, PE, is set and the parity of the received data does not match its parity bit. Clear PF by reading SCI status register 1 (SCISR1), and then reading SCI data register low (SCIDRL).

1 = Parity error
0 = No parity error

### 3.3.5 SCI Status Register 2 (SCISR2)

**Register address: $_5**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Read | 0 | 0 | 0 | TXPOL | RXPOL | BRK13 | TXDIR | RAF |
| Write | | | | | | | | |
| RESET: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 3-6 SCI Status Register 2 (SCISR2)**

Read: anytime

Write: anytime;

TXPOL — Transmit Polarity

This bit control the polarity of the transmitted data. In NRZ format, a one is represented by a mark and a zero is represented by a space for normal polarity, and the opposite for inverted polarity. In IrDA format, a zero is represented by short high pulse in the middle of a bit time remaining idle low for a one for normal polarity, and a zero is represented by short low pulse in the middle of a bit time remaining idle high for a one for inverted polarity.

1 = Inverted polarity
0 = Normal polarity

RXPOL — Receive Polarity

This bit control the polarity of the received data. In NRZ format, a one is represented by a mark and a zero is represented by a space for normal polarity, and the opposite for inverted polarity. In IrDA format, a zero is represented by short high pulse in the middle of a bit time remaining idle low for a one for normal polarity, and a zero is represented by short low pulse in the middle of a bit time remaining idle high for a one for inverted polarity.

1 = Inverted polarity





0 = Normal polarity

BRK13 — Break Transmit character length

This bit determines whether the transmit break character is 10 or 11 bit respectively 13 or 14 bits long. The detection of a framing error is not affected by this bit.

1 = Break character is 13 or 14 bit long
0 = Break Character is 10 or 11 bit long

TXDIR — Transmitter pin data direction in Single-Wire mode.

This bit determines whether the TXD pin is going to be used as an input or output, in the Single-Wire mode of operation. This bit is only relevant in the Single-Wire mode of operation.

1 = TXD pin to be used as an output in Single-Wire mode
0 = TXD pin to be used as an input in Single-Wire mode

RAF — Receiver Active Flag

RAF is set when the receiver detects a logic 0 during the RT1 time period of the start bit search. RAF is cleared when the receiver detects an idle character.

1 = Reception in progress
0 = No reception in progress

### 3.3.6 SCI Data Registers (SCIDRH, SCIDRL)

**Register address: $_6**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Read | R8 | T8 | 0 | 0 | 0 | 0 | 0 | 0 |
| Write | | | | | | | | |
| RESET: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Register address: $_7**

| | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Read | R7 | R6 | R5 | R4 | R3 | R2 | R1 | R0 |
| Write | T7 | T6 | T5 | T4 | T3 | T2 | T1 | T0 |
| RESET: | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

= Unimplemented or Reserved

**Figure 3-7 SCI Data Registers (SCIDRH/L)**

Read: anytime; reading accesses SCI receive data register

Write: anytime; writing accesses SCI transmit data register; writing to R8 has no effect

R8 — Received Bit 8

R8 is the ninth data bit received when the SCI is configured for 9-bit data format (M = 1).

T8 — Transmit Bit 8

T8 is the ninth data bit transmitted when the SCI is configured for 9-bit data format (M = 1).

R7-R0 — Received bits seven through zero for 9-bit or 8-bit data formats

T7-T0 — Transmit bits seven through zero for 9-bit or 8-bit formats

***NOTE:*** *If the value of T8 is the same as in the previous transmission, T8 does not have to be rewritten.The same value is transmitted until T8 is rewritten*

***NOTE:*** *In 8-bit data format, only SCI data register low (SCIDRL) needs to be accessed.*

***NOTE:*** *When transmitting in 9-bit data format and using 8-bit write instructions, write first to SCI data register high (SCIDRH), then SCIDRL.*