Parameter

CPU Type: Q02(H)

Device Setting

Internal relay (M)	8192 points
Latch relay (L)	8192 points
Link relay (B)	8192 points
Annunciator (F)	2048 points
Edge relay (V)	2048 points
Timer (T)	2048 points
Retentive timer (ST)	0 points
Counter (C)	1024 points
Data register (D)	12288 points
Link register (W)	8192 points
Latch relay (L) DISABLE C/L KEY start	
Latch relay (L) DISABLE C/L KEY end	
Link relay (B) ENABLE C/L KEY start	
Link relay (B) ENABLE C/L KEY end	
Link relay (B) DISABLE C/L KEY start	
Link relay (B) DISABLE C/L KEY end	
Annunciator (F) ENABLE C/L KEY start	
Annunciator (F) ENABLE C/L KEY end	
Annunciator (F) DISABLE C/L KEY start	
Annunciator (F) DISABLE C/L KEY end	
Edge relay (V) ENABLE C/L KEY start	
Edge relay (V) ENABLE C/L KEY end	
Edge relay (V) DISABLE C/L KEY start	
Edge relay (V) DISABLE C/L KEY end	
Timer (T) ENABLE C/L KEY start	
Timer (T) ENABLE C/L KEY end	
Timer (T) DISABLE C/L KEY start	
Timer (T) DISABLE C/L KEY end	
Retentive timer (ST) ENABLE C/L KEY start	
Retentive timer (ST) ENABLE C/L KEY end	
Retentive timer (ST) DISABLE C/L KEY start	
Retentive timer (ST) DISABLE C/L KEY end	
Counter (C) ENABLE C/L KEY start	
Counter (C) ENABLE C/L KEY end	
Counter (C) DISABLE C/L KEY start	
Counter (C) DISABLE C/L KEY end	
Data register (D) ENABLE C/L KEY start	
Data register (D) ENABLE C/L KEY end	
Data register (D) DISABLE C/L KEY start	
Data register (D) DISABLE C/L KEY end	
Link register (W) ENABLE C/L KEY start	
Link register (W) ENABLE C/L KEY end	
Link register (W) DISABLE C/L KEY start	
Link register (W) DISABLE C/L KEY end	

IO Configuration

Slot	Type	Items	1st XY	Type Name	Switch					Output mode on error	Operation mode on error	I/O response time	Control Plc
					1	2	3	4	5				
PLC1		16	3E00h										
2	Intelli.	16		AD						Clear	Stop		PLC No. 1
3	Intelli.	16		DA						Clear	Stop		PLC No. 1

Base settings

Extension List	Base Name	Power Supply	Extension Cable	Points

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PLC Setup

Timer limit - low speed	100 ms
Timer limit - high speed	10.0 ms
RUN contact	
PAUSE contact	
Allow remote reset	No
Output mode at STOP to RUN	Previous state
Perform internal arithmetic operations in double precision	No
Synchronize intelligent module's pulse up	Yes
Common pointer No.	P0 After
Points occupied by empty slot	16
Interrupt counter	C0
I28 scan interval	100.0 ms
I29 scan interval	40.0 ms
I30 scan interval	20.0 ms
I31 scan interval	10.0 ms
High speed execution	No
Use special relay / special register from SM/SD1000	Yes
Watchdog timer (WDT)	200 ms
On computation error	Stop
On expanded command error	Stop
On fuse blown	Stop
On module verify error	Stop
On intelligent module program execution error	Stop
On file access error	Stop
On memory card operation error	Stop
On external power OFF	Stop
Carry out battery check	Yes
Carry out fuse blown check	Yes
Verify module	Yes
Constant scanning	
Breakdown history	Recod in PLC RAM
SFC program start mode	Initial start
Start conditions	Do not autostart block 0
Output block when the block is stopped	Keep ON

IRQ pointer settings

Line	PLC side		Intelligent module side	
No.	IRQ pointer start number	IRQ pointer no. of module	Start I/O number	Start SI number

System Variables

Word Range	D6144 to D12287
Bit Range	M4096 to M8191
System Timers Standard	64 to 2047
System Timers Acumlt	
System Counters	512 to 1023
System Labels	2048 to 4095
Step Flags	0 to 8191

Boot options

Clear program memory	No
Create system area to speed up monitoring from other stations	0 KSteps
Create system area to enable Multi Block Online Change (MBOC)	0 KSteps
Auto Download all data from Memory card to Standard Rom	No

Boot file settings

LINE	TYPE	DATA NAME	TRANSFER FROM	TRANSFER TO
1	Sequence	MAIN	Memory card RAM	Program memory
2	Parameter	PARAM	Memory card RAM	Program memory
3	Sequence	CONSIST	Memory card RAM	Program memory

Multiple CPU settings

Number of PLCs	1

Operating mode

n	Stop all stations on STOP of PLCn	Synchronize the start-up of PLCn
1	Yes	

Online modul change

Enable online modul change with another PLC	No

I/O sharing

All CPUs can access all inputs	No
All CPUs can access all outputs	No

MELSECNET / CC IE / Ethernet settings

Module No.	Network Type	Mode	Starting I/O No.	Network No.	Group No.
1	Empty				
2	Empty				
3	Empty				
4	Empty				
5	Empty				
6	Empty				
7	Empty				
8	Empty				

Comp (Prio = 31, Event = TRUE)

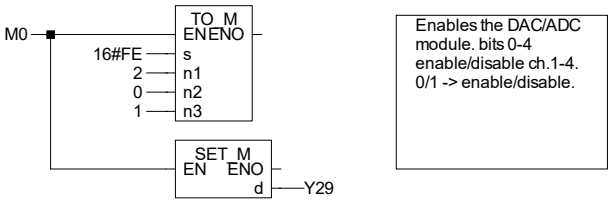
	POU name	Comment
0	ADC	ADC
1	Rampning	Fläkt_ramp
2	DAC	DAC
3	Varvtalsjustera	Jämför mellan börvärde och ärvärde och justerar varvtalet därefter.
4	PIC_to_PLC	Tar in digitalt värde 0-F genom fyra inportar.

ADC [PRG] Body [FBD] Network#1

Network #1 (1) Label: Title:

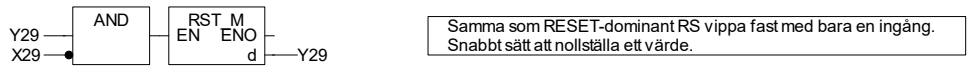
ADC [PRG] Body [FBD] Network#2

Network #2 (1) Label: Title:



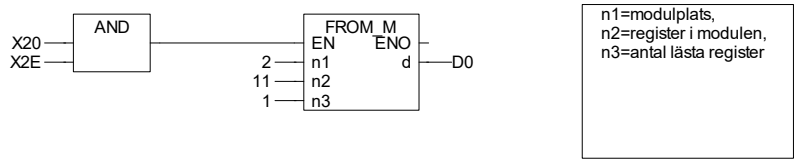
ADC [PRG] Body [FBD] Network#3

Network #3 (1) Label: Title:



ADC [PRG] Body [FBD] Network#4

Network #4 (1) Label: Title:

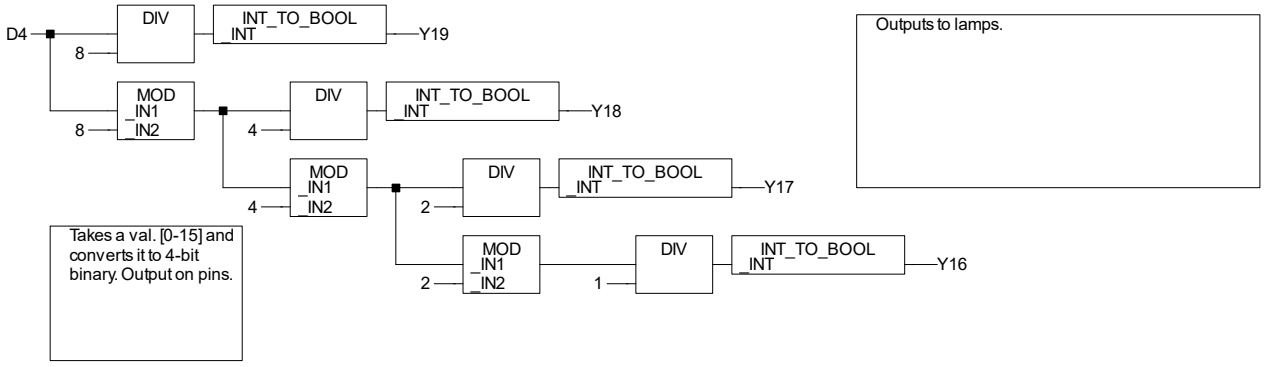


ADC [PRG] Body [FBD] Network#5

Network #5 (1) Label: Title:

ADC [PRG] Body [FBD] Network#6

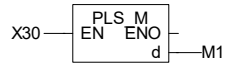
Network #6 (1) Label: Title:



Network #6 (2) Label: Title:

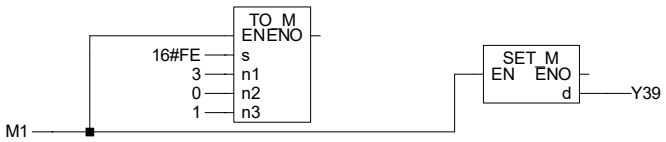
DAC [PRG] Body [FBD] Network#1

Network #1 (1) Label: Title:



DAC [PRG] Body [FBD] Network#2

Network #2 (1) Label: Title:

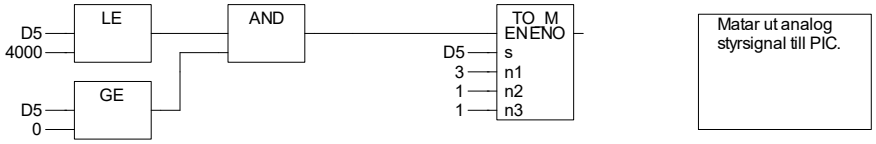


DAC [PRG] Body [FBD] Network#3

Network #3 (1) Label: Title:

DAC [PRG] Body [FBD] Network#4

Network #4 (1) Label: Title:

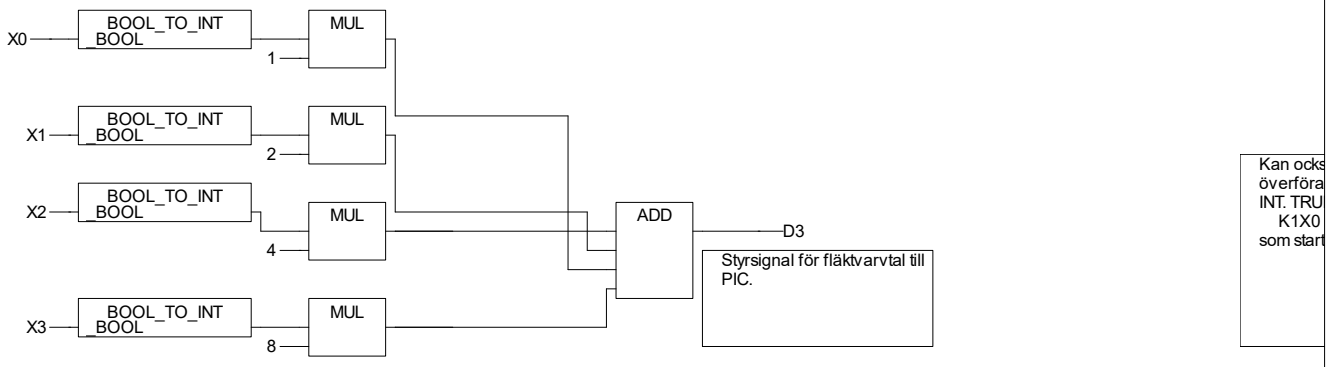


DAC [PRG] Body [FBD] Network#5

Network #5 (1) Label: Title:

PIC_to_PLC [PRG] Body [FBD] Network#1

Network #1 (1) Label: Title:



				Date			2016-05-25 11:26:13	C:\Users\john3\Sync\Chalm...\Prog_main
				Drawn				DAC [PRG] Body [FBD] Network#2
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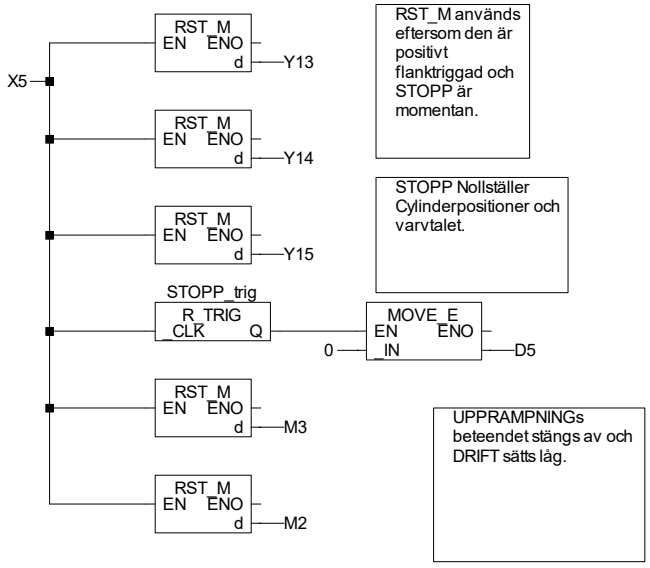
Network #1 (2) Label: Title:

Kan också pröva MOV_M för att direkt överföra bitinformationen till en 16-bitars INT. TRUE->EN, K1X0->s, d->Utvärde.
K1X0 innebär 1*4 bitar i följd med X0 som startadress.

Rampning [PRG] Body [FBD] Network#1

Network #1 (1) Label: Title:



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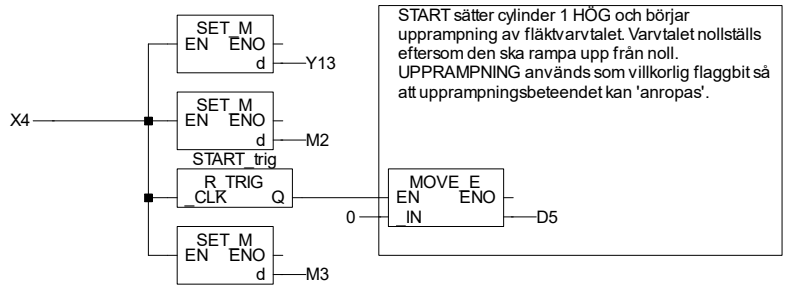
				Drawn				PIC_to_PLC [PRG] Body [FBD] Network#
				Appr.				Page: 6
Rev	Change	Date	Name	Rel.				

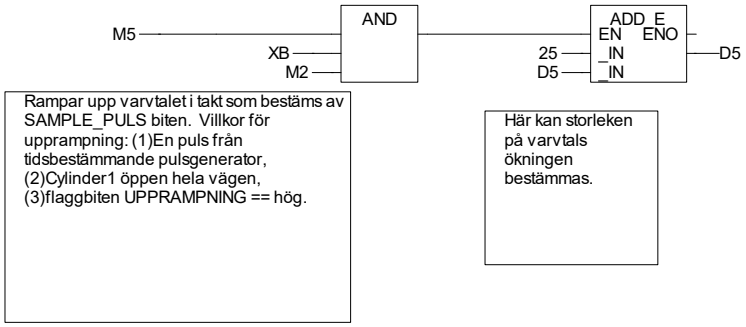
Rampning [PRG] Body [FBD] Network#2

Network #2 (1) Label: Title:



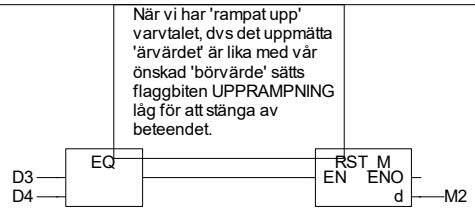
Rampning [PRG] Body [FBD] Network#3

Network #3 (1) Label: Title:



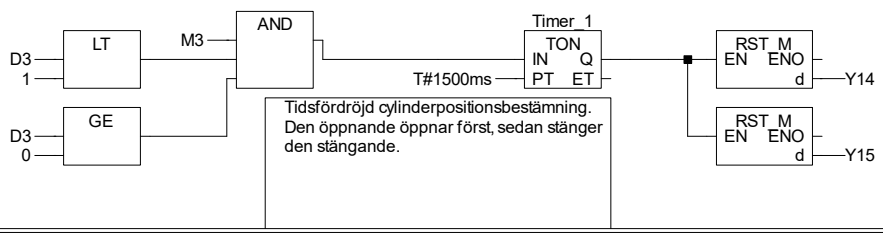
Rampning [PRG] Body [FBD] Network#4

Network #4 (1) Label: Title:



Rampning [PRG] Body [FBD] Network#5

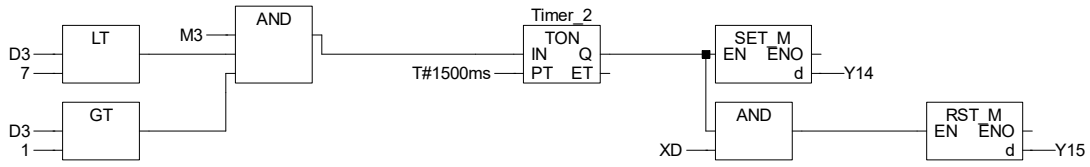
Network #5 (1) Label: Title:



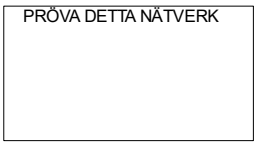
				Date			2016-05-25 11:26:13	C:\Users\john3\Sync\Chalm...\Prog_main
				Drawn				Rampning [PRG] Body [FBD] Network#2
				Appr.				Page: 7
Rev	Change	Date	Name	Rel.				

Rampning [PRG] Body [FBD] Network#6

Network #6 (1) Label: Title:

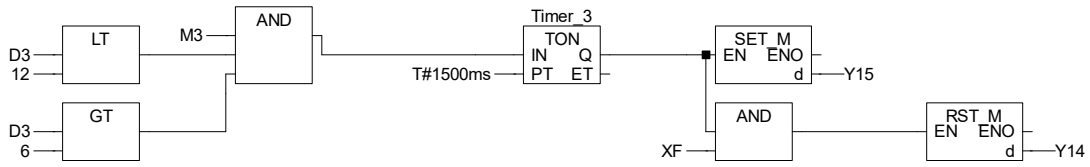


Network #6 (2) Label: Title:



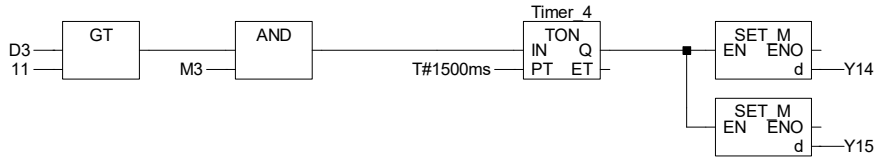
Rampning [PRG] Body [FBD] Network#7

Network #7 (1) Label: Title:



Rampning [PRG] Body [FBD] Network#8

Network #8 (1) Label: Title:

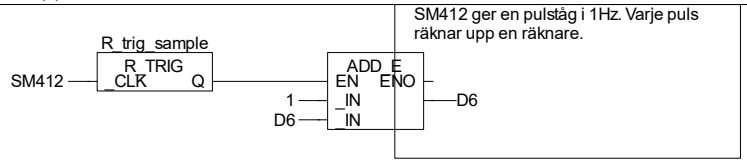


Comment of unit_test [PRG]:

This POU can be used as a 'sandbox' for testing different functions, variables, initial values, fake inputs etc etc... To disable, simply remove from the TASK POOL.

Varvtalsjustera [PRG] Body [FBD] Network#1

Network #1 (1) Label: Title:



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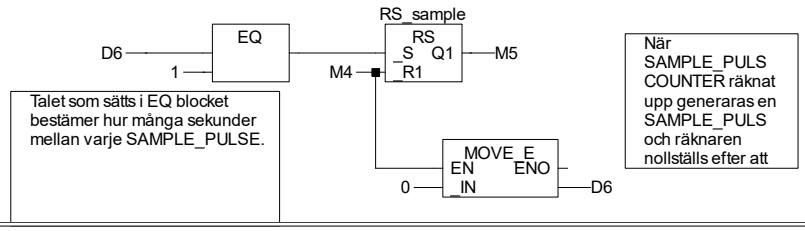
				Drawn				Rampning [PRG] Body [FBD] Network#6
				Appr.				Page: 8
Rev	Change	Date	Name	Rel.				

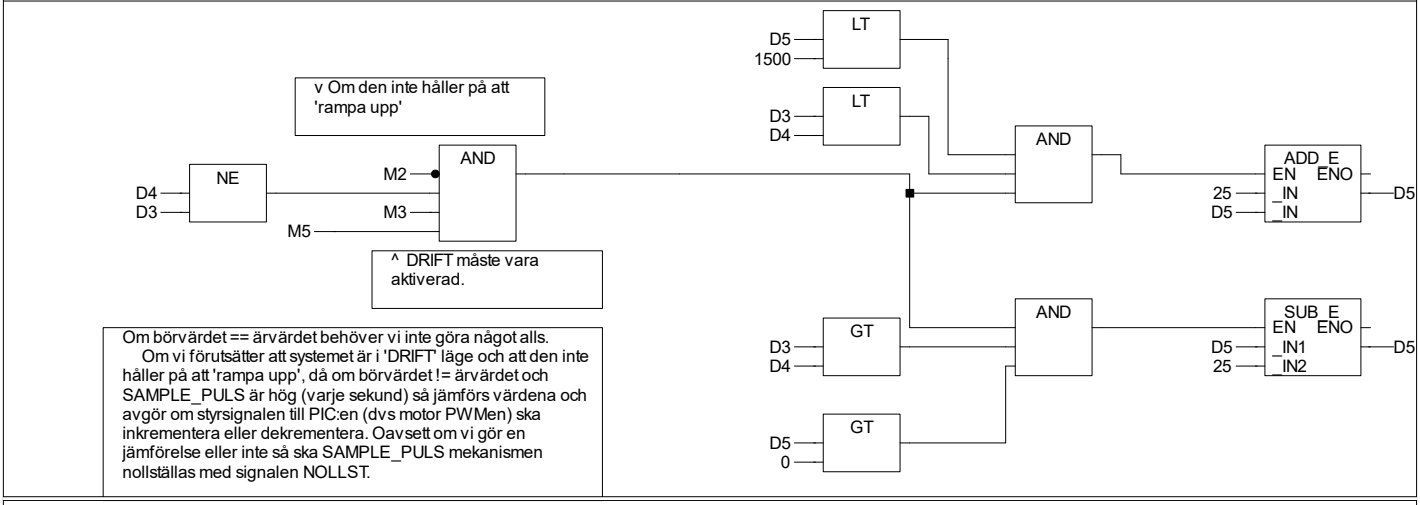
Varvtalsjustera [PRG] Body [FBD] Network#2

Network #2 (1) Label: Title:



Varvtalsjustera [PRG] Body [FBD] Network#3

Network #3 (1) Label: Title:



Network #3 (2) Label: Title:

Varvtalsjustera [PRG] Body [FBD] Network#4

Network #4 (1) Label: Title:

				Date			2016-05-25 11:26:13	C:\Users\john3\Sync\Chalm...\Prog_main
				Drawn				Varvtalsjustera [PRG] Body [FBD] Networ
				Appr.				Page: 9
Rev	Change	Date	Name	Rel.				