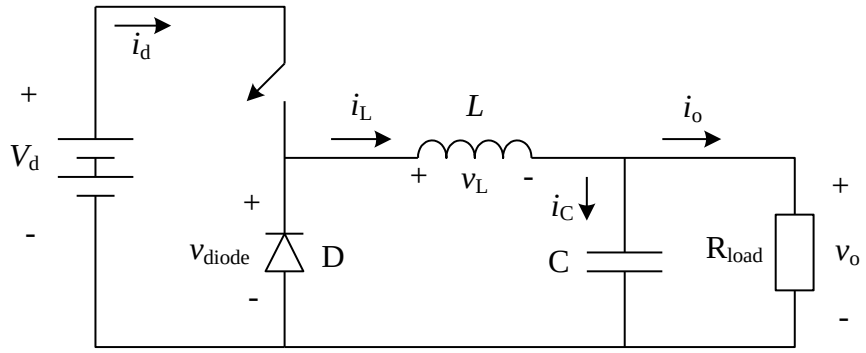
Solution of demonstration 3

Problem 1 Buck Converters



In a step-down converter consider all components to be ideal. Let the output voltage be held constant at 5V by controlling the switch duty ratio D. The input voltage (V_d) is 30V, the switching frequency (f_{sw}) is 50 kHz, the inductance is 100 μH, the capacitance is 470 μF and the output power is 40W. Ignore the forward voltage drop on the diode.

(a) Plot the input current, $i_d(t)$.
(b) Calculate the average input current, I_d.
(c) For a reduction of 10% in V_d, calculate I_d.
(d) Calculate the output voltage ripple.
(e) The output power to the load is suddenly decreased to 2W. What happens in the circuit? Derive an expression for the input/output voltage ratio.
(f) If a more realistic circuit is considered, both the switch and the diode have a voltage drop. How does this resistance influence the expression for the input/output voltage ratio (Duty cycle) when the converter is operating in CCM?

Solution

(a) Plot the input current, $i_d(t)$.

To be able to plot $i_d(t)$ we must first calculate the time the switch is conducting, $t_{on} = DT_{sw}$ where $T_{sw} = 1/f_{sw}$. We start by assuming that the buck converter is operating in steady-state and CCM (continuous conduction mode which means that the inductor current always is greater than zero). The output voltage is assumed to be a pure DC-voltage since the output capacitor is relatively large. For a system in steady state, we know that:

$$v_L(t) = L\frac{di_L(t)}{dt} \quad \rightarrow \quad i_L(T_{sw} + t_0) = i_L(t_0) + \frac{1}{L}\int_{t_0}^{T_{sw}+t_0} v_L(t)dt$$

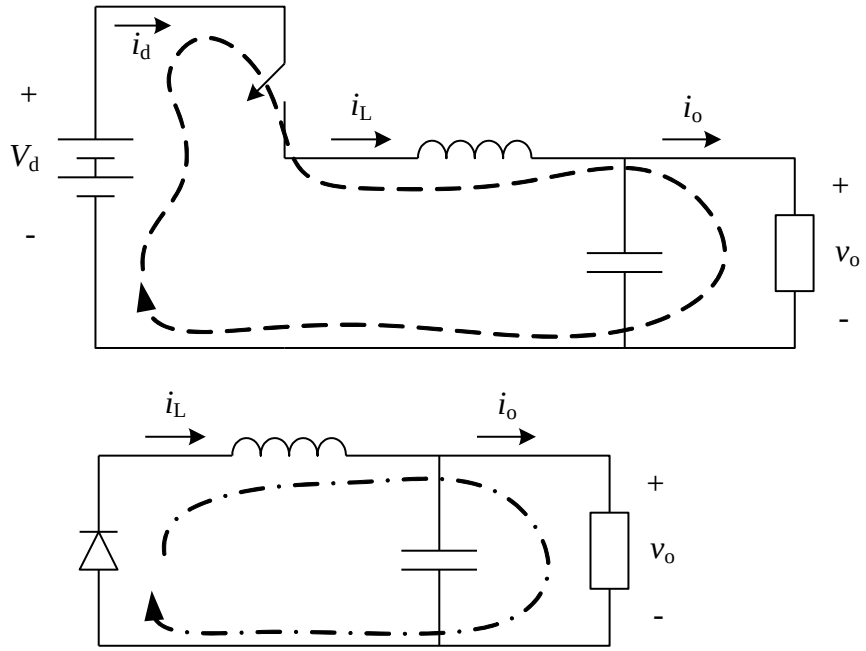
$$i_c(t) = C\frac{dv_c(t)}{dt} \quad \rightarrow \quad v_c(T_{sw} + t_0) = v_c(t_0) + \frac{1}{C}\int_{t_0}^{T_{sw}+t_0} i_c(t)dt$$

But since the system is operating in steady state we know that $i_L(T_{sw} + t_0) = i_L(t_0)$ and $v_c(T_{sw} + t_0) = v_c(t_0)$. This results in:

$$0 = \frac{1}{C}\int_{t_0}^{T+t_0} i_C(t)dt \qquad \text{and} \qquad 0 = \frac{1}{L}\int_{t_0}^{T+t_0} v_L(t)dt$$

From this derivation it can be seen that the average of the inductor voltage and the average of the capacitor current must be zero in steady state. The integral above can be compared with the definition for averaging an arbitrary function.

As in demonstration 1, the fact that the average inductor voltage equals zero over one switching period can be used to derive the ratio between input and output voltage. As mentioned before, we have assumed CCM operation which means that a continuous current is flowing through the inductor. This gives that when the switch is on, the inductor current (i_L) goes through the switch and the diode is blocking. When the switch is off, the inductor current is freewheeling through the diode, see pictures below.

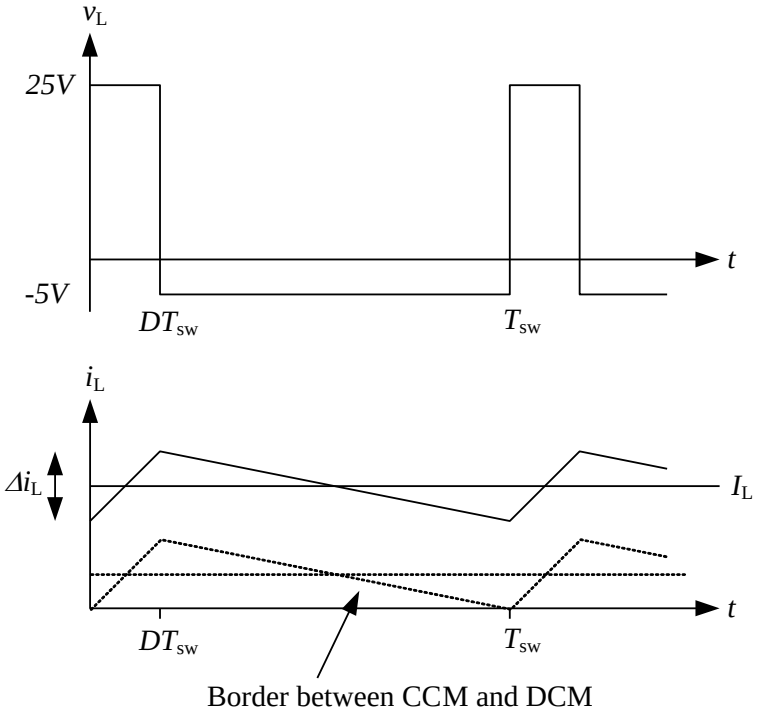


Since we have assumed a large output capacitor, the output voltage is assumed to be a constant DC-voltage. When the switch is turned on, the inductor voltage becomes: $v_L = V_d - V_o$. When the switch is off, the inductor voltage becomes: $v_L = -V_o$.

$$V_L = \frac{1}{T_{sw}}\int_0^{DT_{sw}} V_d - V_o dt + \frac{1}{T_{sw}}\int_{DT_{sw}}^{T_{sw}} -V_o dt = \frac{1}{T_{sw}}(V_d DT_{sw} - V_o DT_{sw} - V_o T_{sw} + V_o DT_{sw}) = 0$$

$$V_o = V_d D \quad \rightarrow \quad D = \frac{V_o}{V_d} = \frac{5V}{30V} = 0.167$$

The inductor voltage and current can now be plotted:



Since v_L and L are constant the derivative of the inductor current must be constant. This gives a linear increase and decrease of the inductor current.

Now we have to check our assumption of CCM. From the figure we see that if $I_L \geq \Delta i_L/2$ then the converter is operating in CCM. During the on-time of the switch, the inductor voltage is constant $(v_L = V_d - V_o)$ which gives

$$v_L = L\frac{\Delta i_L}{\Delta t} \quad \rightarrow \quad \Delta i_L = \frac{v_L \Delta t}{L} = \frac{(V_d - V_o)\cdot DT_{sw}}{L} = \frac{(30V - 5V)}{100\mu H}\cdot\frac{1}{6}\cdot\frac{1}{50kHz} = 0.83A$$

The next step is to define and calculate the average inductor current, I_L. We know that the inductor current (i_L) consists of two parts, i_C and i_o. Since the converter is operating in steady-state, the average current must be zero $(I_C = 0)$, and the since the output voltage is a DC-voltage, the output current must also be pure DC-current $(i_o = I_o)$ due to the purely resistive load. The average capacitor current can be calculated as:

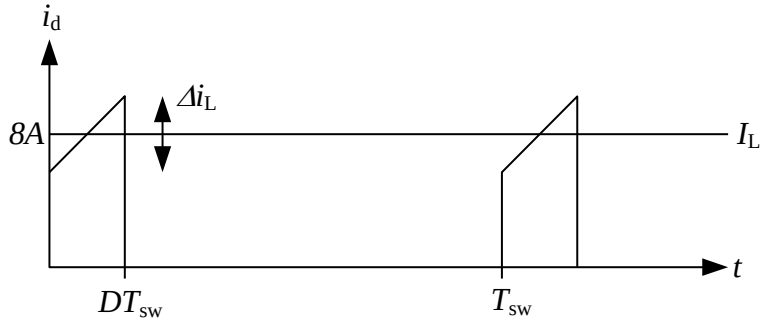
$$I_C = \frac{1}{T_{sw}}\int_0^{T_{sw}} (i_L(t) - I_o)dt = \frac{1}{T_{sw}}\int_0^{T_{sw}} i_L(t)dt - I_o = 0 \quad \rightarrow \quad \frac{1}{T_{sw}}\int_0^{T_{sw}} i_L(t)dt = I_o = I_L$$

The average inductor current must be equal to the output current. This gives that the ripple current in the inductor must go through the capacitor $\left(i_C = i_{L(ripple)} = i_L - I_L\right)$.

$$I_o = I_L = \frac{P_o}{V_o} = \frac{40W}{5V} = 8A$$

The assumption of CCM is valid since $(8A = I_L) > (\Delta i_L/2 = 0.415)$. We know that when the switch is on $i_d = i_L$ and when it is off $i_d = 0$.

The input current $i_d(t)$ can now be plotted:



(b) Calculate the average input current, I_d.

We go back to the definition for average of a waveform and apply it on the input current.

$$I_d = \frac{1}{T_{sw}} \int_0^{T_{sw}} i_d(t)dt = \frac{DT_{sw}}{T_{sw}} \frac{1}{DT_{sw}} \int_0^{DT_{sw}} i_d(t)dt = \frac{DT_{sw}}{T_{sw}} \cdot I_L = DI_L = 8A \cdot \frac{1}{6} = 1.33A$$

Another way is to assume that the converter is loss-less:

$$P_d = P_o \quad \rightarrow \quad I_d = \frac{I_o V_o}{V_d} = \frac{DV_d I_o}{V_d} = DI_o$$

(c) For a reduction of 10% in V_d, calculate I_d.

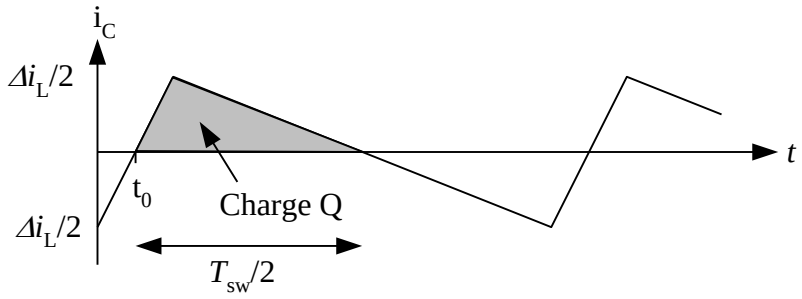
We know that the output voltage is controlled to be constant.

$$I_d = \frac{P_o}{V_d} = \frac{P_o}{0.9 \cdot V_d} = \frac{40W}{0.9 \cdot 30V} = 1.48A$$

(d) Calculate the output voltage ripple.

The average inductor current is equal to the output current ($I_o = I_L$), and the inductor current is equal to the capacitor current plus the output current ($i_L = i_C + i_o$). This gives that the ripple current in the inductor must go through the capacitor ($i_C = i_{L(ripple)} = i_L - I_L$).

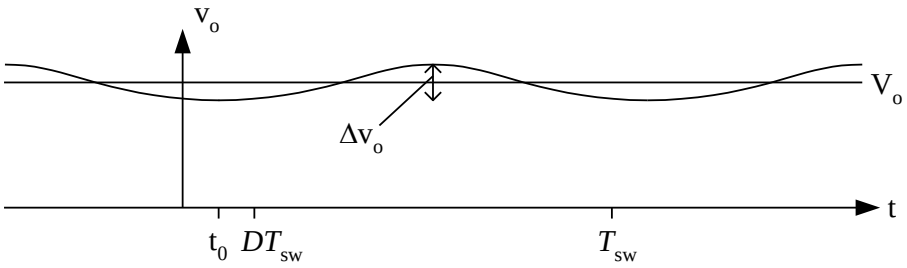
We now plot the capacitor current.



For the voltage across the capacitor we know that it can be expressed as:

$$v_c(t) = v_c(t_0) + \frac{1}{C}\int_{t_0}^{t_0+T} i_c(t)dt$$

This gives that the voltage a time t is the voltage at time t_0 plus the integral of the current from the time t_0 to t. The capacitor current is a linear function, as shown above. This gives that the shape of the output voltage will be some polynomial function of second degree. An approximate figure of the output voltage ripple can be drawn as:



We don't have to solve this because we are only interested of finding the peak-to-peak ripple in the output voltage. From the figure we see that from the time t_0 the capacitor current is positive to time $t = t_0 + T_{sw}/2$. This gives that the capacitor voltage will increase from time t_0 to time $t = t_0 + T_{sw}/2$. The peak-to-peak ripple in the output voltage can then be calculated by

$$\Delta v_o = v_c\left(t_0 + {}^{T_{sw}}/_{2}\right) - v_c(t) = \frac{1}{C}\underbrace{\int_{t_0}^{t_0+T_{sw}/2} i_c(t)dt}_{Charge} = \frac{Q}{C}$$

The integral of the capacitor current is equal to the charge put into the capacitor (marked with a Q in the figure above). From the figure above it can be seen that the charge is equal to the area under the capacitor current, marked with grey in the figure. The output ripple can be expressed as:

$$\Delta v_c = \frac{Q}{C} = \frac{1}{C}\cdot 0.5 \cdot \frac{\Delta i_L}{2}\cdot\frac{T_{sw}}{2} = \frac{\Delta i_L}{8\cdot C\cdot f_{sw}}$$

Where Δi_L can be expressed as:

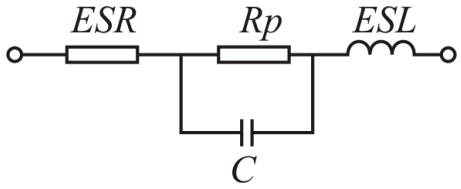
$$\Delta i_L = \frac{(V_d - V_o)D}{f_{sw}L}$$

The final expression for the voltage ripple can now be written as:

$$\Delta v_c = \frac{(V_d - V_o) \cdot D}{8 \cdot f_{sw}^2 \cdot L \cdot C} = \cdots = 4.43mV$$

The approximation of the output voltage to be a pure DC voltage is reasonable ($4.43mV << 5V$). It can also be noticed that the output voltage ripple is independent of the load current in CCM.

Comment: The calculated value on the voltage ripple is based on an ideal capacitor. In reality, every capacitor has some losses. A real capacitor has an in-phase AC resistance called the Equivalent Series Resistance (ESR). ESR is the sum of in-phase AC resistance and includes resistance of the dielectric, plate material, electrolytic solution, and terminal leads. ESR acts like a resistor in series with a capacitor (thus the name) and is specified at a certain frequency. An equivalent model of a capacitor can be seen in the Figure below.



ESR is the equivalent series resistor, ESL is the equivalent series inductance and R_p is the parallel resistor that causes leakage current.

If the non ideal capacitor model pictured above is used in the buck converter, the voltage ripple will become significantly higher due to the ESR.

(e) The output power to the load is suddenly decreased to 2W. What happens in the circuit? Derive an expression for the input/output voltage ratio.

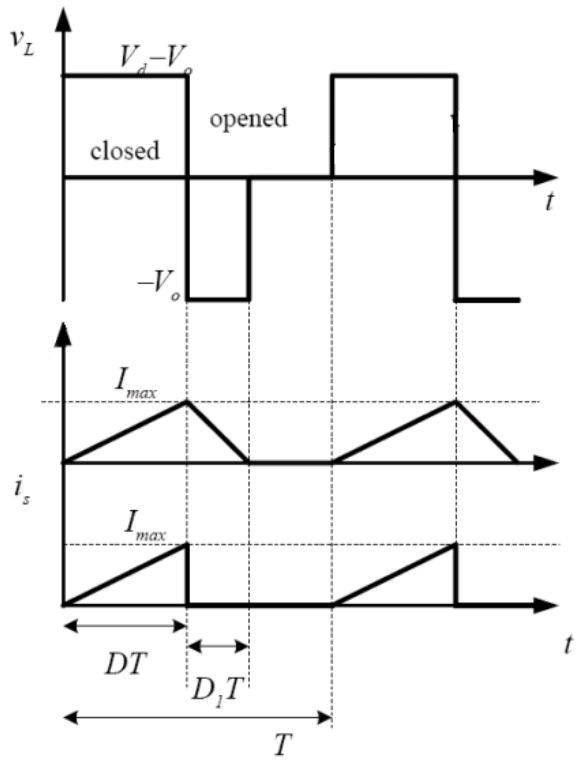
Since the output voltage is regulated, the current is determined by the load resistance. In this case, the resistance is suddenly increased. The duty cycle is regulated in such a way that the output voltage is kept constant.

$$I_o = \frac{P_o}{V_o} = \frac{2W}{5V} = 0.4A$$

Also assume that the duty-cycle is kept constant in this case. Consequently, the current ripple is kept constant since the input-, output voltage and inductance is kept constant.

$$v_L(t) = L\frac{di_L(t)}{dt} = L\frac{\Delta i_L}{\Delta t} \quad \rightarrow \quad \Delta i_L = \frac{v_L \Delta t}{L} = \frac{(V_d - V_o)DT_{sw}}{L} = 0.83A$$

We now note that $I_L \geq \Delta i_L/2 \quad \rightarrow \quad 0.4A \geq 0.83A/2$ no longer is valid. Hence is the converter operating in DCM.



The ratio between input and output voltage can be calculated via the average inductor voltage:

$$V_L = \frac{1}{T_{sw}} \int_0^{DT_{sw}} V_d - V_o dt + \frac{1}{T_{sw}} \int_{DT_{sw}}^{(D+D_1)T_{sw}} -V_o dt \quad \rightarrow \quad \frac{V_o}{V_d} = \frac{D}{D + D_1}$$

The Average load current is the average inductor current:

$$\Delta i_L = \frac{(V_d - V_o)DT}{L} = \frac{V_o D_1 T}{L} \tag{1}$$

$$I_o = \frac{V_o}{R} = \frac{\Delta i_L}{2}(D + D_1) \tag{2}$$

Inserting (1) into (2) gives:

$$\frac{V_o}{R} = \frac{V_o D_1 T}{2L}(D + D_1) \quad \rightarrow \quad D_1^2 + DD_1 = \frac{2L}{RT}$$

Solving for D_1 gives:

$$D_1 = -\frac{D}{2} + \sqrt{\frac{D^2}{4} + \frac{2L}{RT}}$$

Inserted in newly derived expression for input/output voltage ratio gives the final expression for the duty-cycle:

$$V_o = V_d\left(\frac{D}{D+D_1}\right) = V_d\left(\frac{D}{\frac{D}{2}+\sqrt{\frac{D^2}{4}+\frac{2L}{T\cdot R}}}\right) = V_d\left(\frac{2D}{D+\sqrt{D^2+\frac{8L}{T\cdot R}}}\right)$$

(f) If a more realistic circuit is considered, both the switch and the diode have a voltage drop. How does this resistance influence the expression for the input/output voltage ratio (Duty cycle) when the converter is operating in CCM?

The voltage drop over the diode and switch are considered at both time periods, i.e. when the switch is open and when it is closed. During the time when the switch is closed, the inductor voltage can be expressed as:

$$v_L = V_d - V_o - V_{switch}$$

Where V_{switch} is the voltage drop across the switch. During the time when the switch is open the inductor voltage can be expressed as:

$$v_L = -V_o - V_{diode}$$

Where V_{diode} is the voltage drop across the diode. The average voltage over the inductor can be expressed as:

$$V_L = \frac{1}{T_{sw}}\int_0^{DT_{sw}} (V_d - V_o - V_{switch})dt + \frac{1}{T_{sw}}\int_{DT_{sw}}^{T_{sw}} (-V_o - V_{diode})dt$$

$$V_L = (V_d - V_o - V_{switch})D + (-V_o - V_{diode})(1-D) = 0$$

$$V_o = V_d D - V_{switch}D - V_{diode}(1-D)$$

Which is less than for the ideal case. The output voltage is consequently lower for an ideal converter than it is in the ideal case. This can also be seen during the PSpice laborations.