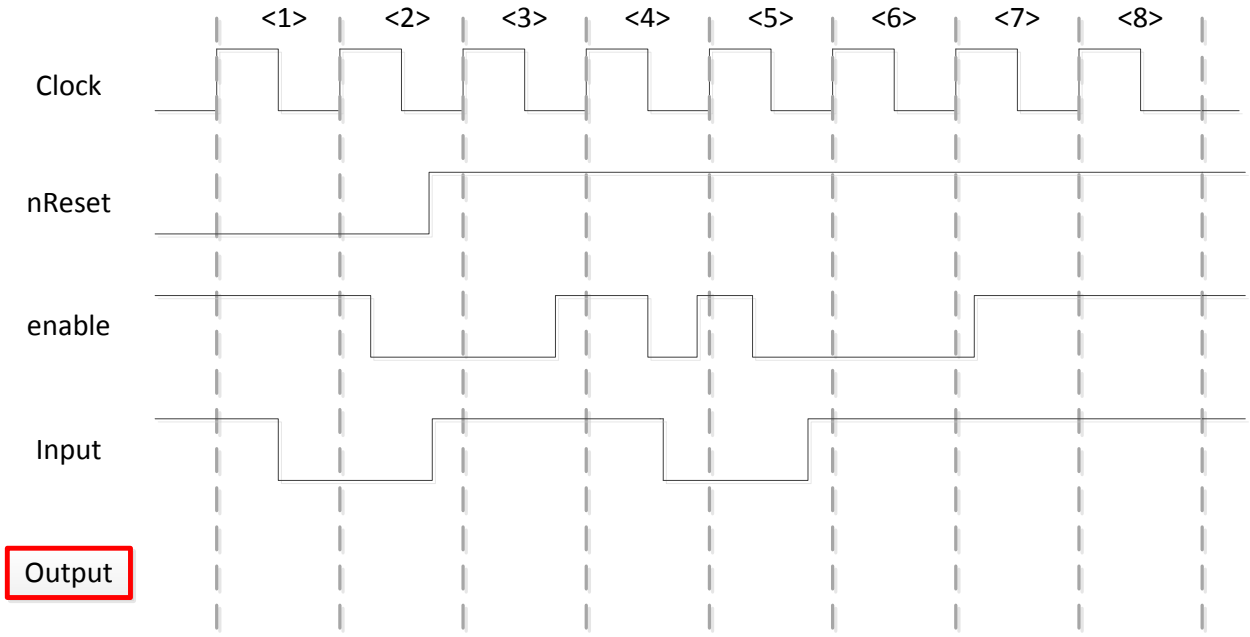
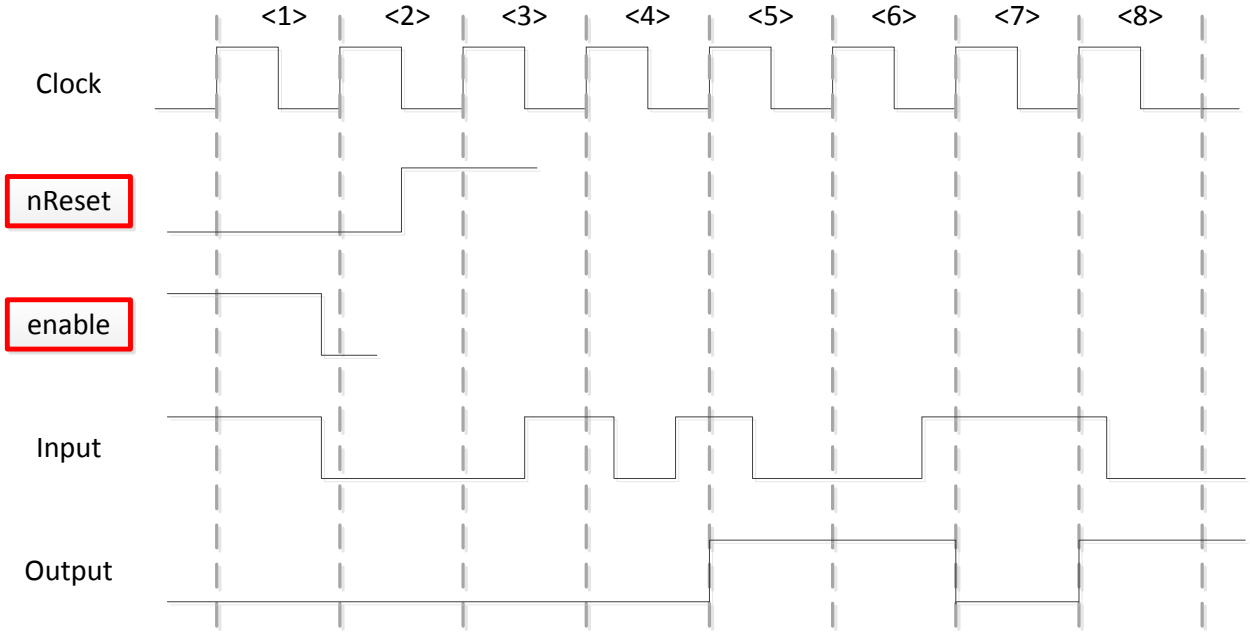
Flip flops

A) Draw the signal "Output"

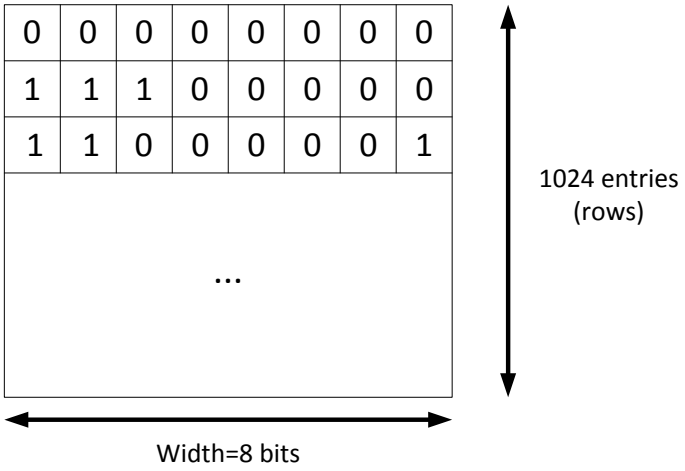


B) Draw the signals "nReset" and "enable" given the "Output" and "Input"



Memory

Suppose that we would like to implement in VHDL the following memory. It has 1024 entries and each wordline (entry) can save words of 8 bits.



Please answer to the following questions:

1) What is the size of memory (in bits)? Which column saves the most significant bit and which the least significant one? Mark them in the figure above.

2) What is the width of the address signal that is needed to access this memory?

3) Write the VHDL command to create a memory array for the memory above. Use the format, as given in the box below. The number of entries should be expressed using the address width (see question 2). The data size should be expressed in the same way we declare a signal.

```
Type MEMORY_ARRAY is ARRAY (<number of entries>) of <data type>(<data size>)
```

4) Given the following code and the memory above, what is the value of the signal "out" ?

```
signal temp: MEMORY_ARRAY;
signal out: std_logic_vector (7 downto 0);
out <= temp(2);
```