EDA321: Digital Design
Sample Exam

Date: xx-xx-xx

Time: **xx:00-xx:00**

Examiner: Ioannis Sourdis

Department: Computer Science and Engineering

Inquiries: Ioannis Sourdis (extension 1744); will visit the room at **xx:00** and at **xx:00**

Results and grading review: See me in my office on xx-xx-xx.

Duration: 4 hours

Grading scale: 100 points

Chalmers:
0: 0%-39%, 3: 40%-59%, 4: 60%-79%, 5: 80%-100%
GU:
Fail (U): 0%-39%, Pass (G): 40%-69%, Pass with Distinction (VG): 70%-100%
Available references: Blank paper and a calculator are allowed. No text books, lecture notes, research articles, etc. are allowed.

General: Submit your solutions, in English, on blank paper sheets. Write legibly; feel free to use figures to get your point across.

Please start the solutions for each problem on a new sheet. Please number the sheets so that the solutions are in numerical order.

Note that it is possible to receive partial credit for an answer even if it is not 100% correct.

Your personal identity code is required on each submitted sheet!

Good luck!

IMPORTANT NOTE: This example exam is provided only to give a feeling on the style of questions that the final exam of the course will have. Its is not indicative of the topics to be covered in the exam and therefore it is strongly not recommended to focus your study based on this examples.

Question 1: (10 points – 30 minutes)

Book exercise 4.25

Question 2: (5 points - 10 minutes)

Book exercise 6.7

Question 3: (15 points – 30 minutes)

a) Draw and describe an 8-bit carry-select adder with blocks of 4 bit ripple carry adders. Assume that a full-adder is given. (8 points)
b) What is the critical path (2-points)
c) How the critical path of the adder increases as the number of bits increase when keeping the same block size? (3-points)
d) Compare the delay and the area of the carry-select adder with the one of the ripple carry adder. (2-points)

Question 4: (3 points – 10 minutes)

Compare an ASIC, an FPGA and a general-purpose processor running software in terms of performance, and flexibility/programmability?

Question 5: (20 points – 40 minutes)

Book exercise 8.46

Question 6: (9 points – 30 minutes)

Book exercise 11.2

Question 7: (8 points – 15 minutes)

Book exercise 7.24

Question 8: (5 points – 10 minutes)

What are the differences between a coarse-grain and a fine-grain reconfigurable device? In general, which one is better in terms of flexibility, performance, power, and area?

Question 9: (5 points – 10 minutes)

What are the differences between an SRAM and a DRAM cell?

Question 10: (5 points – 10 minutes)

Which are the means a hardware designer can use to reduce the power consumption of a design, provided that the VLSI CMOS fabrication technology is fixed and she/he cannot control it?

Question 11: (15 points – 30 minutes)

Make a binary and an one-hot state assignment of the FSM in the figure of Lecture 7 slide 18. Draw the hardware design of each case using D-flip-flops. Which one is faster (find the critical path)? Which one needs less area?

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Alternative Question 11: (15 points – 30 minutes)

a. Make the binary multiplication of 1001*1101 (2 points)
b. Draw the design of a 4x4-bit array multiplier and explain how it works. (10 points)
c. What is the critical path? (3 point)

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