EDA322: Digital Design
Exam - August 2017

Date: August 24, 2017

Time: **14:00-18:00**

Examiner: Ioannis Sourdis

Department: Computer Science and Engineering

Inquiries: Ioannis Sourdis (extension 1744); will visit the room at **15:30** and at **17:00**

Results and grading review: room 4128 EDIT on **September 15th at 11:00**.

Duration: 4 hours

Grading scale: 100 points in total

Chalmers:
0: 0%-49%, 3: 50%-64%, 4: 65%-84%, 5: 85%-100%
GU:
Fail (U): 0%-49%, Pass (G): 50%-79%, Pass with Distinction (VG): 80%-100%

Available references: a calculator is allowed. No textbooks or lecture notes, etc. allowed.

General: Submit your solutions, in English, on blank paper sheets. Write legibly; feel free to use figures to get your point across.

The order of answering the questions does not matter (start with the easiest ones).

Please start the solutions for each problem on a new sheet. Please number the sheets so that the solutions are in numerical order.

Note that it is possible to receive partial credit for an answer even if it is not 100% correct.

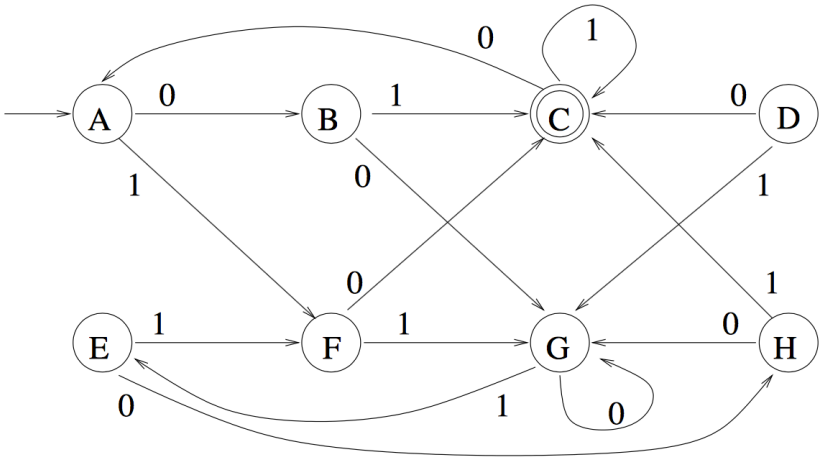
Your personal identity code is required on each submitted sheet!

Good luck!

Question 1: (10 points)
Design in gatelevel a circuit that takes as an input a 4-bit integer A(3:0) and produces the integer part of the result of the following equation R= A*(9/8)

Answer:
R= A*(9/8) = A + A/8
A/8 requires a shift right of 3 bits and then the result should be added to A with a 4-bit adder

Question 2: (10 points)
Minimize the states of the FSM described by the following state diagram using an implication table, then, rewrite the state diagram:



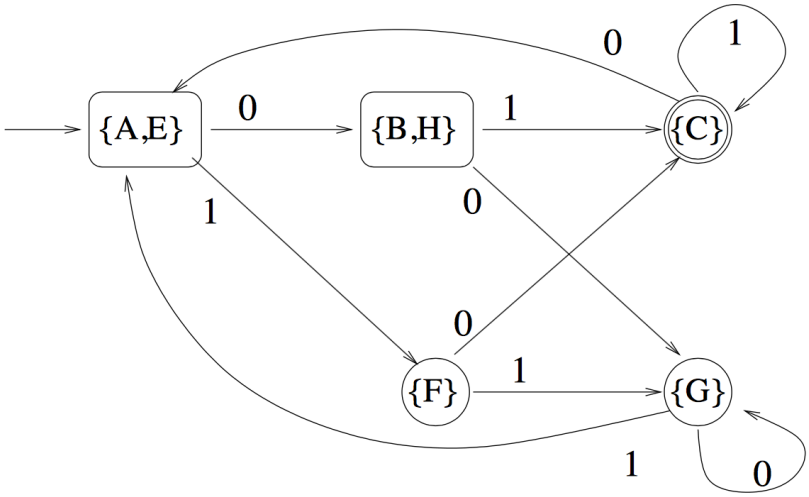
All states give "0" (zero) to the output except state C which gives "1".

Answer:

B						
C	X	X				
E			X			
F			X			
G			X			
H			X			
	A	B	C	E	F	G

B	X					
C	X	X				
E		X	X			
F	X	X	X	X		
G		X	X		X	
H	X		X	X	X	X
	A	B	C	E	F	G

B	X					
C	X	X				
E		X	X			
F	X	X	X	X		
G	X	X	X	X	X	
H	X		X	X	X	X
	A	B	C	E	F	G



Question 3: (10 points)
a) What is the main (types of) "resources" that an FPGA contains? What other specialized modules may be included in an FPGA?
b) What are the most area and power consuming resources? Why is that in your opinion?

Answer:
Lecture 11, slides 9, 35-39, 42, 44

Question 4: (10 points)
Draw the block diagram of a bus that connects 4 clients and the block diagram of a crossbar that connects 4 clients. Consider that a client makes a transaction (communicates data to another client) when the bus or the crossbar allows with a delay of one cycle. Show the timing of the following transactions (all requests are created and are available in cycle 0):

- Client 1 to Client 2
- Client 2 to Client 1
- Client 3 to Client 4
- Client 4 to Client 3
- Client 1 to Client 4
- Client 1 to Client 2
- Client 2 to Client 1

How many cycles does a bus need for the transactions and how many does the crossbar?

Answer:
Crossbar needs 3 cycles, bus needs 7

Question 5: (10 points)
How can a memory block be used to implement combinational logic? When in your opinion would that be useful? What are the 3 types of Programmable Logic Devices and what are their main differences?

Answer:
Lecture 15 slide 37.

It would be useful if the combinational logic is too complex to implement with gates or it is required to be dynamically changed. In the second case the memory could be reprogrammed to like an FPGA logic cell to implement a new Boolean function.

Lecture 15, slide 39

Question 6: (10 points)
a) What is the difference between testing and verification?
b) What are the 3 different types of faults that can happen in a digital circuit and what are their causes?

Answer:
Lecture 16, slides 5, 11

Question 7: (10 points)
a) Draw the block diagram of a 4-bit array multiplier, showing the internals of a full-adder at least once.
b) Show the critical path of the design considering that the inputs and outputs of the multiplier are registered.

c) Considering that the delay of a XOR gate is 0.5 ns, the delay of an AND/OR gate is 0.2 ns, NOT gates have zero delay, the setup time of a flip-flop is 0.1 ns, the hold time of a flip-flop is 0.01ns and the propagation time of a flip-flop is 0.1 ns. Find the minimum clock period of the design.
d) Show how to best split the design in **two** pipeline stages in order to achieve the highest frequency. Show/Mark the wires in the block diagram that would be registered in this case. What would then be the minimum clock period of the design.

Answer:

a) Lecture 12, slide 17-18 (plus showing the FA internals)
b) Lecture 12, slide 18
c) 200 MHz (clock period 5 ns) 23-27, 32-18
d) All wires crossed by X3 and its projection to the right would be registered, then the critical path would be 2.7ns and the operating frequency 370 ns.

Question 8: (10 points)

Draw the block diagram and truth table of an SR-latch. Analyze the circuit following the methodology used in the asynchronous circuits and explain what would happen when if inputs change from SR=11 to SR=00

Answer:

Lecture 19, slides 18-20

Question 9: (10 points)

a) What does the delay of a gate depend on?
b) What does the delay of a wire depend on?

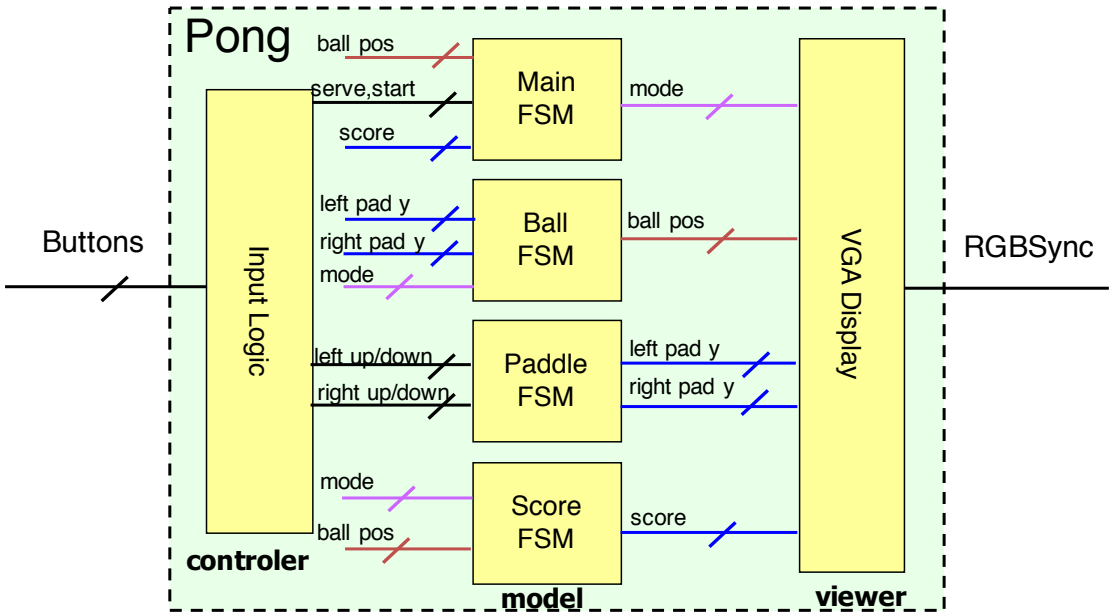
Answer:

Lecture 18, slides 9-17

Question 10: (10 points)

After defining the specifications of a system to be designed, a common practice to proceed with the designing step is to follow a Divide and Conquer approach.

a) Explain what is the Divide and Conquer approach in that context.
b) Describe the 3 different themes (styles/ways) you can apply Divide and Conquer for the design of a system.
c) What is (are) the theme(s) based on which the following system is designed. Explain why.



Answer:
Lecture 14, slides 5-9

END of EXAM