EDA322: Digital Design
Exam - June 2017

Date: June 9, 2017

Time: **14:00-18:00**

Examiner: Ioannis Sourdis

Department: Computer Science and Engineering

Inquiries: Ioannis Sourdis (extension 1744); will visit the room at **15:30** and at **17:00**

Results and grading review: room 4128 EDIT on **June 29th at 11:00**.

Duration: 4 hours

Grading scale: 100 points in total

Chalmers:
0: 0%-49%, 3: 50%-64%, 4: 65%-84%, 5: 85%-100%
GU:
Fail (U): 0%-49%, Pass (G): 50%-79%, Pass with Distinction (VG): 80%-100%

Available references: a calculator is allowed. No textbooks or lecture notes, etc. allowed.

General: Submit your solutions, in English, on blank paper sheets. Write legibly; feel free to use figures to get your point across.

The order of answering the questions does not matter (start with the easiest ones).

Please start the solutions for each problem on a new sheet. Please number the sheets so that the solutions are in numerical order.

Note that it is possible to receive partial credit for an answer even if it is not 100% correct.

Your personal identity code is required on each submitted sheet!

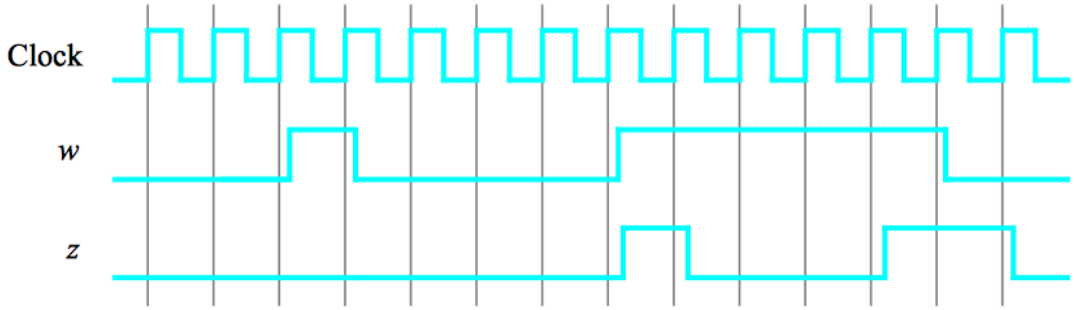
Good luck!

Question 1: (10 points)
Design in gatelevel a multiplier that multiplies a 4-bit integer A(3:0) with the constant decimal value "10" ('1010' in binary).

Answer:
Lecture 12, slide 6 with an additional least significant bit that is always zero. In addition the internals of the 4-bit adder should be shown, which could be a ripple carry adder.

Question 2: (10 points)

Design a synchronous FSM (Finite State Machine) that recognizes two specific sequences of applied input symbols, namely four consecutive 1s ("1111") or four consecutive 0s ("0000"). There is an input w and an output z. Whenever w = 1 or w = 0 for four consecutive clock pulses the value of z has to be 1; otherwise, z = 0. Overlapping sequences are allowed, so that if w = 1 for five consecutive clock pulses the output z will be equal to 1 after the fourth and fifth pulses. The Figure bellow illustrates the required relationship between w and z.

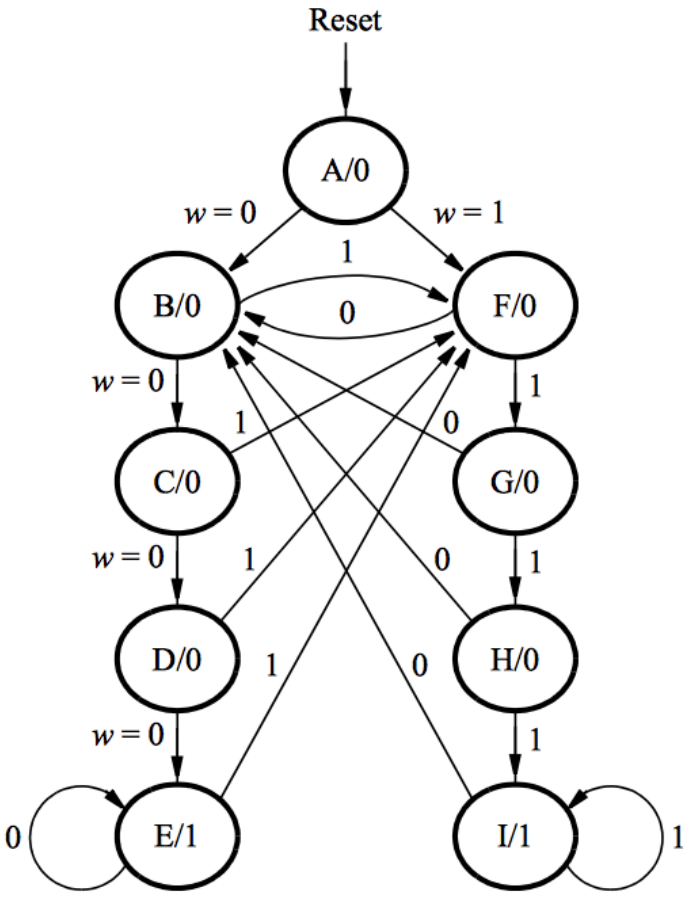


a) Draw the state-diagram of the FSM
b) Fill in the state-table of the FSM
c) Make a state-assignment and derive the Boolean functions that produce the next state bits and the output.
d) Draw the hardware design (block diagram) of the FSM.

Note: if there is any information missing in the above description of the FSM, feel free to define it yourselves. In such case, explain it in your answer.

Answer:
Similar to the example of lecture 7 slides 6-12

One possible state diagram:



Question 3: (10 points)
a) What is an FPGA configuration bitstream (also called datastream)? Which FPGA parts do the bits of a bitstream configure and how do they control the functionality of these parts?
b) What types of reconfiguration memories are there? What are the advantaged and disadvantages of each?

Answer:
Lecture 11, slides 46-48

Question 4: (10 points)
Draw and describe a bus, a crossbar and an interconnection network. What are their differences?

Answer:
Lecture 15, slides 5-8

A bus needs less area (logic and wires) than a crossbar or a network but allows one sender to use the bus at any point in time. Its performance becomes poor as the number of clients increase

A crossbar requires more area than a bus. The area grows in $O(n^2)$ where n is the number of clients). It allows every input to send data to a different output in one hop (cycle).

A network scales its area better than a crossbar (as the number of clients increase). It allows multiple clients to concurrently send data to the same or different destinations. Each transaction may take multiple hops to complete.

Question 5: (10 points)
Draw the block diagram of a 4x4 memory array (4 rows of 4–bits) using D-flip-flops. Find the maximum clock frequency of the memory block considering that:

- a 2-input AND gate or a 2-input OR gate has a delay of 1 ns,
- the setup time of a D flip flop is 0.5 ns,
- the hold time of a D flip flop is 0.1 ns,
- the propagation delay of a D flip flop is 0.5 ns,
- inverters and wires have zero delay

Answer:
Lecture 15 slide 15, 6 ns -> 166.66 MHz.

Question 6: (10 points)
The cost of a chip is 15 SEK when the yield is 75%. What should be the yield for the chip price to go down to 12 SEK?

Answer:
The cost of a chip (good or bad) is:
chip-cost = Wafer cost / total#chips

the cost of good chips is

Good-chip-cost = Wafercost/ (total#chips* yield)

Wafercost (WC) and total#chips (n) are constants

So with yield 0.75 the yield = WC/n*15SEK
With yield y yield= WC/n*12 SEK

So:
y = 0.75*[(WC/n*12SEK)/ (WC/n*15SEK)] = 93.75%

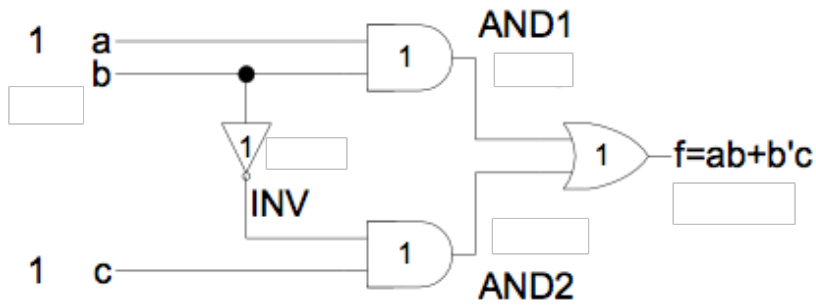
Question 7: (10 points)
Considering that the delay of a full adder (FA) is 1 ns, the setup time of a flip-flop is 0.1 ns, the hold time of a flip-flop is 0.01ns and the propagation time of a flip-flop is 0.1 ns. Find the latency, throughput and minimum clock period of the following 8-bit ripple carry adder designs:

a) Non-pipelined (1 stage of 8-bits)
b) Pipelined in 2 stages of 4-bits each
c) Pipelined in 4 stages of 2-bits each
d) Pipelined in 8 stages of 1-bits each

Answer:

a) 8 ns latency, 1 operation every 8 ns (125 MOPS), 8ns period
b) 2*(4+0.2)= 8.4ns latency, 1 operation every 4.2 ns (238 MOPS), 4.2ns period
c) 4*(2+0.2)= 8.8ns latency, 1 operation every 2.2 ns (454 MOPS), 2.2ns period
d) 8*(1+0.2)= 9.6ns latency, 1 operation every 1.2 ns (833 MOPS), 1.2ns period

Question 8: (10 points)
Find the hazard in the circuit below and fix it



Answer:

Lecture 19, slides 71-74

Question 9: (10 points)
Describe the following terms and explain what can be done to minimize their impact:
a) clock skew
b) metastability

Answer:
Lecture 18, slides 18-19 (+ avoid adding delays to the clock trees), 28-32

Question 10: (10 points)
Describe the push flow control and pull flow control interfaces using a timing diagram to show the data transfer between a sender and a receiver.

Answer:
Based on lecture 14 slide 37

END of EXAM