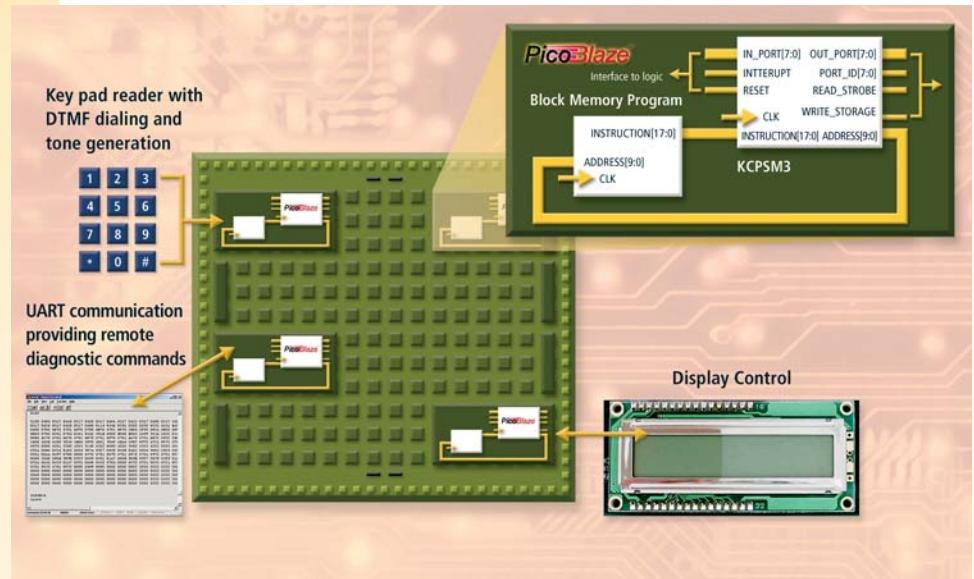


PicoBlaze™ 8-bit Microcontroller Reference Design for FPGAs and CPLDs

There are literally dozens of 8-bit microcontroller architectures and instruction sets. Modern FPGAs can efficiently implement practically any 8-bit microcontroller, and available FPGA soft cores support popular instruction sets such as the PIC, 8051, AVR, 6502, 8080, and Z80 microcontrollers.

The Xilinx PicoBlaze microcontroller is specifically designed and optimized for the Virtex and Spartan series of FPGAs and CoolRunner-II CPLDs.

The PicoBlaze solution consumes considerably less resources than comparable 8-bit microcontroller architectures. It is provided as a free, source-level VHDL file with royalty-free re-use within Xilinx FPGAs. Because it is delivered as VHDL source, the PicoBlaze microcontroller is immune to product obsolescence as the microcontroller can be retargeted to future generations of Xilinx FPGAs, exploiting future cost reductions and feature enhancements.



The Solution for Simple Processing

PicoBlaze is a compact, capable, and cost-effective fully embedded 8-bit RISC microcontroller core optimized for the Spartan™-3, Virtex™-II, Virtex-II Pro™ and Virtex-4 FPGAs and CoolRunner™-II CPLDs. The PicoBlaze solution delivers:

Free PicoBlaze Macro — The PicoBlaze microcontroller is delivered as synthesizable VHDL source code. As a result, the core is future-proof and can be migrated to future FPGA and CPLD architectures.

Easy-to-Use Assembler — The PicoBlaze assembler is provided as a simple DOS executable. The assembler will compile your program in less than 3 seconds and generate VHDL, Verilog and an M-file (for Xilinx System Generator) for defining the program within a block memory. Other development tools include a graphical integrated development environment (IDE), a graphical instruction set simulator (ISS) and VHDL source code and simulation models.

Powerful Performance — PicoBlaze delivers 44 to 100 million instructions per second (MIPS) depending on the target FPGA family and speed grade — many times faster than commercially available microcontroller devices.

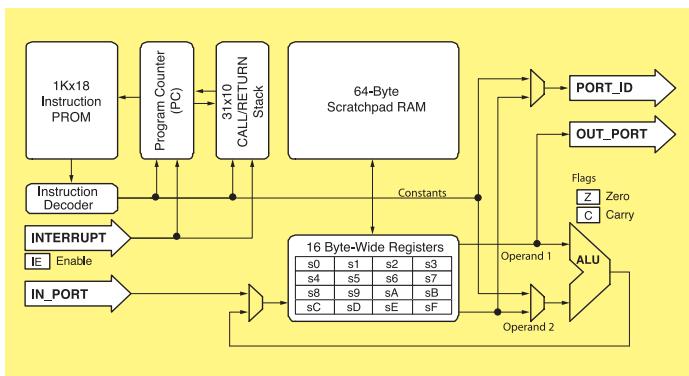
Minimal Logic Size — PicoBlaze occupies 192 logic cells, which represents just 5% of a Spartan-3 XC3S200 device. Because the core only consumes a small fraction of the FPGA and CPLD resources, many engineers can use multiple PicoBlaze devices for tackling larger tasks or simply keeping tasks isolated and predictable.

100% Embedded Capability — The PicoBlaze microcontroller core is totally embedded within the target FPGA or CPLD and requires no external resources. Its basic functionality is easily extended and enhanced by connecting additional logic to the microcontroller's input and output ports.

Key Feature Set*

- 16 byte-wide general-purpose data registers
- 1K instructions of programmable on-chip program store, automatically loaded during FPGA configuration
- Byte-wide Arithmetic Logic Unit (ALU) with CARRY and ZERO indicator flags
- 64-byte internal scratchpad RAM
- 256 input and 256 output ports for easy expansion and enhancement
- Automatic 31-location CALL/RETURN stack
- Predictable performance, always two clock cycles per instruction, up to 200 MHz or 100 MIPS in a Virtex-4™ FPGA and 88 MHz or 44 MIPS in a Spartan-3 FPGA
- Fast interrupt response; worst-case 5 clock cycles
- Assembler, instruction-set simulator support

PicoBlaze Block Diagram*



PicoBlaze Performance and Features Comparison

Feature	PicoBlaze for Spartan-3, Virtex-II/Pro and Virtex-4	PicoBlaze for Virtex-E and Spartan-II/E	PicoBlaze for CoolRunner-II
Program Space	1024	256	256
Instruction Size	18-bit	16-bit	16-bit
Internal Program	Yes	Yes	Yes
8-Bit Registers	16	16	8
Stack Depth	31	15	4
Assembler	KCPSM3	KCPSM	ASM
Size	96 Spartan-3 slices	76 Spartan-II/E slices	212 macrocells in XC2C256
Performance	44 MIPS (Spartan-3) 76 MIPS (Virtex-II) 100 MIPS (Virtex-II Pro) 100 MIPS (Virtex-4 LX, SX) 102 MIPS (Virtex-4 FX)	37 MIPS (Spartan-II/E)	21 MIPS

PicoBlaze Instruction Set*

Program Control	Logical	Arithmetic
JUMP aaa	LOAD sX,kk	ADD sX,kk
JUMP Z,aaa	AND sX,kk	ADDCY sX,kk
JUMP NZ,aaa	OR sX,kk	SUB sX,kk
JUMP C,aaa	XOR sX,kk	SUBCY sX,kk
JUMP NC,aaa	TEST sX,kk	COMPARE sX,kk
CALL aaa	LOAD sX,Y	ADD sX,sY
CALL Z,aaa	AND sX,sY	ADDCY sX,sY
CALL NZ,aaa	OR sX,sY	SUB sX,sY
CALL C,aaa	XOR sX,sY	SUBCY sX,sY
CALL NC,aaa	TEST sX,sY	COMPARE sX,sY
Shift and Rotate	Storage	
RETURN	FETCH sX,ss	
RETURN Z	FETCH sX,(sY)	
RETURN NZ	STORE sX,ss	
RETURN C	SRX sX	
RETURN NC	SRA sX	
RR sX	RR sX	
SL0 sX	SL0 sX	
SL1 sX	SL1 sX	
SLX sX	SLX sX	
SLA sX	SLA sX	
RL sX	RL sX	
		Interrupt
		RETURNI ENABLE
		RETURNI DISABLE
		ENABLE INTERRUPT
		DISABLE INTERRUPT
		All instructions execute in 2 clock cycles

Take the Next Step

Visit www.xilinx.com/picoblaze to download the free PicoBlaze microcontroller reference design, which includes the PicoBlaze VHDL source code, assembler, and related documentation.

*Based on PicoBlaze for Spartan-3, Virtex-II/Pro and Virtex-4 (KCPSM3).

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