Exam, Introduction to Electronic System Design (DAT091, DAT092, DAT093)

Tuesday Oct 28, 2014

Time and place: Tuesday Oct 28, 08:30, Hörsalsvägen

Examiner: Lars Svensson

Department: Computer Science and Engineering

Inquiries: Lars Svensson (ext. 1704); Sven Knutsson (ext. 5727) will visit the room at 9:30 and 11:30

Solutions: To be posted on Wed Oct 29, in PingPong

Results: To be posted on or before Sun Nov 16, in LADOK

Grading review: Room and time to be posted in PingPong

Grade limits:

3: 30–39 points; 4: 40–49 points, 5: 50– points

Extra grade points earned during the lab course (the 2014 installment) will be added to the exam result before computing the final grade.

Allowable references and utilities: English dictionary; no other books or papers.

General: Submit your solutions, ***in English***, on the blank paper sheets provided. Write legibly; feel free to use figures to get your point across.

Please do not combine solutions to several problems on the same sheet. Please order your sheets in sequence with the problems solved. Please write on only one side of each sheet.

In some problems, it may be necessary to make assumptions. When you do, state your assumptions explicitly and motivate them. Reasoning and descriptions can give partial credit even if the end result is incorrect.

The maximum points for each problem is given in parenthesis after the problem text.

Be sure to write your identification code on each sheet!

Good luck!

Problems

1. Consider the following VHDL code snippet:

```
ENTITY and_or IS
  PORT(a:STD_LOGIC;
       b:STD_LOGIC;
       c:IN STD_LOGIC;
       y1:OUT STD_LOGIC;
       y2:OUT STD_LOGIC);
END and_or;

ARCHITECTURE arch_and_or OF and_or IS
  SIGNAL x1:STD_LOGIC;
  SIGNAL x2:STD_LOGIC;
BEGIN
  x1 <= a AND b;
  y1 <= x1 OR c;
 proc1:
  PROCESS(a,b,c)
  BEGIN
    x2 <= a AND b;
    y2 <= x2 OR c;
  END PROCESS proc1;
END arch_and_or;
```

   (a) When the process has triggered, `a` and `c` are 1 and `b` is 0. What are the resulting values of `y1` and `y2`? (6p)

   (b) In VHDL, what is the difference between the operators `:=` and `<=`? (4p)

2. (a) Why do you need to keep track of characteristic impedances in PCB design? (2p)

   (b) How can you control the characteristic impedances in PCB design? (2p)

   (c) List at least three important criteria to consider when choosing a packaging option for a semiconductor chip. (6p)

3. (a) A technology implementation platform for electronic systems, in a broad sense, may be considered to comprise four parts. What are these? (4p)

   (b) The issue of device variability is of increasing importance in integrated-circuit design. Briefly describe three possible ways to manage the effects of such variability. (6p)

4. (a) Software benchmark suites do not always usefully predict the performance of a certain hardware/software combination. Give at least three possible reasons for such insufficiency. (6p)

   (b) The current trends for microprocessor design include a continued growth of the number of processor cores per chip. Describe the trends for clock frequency scaling and for power dissipation *per core*. (4p)

5. The lecture on power dissipation brought up several ways to manage and/or reduce dissipation at different points in the design process. Briefly describe up to five of these. You'll get two points per separate and well-enough described approach. (10p)

6. (a) The lecture on real-time systems (Risat Pathan) introduced the concept of *formal proof* of system real-time properties. Despite the reassuring term, some sources of uncertainty still remain. List two of those. (4p)

   (b) Intuitively, data conversion is perfect only when it is *lossless*—when an A-to-D-to-A conversion is an identity operation. No practical implementation fulfills such a condition, and approaching the ideal gets progressively more expensive. Describe at least three design parameters which influence the error/loss in data conversion; in each case, suggest why exaggerated parameter values may be expensive. (6p)

THE END