Exam, Introduction to Electronic System Design (DAT093)

Sat Oct 21, 2017

Time and place: Saturday Oct 21, 08:30, V building

Examiner: Lars Svensson

Department: Computer Science and Engineering

Inquiries: Lars Svensson (ext. 1704); will visit the room at 9:30 and at 11:30

Solutions: To be posted on Oct 23, in PingPong

Results: To be posted on or before Nov 9, 2017, in LADOK

Grading review: Room and time to be posted in PingPong

Grade limits:

3: 24–39 points; 4: 40–49 points, 5: 50– points

Extra grading points earned during the lab course (the 2017 installment) will be added to the exam result before computing the final grade.

Allowable references and utilities: English dictionary; no other books or papers.

General: Submit your solutions, ***in English***, on the blank paper sheets provided. Write legibly; feel free to use figures to get your point across.

Please write on only one side of each sheet. Please do not combine solutions to several problems on the same sheet. Please order your sheets in sequence with the problems solved.

In some problems, it may be necessary to make assumptions. When you do, state your assumptions explicitly and motivate them. Reasoning and descriptions can give partial credit even if the end result is incorrect.

The maximum points for each problem is given in parenthesis after the problem text.

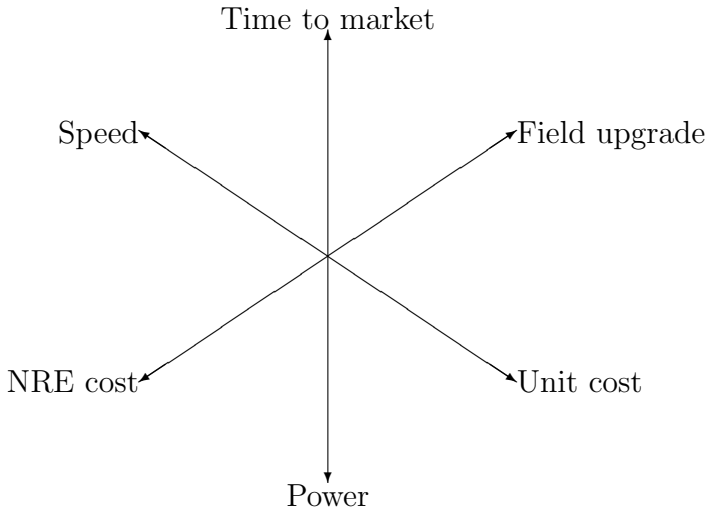
Be sure to write your identification code on each sheet!

Good luck!

Problems

Read through all problems before starting on the solutions.

1. (a) A diagram similar to the one below was shown in one of the lectures. Please *copy the diagram below to a numbered solution sheet* (you don't want your solution to be lost by mistake!) and mark approximate curves for an FPGA technology and an ASIC technology in the diagram. Use the "bigger is better" convention. (Note that the order of the axes has been changed with respect to the figure shown in the lecture.) (4p)



   (b) Under what cirumstances might it be a good idea to implement a special-purpose processor in an ASIC rather than just use a processor off the shelf? Please give one cost-driven example and one performance-driven example. (4p)

2. Benchmarking is frequently used in the design of microprocessor-based systems.

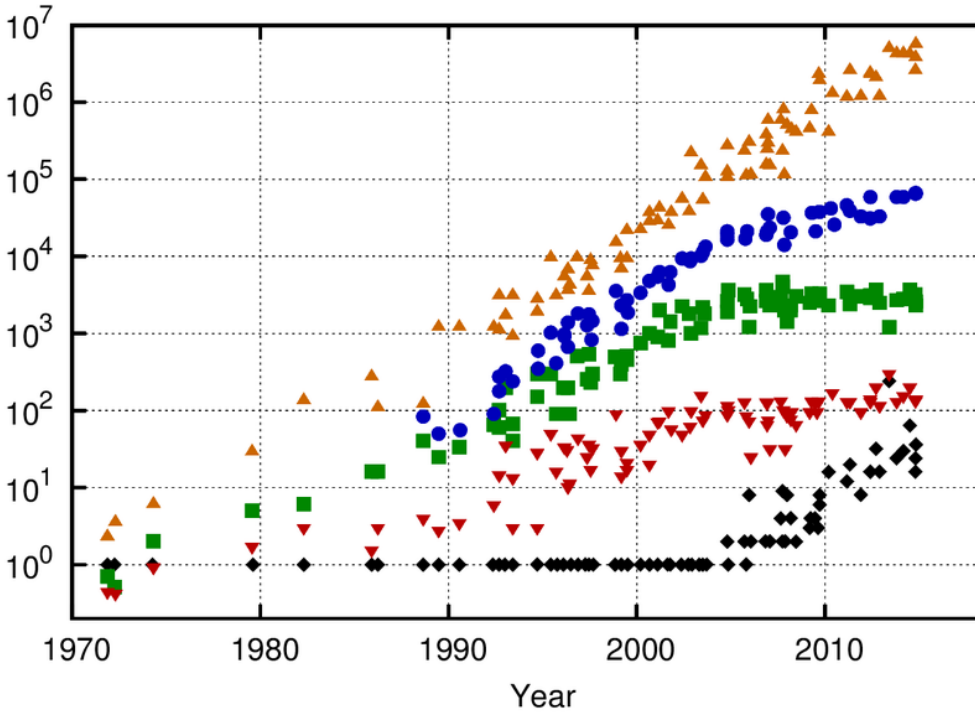
   (a) What is the benefit of using well-established benchmark suites to evaluate processor performance? Are there also potential drawbacks? If so, specify. (5p)

   (b) If you were to use special-purpose benchmark software to evaluate processor alternatives, what would be the important points to consider when choosing/creating the benchmark suite? (3p)

3. Functional specifications of the behavior of digital systems may often be captured in hardware description languages such as VHDL. Non-functional requirements may be just as important, but are handled outside the HDL formalisms. Briefly discuss *two* (not more) important non-functional requirements, and how each of these may influence *packaging* and *PCB design*. (8p)

4. System power dissipation may affect overall costs in a multitude of ways, many of which have been directly and indirectly referred to in the lectures. List up to eight of these, each with a sentence that explains the link. *Note:* you are not allowed to re-use answers from problem 3. (8p)

5. The following diagram was shown in the guest lecture on computer architecture:



The yellow, blue, green, red, and black markers show data on microprocessors over the past decades. The data shown are typical power (in watts); number of transistors (in thousands); clock frequency (in MHz); number of processor cores; and single-thread performance (in SpecINT $\times 10^3$). Note the logarithmic vertical axis!

Your task is to match the colors with the data types. You get 8 points if all pairs are correct; six points for three correct pairs; four points for two correct pairs; and two points for one correct pair. (8p)

6. (a) In discussion of design margins, what do the letters "PVT" signify? (2p)

   (b) How may CMOS device parameter variability increase *static* power dissipation compared to that of a hypothetical design with all-nominal parameters? (3p)

   (c) How may CMOS device parameter variability increase *dynamic* power dissipation compared to that of a hypothetical design with all-nominal parameters? (3p)

THE END