Exam solutions (DAT093)

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What follows are brief suggested answers/solutions. Other solutions than those listed here may be acceptable.

1. (a) *List three design parameters that will affect the cost of a "bare" PCB, that is, before adding the components.*

   Here are four: the PCB area, the number of layers of metal, the number of drilled holes (if any), and the substrate material.

   (b) *Compare and contrast through-hole mounting and surface mounting. When would you consider each of these alternatives?*

   Surface mounting can be considered the default, for reasons of size, packing density, and performance. Through-hole mounting may still be used for bulky, heavy, or high-power components, and for hand-built prototypes.

2. (a) *State the standard formula for dynamic power dissipation in CMOS circuits, and explain what the formula parameters mean.*

   $P_{dyn} = \alpha f C V^2$, where P_{dyn} is the dynamic power dissipation, V is the supply voltage (and also the voltage swing), C is the driven capacitance under consideration, f is the clock frequency, and α is the activity factor.

   (b) *Based on the formula you just gave, discuss how* **clock gating** *and a* **variable supply voltage** *may help reduce power dissipation. What extra design considerations arise when using these techniques?*

   Clock gating reduces α by eliminating clock transitions, and therefore other logic transitions, during cycles when the computed results would not not influence the overall computation. It is necessary to verify that the system behavior is identical with and without the clock; and clock tree balancing may require extra care.

   A variable supply voltage lets the system reduce the voltage V when the performance requirements allow it. Any clock signal frequency may have to be reduced commensurately in order to avoid setup violations; also it is necessary to verify functionality not at one, but several voltage levels.

3. (a) *The choice of technology platform is usually determined by a combination of several design requirements. Briefly discuss requirements that would cause you to consider an FPGA platform and an ASIC platform, respectively, and compare and contrast the two cases.*

   FPGA platforms are superior in terms of time-to-market, upgradeability, and NRE

cost. ASICs win on power, speed, and cost per part.

(b) *The ASIC/FPGA consideration need not be a strict either/or choice. Briefly discuss how the two technologies can be used to complement eachother in the same project.*

FPGAs may be used in prototypes and even in the first version of the product, since they allow for fast iterations and bug fixes within reasonable cost. Then, if production volumes motivate it, the FPGA may be replaced by an ASIC in the next version in order to reap the benefits of the low power dissipation and per-part cost.

4. (a) *How can pipelining help improve the performance of a microprocessor? May pipeline length be usefully extended indefinitely? Why or why not?*

A microprocessor pipeline improves performance by subdividing the work of each instruction into several parts, and by working on several instructions simultaneously. Its applicability is limited by circuit overheads per stage and by pipeline hazards.

(b) *The Tensilica "Xtensa" and Mentor "Catapult-C" design systems were discussed in class, and overview descriptions were included in the reading material for the course. Both these design systems make it possible to describe behavior in C or C++ rather than VHDL; but there is a major difference in how they approach the task. In what situations might each approach be preferable?*

The Xtensa system produces a special-purpose processor and a compiler to map a C++ program onto it. The Catapult-C system produces hardware directly from the C++ description. The Xtensa approach retains all the benefits of a software-defined behavior (flexibility, upgradeability, etc); the Catapult-C system should have the edge in terms of performance.

5. (a) *How do larger design margins contribute to the cost of a product?*

A simple way to increase design margins is to use slightly stricter design specifications than motivated by the system requirements; thus, the original overall requirements may be met even when specs are violated somewhat. This overdesign may result in more hardware (a manufacturing cost) and higher dissipation (an operational cost).

(b) *In the context of design margins, describe what each of the letters "PVT" means, and exemplify how you might reduce the necessary design margin associated with each letter.*

Process variations may be reduced during design by using regular layouts.

Voltage variations may be reduced by well-designed supply distribution networks and voltage regulators.

Temperature variations may be reduced by appropriate cooling arrangements (and in rare cases, such as high-precision oscillators, by temperature-controlled ovens).

(Remaining variability could be handled using *adaptive circuits* which increase their own supply voltage if performance slips too low.)

6. *For the challenges of* **reduced development time** *and* **increased power dissipation**, *discuss why each of them pose problems, and how the challenges may be met.*

A fast-moving globalized market increases pressures on development time: a missed market window may cost huge sums in missed revenue when prospective customers choose a

competitor's offering. Large product portfolios are therefore often built on *design platforms* which comprise hardware and software components which combine in several ways to deliver functionality and performance. (Think about a PC with alternative motherboard, CPU, PSU, graphics card etc, which can be combined in many ways.)

Higher performance requirements and often smaller physical size make both power delivery and heat removal more difficult. Opportunities for increased integration levels can be used to include circuits which are *specialized* for common tasks, and which therefore perform these tasks more efficiently than a general-purpose processor could.