On-chip Power Integrity Evaluation System

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Abstract—Power supply disturbance excited by simultaneous switching output (SSO) circuits or core circuits is a serious issue in a system-in-package (SIP), especially in 3D stacked die package, because much more I/O circuits and core circuits excited simultaneously in synchronized with clock edges than the case of single die package. Therefore, decoupling schemes in such SiP's must be carefully designed including on-chip capacitance as well as off-chip capacitance so as to reduce the impedance of power distribution network (PDN) as low as possible up to high frequency range. In this paper, an on-chip power integrity evaluation system has been established using a test chip with both noise generating circuits and monitoring circuits for on-chip power supply noise. On-chip power integrity has been examined and compared for the cases with and without on-chip capacitance and for the various embedded capacitors inside an interposer.

Keywords— On-chip Power Integrity; Power supply disturbance; system-in-package; power distribution network; interposer

I. INTRODUCTION

Power supply disturbance excited by simultaneous switching output (SSO) buffer circuits or core circuits is one of major sources of system instability and of electromagnetic radiation in the high-speed CMOS digital systems. Power integrity design has become a critical issue in a board, in a package, and even on an LSI chip [1]-[7].

Recently, various types of system-in-packages (SiP's) have been developing to make the form factor of overall system smaller. Decoupling schemes is more important to reduce larger noisy environments in SiP's, such stacked die packages, or 3D integrated dies, because much more I/O circuits and core circuits may switch simultaneously in synchronized with clock edges than the case of single die package. Power distribution network impedance (PDN) in SiP must be designed to be as low as possible up to GHz range and to avoid the parallel resonance due to chip-package parallel connection. Surface mount device (SMD) type capacitors are normally closely placed to LSIs to reduce the switching noise. However, the impedance profile of the conventional discrete decoupling capacitor is narrow band pass due to the equivalent series inductance (ESL) of the capacitor itself.

This paper reports an on-chip power integrity evaluation system, which has been established with a test chip fabricated by 130 nm CMOS process technology. Both noise generating circuits and on-chip noise monitoring circuits have been implemented in the test chip. Furthermore, MIM type on-chip decoupling capacitance has been implemented in a half of the core circuits. In addition, four types of interposers with different off-chip decoupling schemes has been fabricated to examine the effectiveness of off-chip capacitors.

II. TEST CHIP DESIGN

A test chip has been designed and fabricated in a CMOS 130 nm process with 7 metal layers. The chip size was 5 mm by 5 mm. The total number of pins was 224 pins. The block diagram of the chip is shown in **Fig.1.**

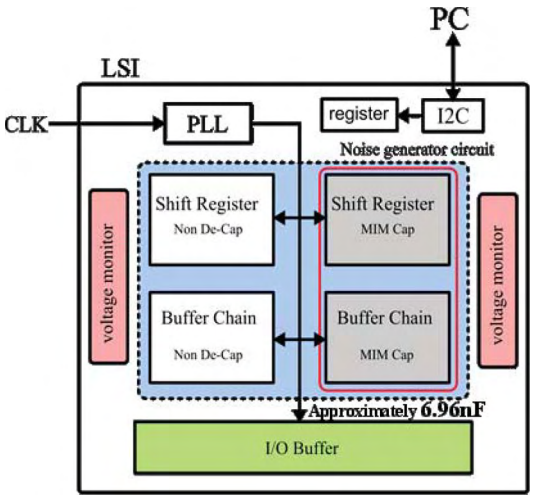


Fig.1 Block diagram of test chip

The key features of the test chip are as follows: 1) Core circuits and output buffer circuits were implemented as noise generating sources. 2) The current drivability of each output buffer was variable to 1mA, 2mA, 4mA, and 8mA by parallel connecting buffer element circuits. 3) The core circuits were separated into two parts. One was with intentional on-chip decoupling capacitance fabricated by a metal-insulator-metal (MIM) structure, and the other was without on-chip decoupling capacitance. A total intentional capacitance value was 6.96 nF for the half of the core circuits. 4) Each part consisted of shift resister circuits and buffer chain circuits. These circuits were activated by setting a register, which can be controlled by specific software on a PC. 5) Clock signal was applied from an external crystal oscillator, and the operating frequency can be changed by a PLL circuit to x1, x2, x4, and x8. 6) Built-in power noise monitoring circuits were implemented to observe real-time continuous power supply noises on various locations on a chip.

Fig.2 shows a layout image of the test chip. **Fig.3** shows the backside of the chip with a redistribution layer (RDL) to form the solder bumps for flip-chip connection to the package substrate. A total number of solder bumps was 225, which were arranged in an area array of 15 by 15.

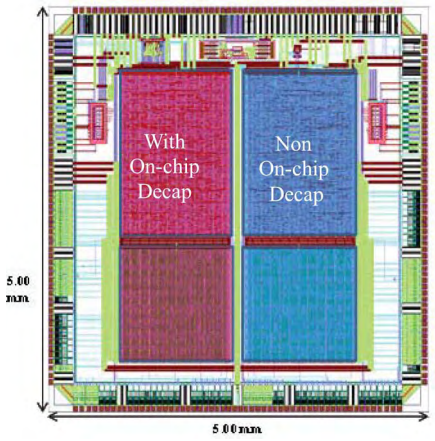


Fig.2 Layout image of CMOS test chip

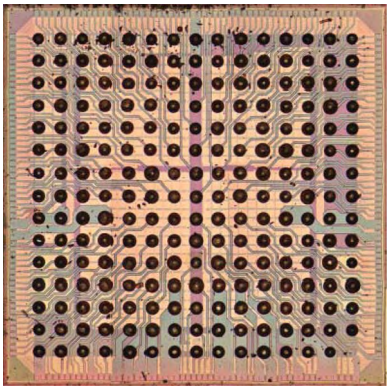


Fig.3 RDL of test chip

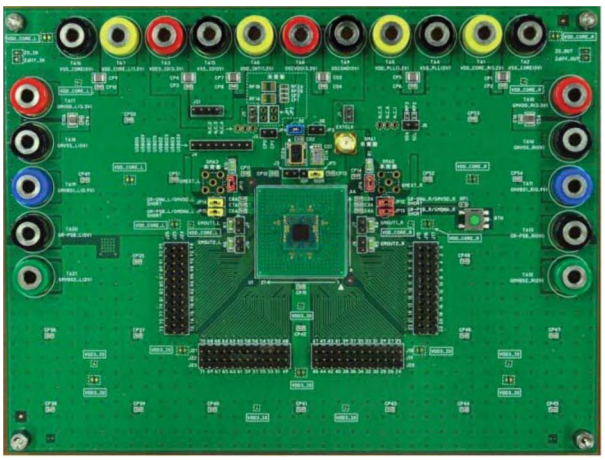


Fig.4 An evaluation board

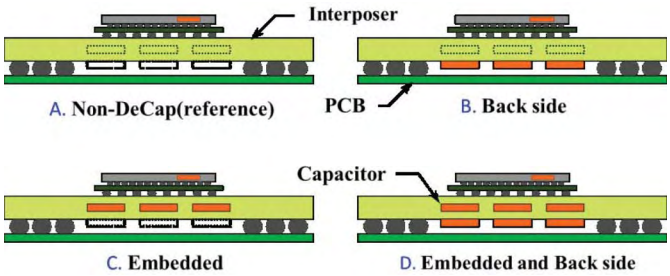


Fig.5 Four different placements of off-chip decoupling capacitors in the stacked interposer

III. STACKED INTERPOSERS & BOARD CONFIGURATION

Fig.4 shows an evaluation board to examine on-chip power integrity. The evaluation board consisted of 6 conductive layers, and the size of the board was 200 mm by 150 mm. The CMOS test chip was attached on a stacked organic interposer, which consisted of a small substrate and a large substrate. The test chip was flip-chip bonded to the small substrate with solder bumps in a pitch of 300 μm. The small substrate consisted of 8 conductive layers and its size was 12 mm by 12 mm. Then, the small substrate was connected to the large substrate with solder balls in a pitch of 600 μm. The large substrate consisted of 6 conductive layers and its size was 30 mm by 30 mm. Ball pitch was 1.27 mm.

The four types of stacked interposers were prepared as shown in **Fig.5**. First one was without any discrete SMD capacitors on the interposer. Second one was the case with SMD capacitors attached on the backside of the interposer. Third one was the case with SMD capacitors embedded inside the laminated core of the interposer. Fourth one was the combination of the backside capacitors and the embedded capacitors. The SMD capacitor was multilayer ceramic capacitors (MLCC) with a value of 0.1 μF. A total of 32 capacitors were implemented into the second and third interposer, respectively.

IV. MEASUREMENT METHOD

A. SSO noise monitoring

The noise waveforms excited by simultaneous switching output (SSO) buffers can be observed by a fixed high/low buffer method. By this method, either power line disturbance or ground line disturbance can be measured at the terminals of quiet output buffers by fixing the logic level of output buffer high or low, respectively, as shown in **Fig.6**. The SSO noise waveforms were measured by varying the current drivability of output buffers from 1mA, 2 mA, 4 mA, and 8 mA. Furthermore, the number of simultaneous switching buffers was changed from 4, 8, 16, 32, and 46. A pair of power/ground was arranged approximately for 8 output buffers in the test chip.

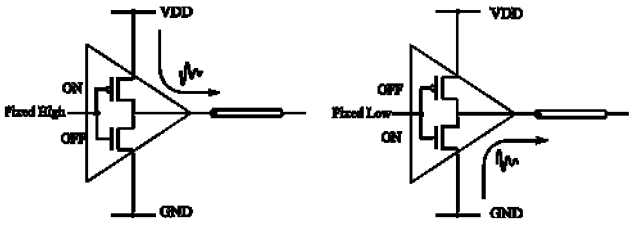


Fig.6 Fixed high/low buffer method

B. *Core noise monitoring*

Fig.7 shows a simplified equivalent circuit to observer on-chip power supply noise. The noise monitor circuit basically consisted of a source follower circuit [8]-[9]. This circuit has suitable properties with high input impedance, low output impedance, and its gain of unity. The output current of the source follower circuit was terminated by a resister of 50 ohms after the 50-ohm transmission line. **Fig.8** shows a measurement set up. The test chip was supplied by 3.3 V for I/O circuits, and 1.2 V for core circuits. The noise evaluation system was controlled by specific software installed on a personal computer. The output signal and power supply noises were measured with a real time oscilloscope (Agilent Infiniium 90000 series).

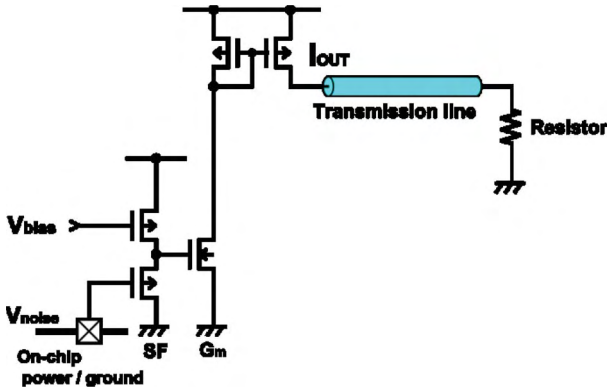


Fig.7 Noise monitoring basic circuit

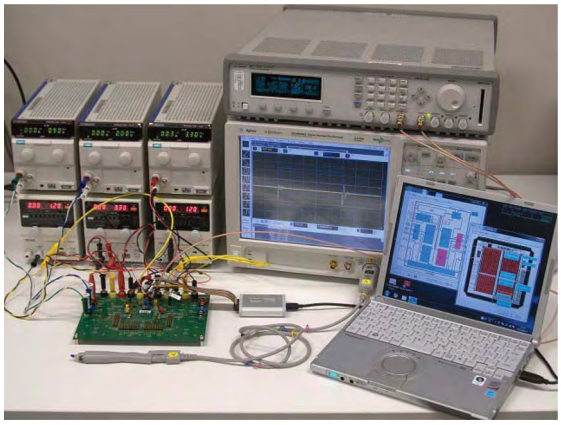


Fig.8 Measurement setup

V. MEASUREMENT RESULT

A. *SSO noise*

Fig.9 shows simultaneous switching noise when the number of switching buffers changed from 46 for the reference interposer substrate. The current drivability of output buffers was 2 mA. In this figure, the middle trace is a typical output signal waveform, upper traces are power bounces, and bottom traces are ground bounces. It is found that the peak-to-peak noise amplitude increased parabolically as the number of switching buffers.

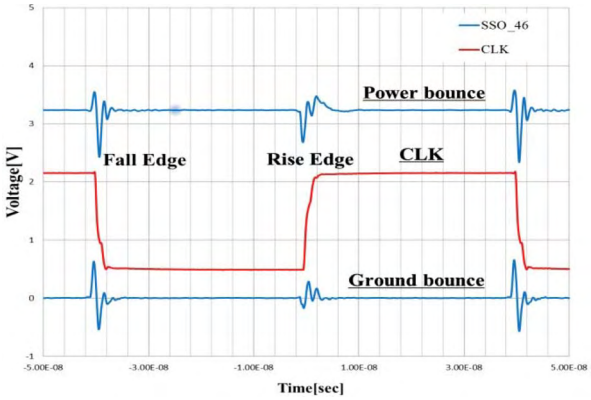


Fig.9 Measured switching noise waveforms

B. *Core noise*

Fig.10 shows power supply noise waveforms due to the core circuits without on-chip capacitance for the reference interposer using on-chip noise monitoring circuits. **Fig.11** shows the case with on-chip capacitance. From the measured data, noise reduction ratio of approximately 65 percent was observed for the rising edge, 57 percent reduction was observed for the falling edge.

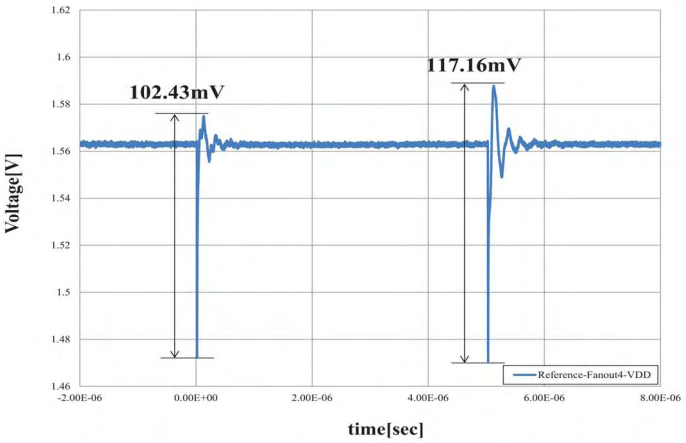


Fig.10 Power supply noise without on-chip capacitance

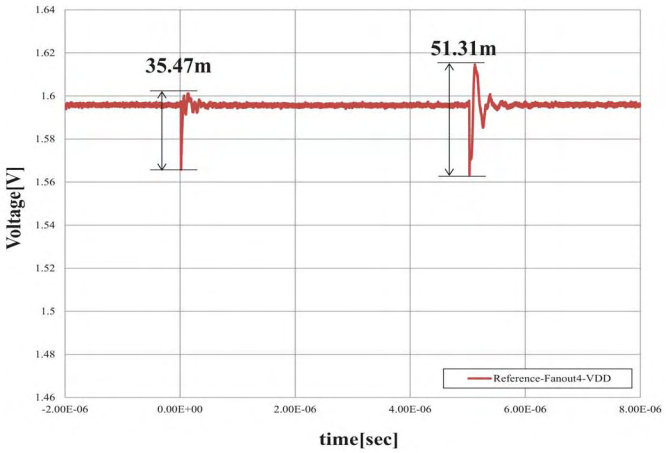


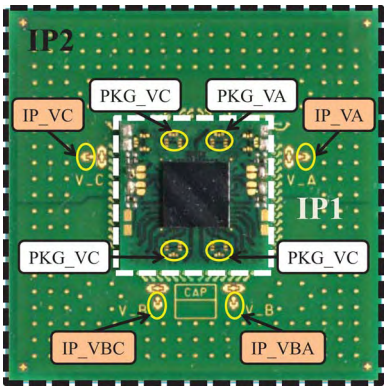
Fig.11 Power supply noise with on-chip capacitance

Compared with interposers with different placement and values of decoupling capacitors, an interposer with embedded capacitors showed approximately 68 percent reduction of power supply noise at the rising edge, and showed approximately 60 percent reduction of power supply noise at the falling edge.

VI. PDN IMPEDANCE MEASUREMENT AND SIMULATION

A. PDN impedance for stacked interposer

Fig.12 shows a stacked interposer consisted of 2 organic substrates. Several probing pads were placed to monitor the PDN impedance from the stacked interposer.



	Core power supply(Non Decap)	Core power supply (with On-chip Decap)
Interposer 1 (Chip side)	PKG_VA	PKG_VC
Interposer 2 (Board side)	IP_VA	IP_VC

Fig12 Probing pads on a stacked interposer

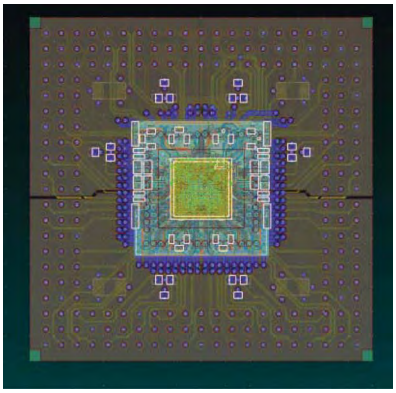
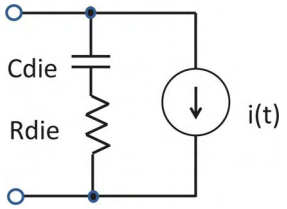


Fig13 CAD layout for stacked interposer

Fig.13 shows CAD layout for the stacked interposer. A 2D field solver (SIwave, Ansys Corp.) was used to obtain PDN impedance. Moreover, on-chip PDN impedance was calculated using a power supply analysis tool (Redhawk, Apache Design Solutions). The equivalent circuit model and its values, called CPM (Chip Power Model) were shown in **Fig.14**.



	Cdie (nF)	Rdie (Ω)
On-chip Dcap	7.075	1.392
On-chip Non-Dcap	4.366	1.729

Fig14 Equivalent circuit model of on-chip PDN

Fig.15 shows measured PDN impedances for the stacked interposer. The pad (PKG_VA) is corresponding to the power supply for core circuits without on-chip capacitance, while the pad (PKG_VC) is corresponding to the power supply for with on-chip capacitance. **Fig.16** shows simulated results.

From the measured PDN impedances for the reference interposer, equivalent value of capacitance can be estimated to be 3.18 nF for the case without on-chip capacitance, while equivalent value was estimated to be 7.96 nF for the case with on-chip capacitance. The measured capacitance value for with on-chip capacitance was almost same as the simulated one for with on-chip capacitance, while the measured capacitance value for without on-chip capacitance was relatively large contrary to our expectation. The equivalent value of resistance was approximately 1 ohm.

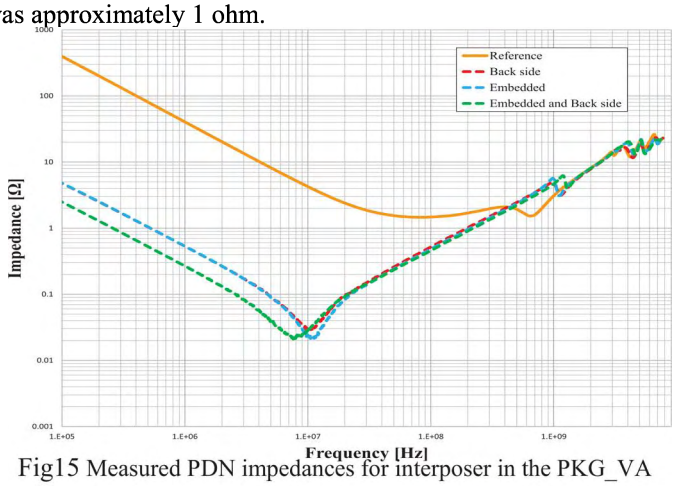


Fig15 Measured PDN impedances for interposer in the PKG_VA

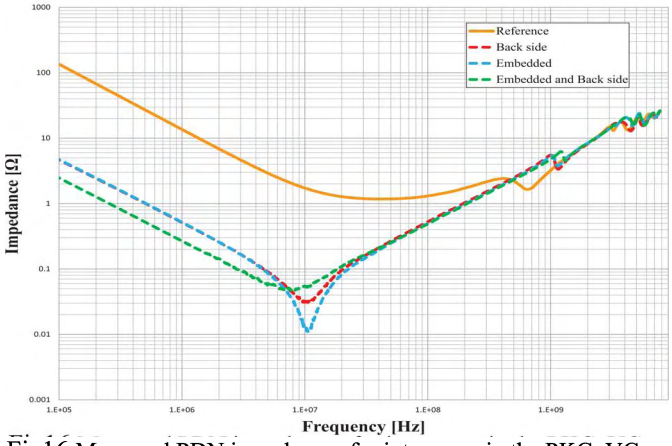


Fig16 Measured PDN impedances for interposer in the PKG_VC

B. PDN impedance for total evaluation board

Fig17 shows measured PDN impedances for the total evaluation board with the stacked interposer and the test chip probed at the pads (PKG_VA, IP_VA). **Fig.18** shows simulated PDN impedance for the total evaluation board probed at the same pads. A 2D field solver (SIwave) was also used to obtain the total PDN impedance. Eight SMD capacitors of 0.1μF and one titanium capacitor of 10 μF, which were mounted on the evaluation board were included in this simulation. From the data, measured value of total capacitance was ranged from 8.55 to 8.65 μF, while simulated result was 10.8 μF. From the both results, it has been found that anti-resonance peak due to chip-package resonance phenomenon occurred around 5 MHz.

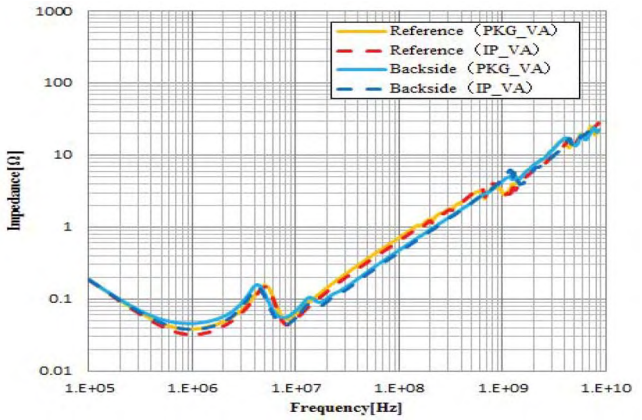


Fig 17 Measured PDN impedances for total board

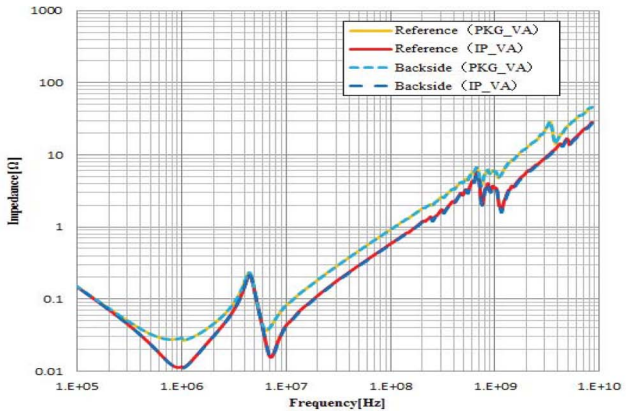


Fig 18 Simulated PDN impedances for total board

VII. SUMMARY

An on-chip power integrity evaluation system has been established by developing a 0.13 um CMOS test chip with both noise generating and monitoring circuits. Simultaneous switching noise due to I/O switching was measured by fixed-High/fixed-Low method. The reduction of power supply noise in core circuits for various combination of on-chip and off-chip decoupling capacitance has been examined by on-chip voltage monitoring circuits. Furthermore, simulated results of PDN impedances for the stacked interposer and the total evaluation board by using a field solver combined with a CPM model of the test chip showed a good agreement with measured results.

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