

Chapter 8

Signal Integrity Simulations

LEARNING OBJECTIVES

- Define common simulation terms, techniques, and tool types
- Review transient analysis techniques
- Learn fast convolution and statistical methods
- Review applications of quasistatic field solvers
- Review applications of three-dimensional finite element field solvers
- Show how numerical solution tools are used by Signal Integrity engineers to make decisions about high-speed circuit parameters

INTRODUCTION

The foundations of Signal Integrity stand upon solutions to Maxwell's equations. In *Maxwell's Equations*,¹ the mathematical meaning of the original equations was developed along with some definitions of what constituted quasistatic solutions within *good* conductors and dielectric materials. The propagation of electromagnetic waves was then studied in several media that were defined in terms of good, medium, and poor conductors, and characteristics of those waves were considered at the boundary between materials. In the current text, applications were studied in terms of common types of transmission lines, including those involved in the fabrication of printed circuit boards. Real-world materials were introduced after which analysis of propagation was conducted for complex dielectric materials and rough surfaces. The first Born approximation permitted an approximate solution to material features such as spherical snowballs on the surface, and theoretical calculations were made and compared with measurements with good correlation. A second-order Born approximation permitted us to consider effects of multiple scattering and absorption on realistic geometries, and a scale of magnitudes was developed to show how good

or poor assumptions were. The major feature of those calculations was to show how well the theoretical solutions compared with numerical solutions of Maxwell's equations using the same geometries. These results built confidence that the magnitude and phase of the numerical solutions checked with theory and measurement, but they also showed that the propagation velocity of waves in conductors was consistently predicted in terms of retarded scalar and vector potentials and dispersed waves.

Numerical solution software for Maxwell's equations is produced by several commercial and many individual research organizations. Industry tends to rely on software tools that are well documented and that are large enough to be used by suppliers and vendors. Some of the large companies that produce numerical solutions to Maxwell's equations or circuits that depend on them are Agilent of Santa Clara, CA, Ansoft of Pittsburgh, PA, CST of Framingham, MA, Sonnet of Syracuse, NY, and Synopsys of Mountain View, CA. Many of these companies produce a suite of tools for different Signal Integrity decision making. Each of the tools has its own strength and weaknesses, but, because the Ansoft tools permit one to describe electromagnetic fields inside conductors and because they provide a consistent suite of results that feeds successive tools, Ansoft tools are presented as examples in this chapter.

An important aspect of achieving quick success when designing electrical systems requires the utilization of simulation software and application of good engineering analysis techniques on the predicted data integrity at high speeds. This approach provides solutions using numerical analysis techniques to solve complex boundary condition problems that would otherwise be impractical. This chapter provides the reader with a general understanding of a suite of simulation tools used by signal integrity engineers that shows how different tools can provide pieces of a complete solution.

8.1 DEFINITION OF TERMS AND TECHNIQUES

Many types of simulation tools exist today, with applications ranging from slowly time-varying geothermal studies of global warming to thermodynamic studies of heat dissipation on spacecraft returning to Earth. Understanding and applying the specific tools and theory to solve signal integrity problems are a developing art because most of the effects occur at the speed of light in some medium. A core tool of the signal integrity engineer is the circuit simulator. Simulation program with integrated circuit emphasis (SPICE) transient techniques are often taught and discussed during the initial course work of an electrical engineer, but signal integrity engineers generally require more complex methods and algorithms than those initially learned from undergraduate studies. This is because several timing methodologies exist to determine if a system will work reliably at higher speeds. Open source SPICE software developed² at the University of California at Berkeley is often taught in undergraduate courses because it can be downloaded freely. The most common form of this software, PSpice, introduced in Chapter 3 section 3.7 is capable of handling alternating currents (AC) and transient pulses but was shown to have

limitations in attenuation and dispersion effects. The integrated circuit industry developed³ proprietary versions of SPICE and many others including HSPice by Synopsys in Mountain View, CA have developed analog and radio frequency (RF) circuit simulation design tools that address public domain Spice software limitations.

In the 1970s and 1980s, relatively slow-speed buses employed *common clocking* techniques that required data to be valid for a certain “setup” time prior to being “clocked” in; then the data were required to meet a “hold” time to ensure that the data were valid after they were clocked into the latch. Because of the timing and length limitations between “clk” and “data” associated with common clocking methodologies, *source synchronous* timings evolved for higher-speed buses (e.g., DDR3 = 1600 Mb/s). These buses generally make use of “pumping” techniques to achieve higher data rates with slower fundamental frequencies; that is, double-pumped data rates are twice the fundamental frequency and quad-pumped data rates are four times the fundamental frequency.

An “eye diagram” is a common way to show data created with a timing “strobe,” which requires data to meet a “time valid before,” t_{vb} , and a “time valid after,” t_{va} , period. The timing strobe is in an adjacent transmission line to that carrying the data so that data at any point can be said to be referenced to a local clock.

Other timing methodologies that are often used with high-speed differential signaling schemes exist such as forwarded, distributed, and embedded clocking. These methods utilize phased lock loop designs that generally multiply a slower-speed clock up to the fundamental operating frequency of the data and make use of silicon transistors to automatically center the clock in the data prior to latching it.

In Figure 8.1, several sequential **data voltage pulses** are plotted relative in time to two **clock strobe voltage pulses** and are all superimposed on one another by overlaying the voltage signals after a delay of integer multiples of the strobe clock period (called the **Unit Interval**, or **UI**). For the two **strobe pulses** shown in

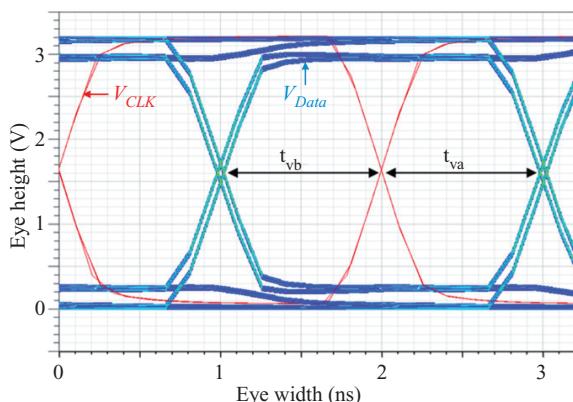


Figure 8.1 Depiction of source synchronous timing showing voltage data timing with respect to a strobe or clock voltage pulse.

Figure 8.1, the **data voltage** fell to zero some of the time but was slightly higher than zero at other times because of some irregular voltage source such as cross talk from other parts of the circuit. The data voltage pulses rose as high as 3.2V for part of the cycle and only to 3.0V for other parts of the cycle. The data pulses (light blue and dark blue) were not exactly in the same time phase with the strobe voltage pulses, as one rose slightly earlier than the other. If the rise and fall times are statistically variable (jitter in the timing) then we see the case of a two data voltage measurement in Figure 8.1. To achieve a more statistically significant set of results, we could superimpose additional voltage signals on the two-pulse set of Figure 8.1. With many such superimposed measurements, the width of the lines would overlap to such an extent that they would appear to be a blurred rising and falling set of some finite width, as shown in Figure 8.2. Here, the **clock strobe voltage pulses** of Figure 8.1 have been omitted. These so-called eye diagrams can be measured on an oscilloscope for real-world voltages on a high-speed circuit or simulated by using numerical analysis that incorporates cross talk and jitter from a complex circuit among its parameters. When more statistical data are superimposed in a plot like Figure 8.2, the width of the crossing points (~ 10 ps centered around 50 and 150ps) will grow, and the various low- and high-voltage blurred lines will get fatter; the eye is said to be closing in such cases. For the data shown in Figure 8.2, the gray diamond of width $\Delta UI = 0.50$ and height ΔEH (eye height) = 700 mV is a timing/voltage regime where the signal has not intruded for the set of measurements or simulations shown. Thus, any circuit decision (such as the trigger of a data count) made within this regime is certain to be reliable; that is, the data signal has integrity.

In Figure 8.2, a bit rate of 100ps is shown, and the UI is equivalent to the bit rate. A 0.5 UI results in an eye width of 50ps, as shown by the width of the gray diamond.⁴ The timing required for a reliable operating channel is 50ps in this example. In addition, for the receiver threshold, the EH is also specified to be between $EH_{upper} = 350$ mV and $EH_{lower} = -350$ mV, resulting in $\Delta EH = 700$ mV. Specification of the receiver parameters in this method is generally referred to as defining an eye mask. Eye masks are commonly specified at test point locations for both the transmitter and the receiver. Numerical simulations are employed to predict

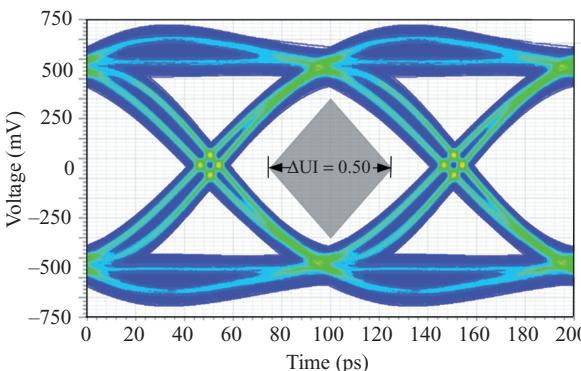


Figure 8.2 Unit interval plot where the eye width is $\Delta UI = 0.50$ with eye height between $EH_{min} = -350$ mV, and $EH_{max} = 350$ mV.

the eye width and EH, and measurements of a prototype board are then made to confirm or validate those predictions. Depending on the standard, the mask may or may not be specified for termination into a standardized load (say, 50Ω).

Another aspect of modern signaling includes the ability to understand information from the frequency domain. Commonly, bus standards specify channel loss, cross talk, phase lock loop bandwidth, and filter information using an s-parameter matrix where the maximum insertion loss (IL) or minimum return loss (RL) is specified at a given frequency (see Figures 6.24, 6.25, 6.26 as examples). Other less known derivations such as insertion loss deviation⁵ are sometimes specified to provide the reader with a deeper insight into the channels characteristics to ensure proper operation. These data are obtained through simulation and measurement and are then used in circuit simulators to determine if the system will pass a set of required margin specifications.

Historically, numerical analysis performed in the time domain used transient simulations, but, for higher-speed applications, inter-symbol interference (ISI) has become a dominant factor of the overall margin in an operating system. ISI analysis sometimes requires prohibitively long simulations into the million to billions of bits. The requirement has necessitated the need for simulation methodologies such as fast convolution and statistical techniques in lieu of repeated transient simulations because these types of simulations can quickly provide millions to billions bits of data to the user. These techniques make the assumption that the system is linear time invariant (LTI) because of the use of superposition and convolution and will be discussed in the next section.

One of the fundamental building blocks within the signal integrity engineer's simulation toolbox is the tabular transmission line, often referred to as the tabular *w*-element. The *w*-element quickly emulates the effects of loss in transmission line structures up to at least 30GHz.⁶ This element can reproduce the effects of frequency-dependent dielectrics and surface roughness and then be translated into a distributed network of passive resistor, inductor, conductor, and capacitor (RLGC) components, but the user of this technique must be warned that there is no physical basis for the *w*-element; it is a parameterization of the outcomes.

Initial modeling of the transmission line requires a two-dimensional (2-D) electrostatic field solver in which the transmission line geometry may be accurately described. Software tools such as Q3D ExtractorTM by Ansoft, a subsidiary of ANSYS, Inc. of Pittsburgh, PA incorporate a 2-D electrostatic field solver that can accurately extract RLGC parameters for transmission line structures and then generate the required "net list" for the tabular *w*-element that may be used in a SPICE sub-circuit model (Figure 8.3).

Real systems such as vias and connectors often include three-dimensional (3-D) geometries that cannot be modeled by using simple 1-D and 2-D techniques (Figure 8.4). For the electromagnetic interactions to be more accurately captured, a more complete physical geometry must be modeled. This requires the use of more complex simulation tools that model and numerically solve Maxwell's equations. Within industry and academia, the finite element method (FEM) has been proven to provide the robustness required to accurately predict the electromagnetic fields

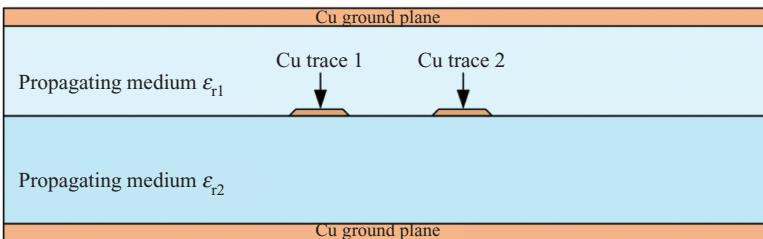


Figure 8.3 Example of differential stripline geometry drawn in Q3D™ employing a two-dimensional electrostatic field solver used for exporting to tabular w -element tools.

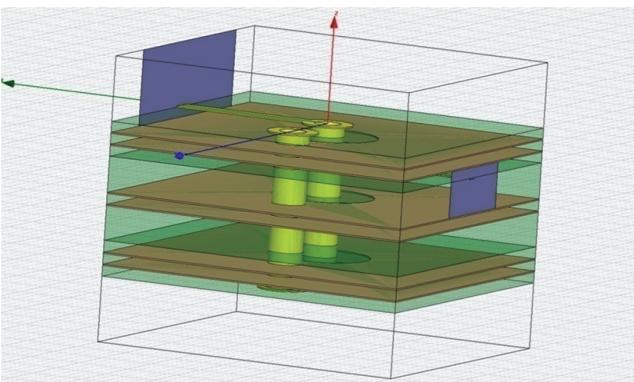


Figure 8.4 Example of signal and ground via in a multi-layer PWB drawn in HFSS™.

within arbitrary 3-D shapes primarily because of the tools' ability to mesh arbitrary shapes using tetrahedrons. High Frequency Structure Simulator (HFSS™, also by Ansoft, Inc.) uses the FEM technique along with an adaptive meshing algorithm, which automatically creates the required mesh based on several user inputs such as the frequency band of interest and the maximum deviation allowed between sweeps of s-parameters. Once solved, this information is generally exported as s-parameters by using the Touchstone⁷ file format developed by the Agilent Corporation of Santa Clara, CA to be used in circuit simulation.

Simulation tools that combine several modeling techniques are becoming more common within the signal integrity discipline. The primary motivation is to simulate complex structures that have large geometries compared with the wavelength (e.g., server board structures operating at 5–10 Gb/s). The resulting hybrid simulation tools have enabled simulation of entire printed wiring boards (PWBs) in an acceptable run time (less than 1 day). Typically, these types of simulation tools are utilized post layout and extracted into the simulation environment from computer aided drawings (CAD). Another interesting benefit of these hybrid simulation tools is the ability to analyze interactions between a system's signal integrity, power integrity, and electromagnetic compatibility/interference. Previously, these features were

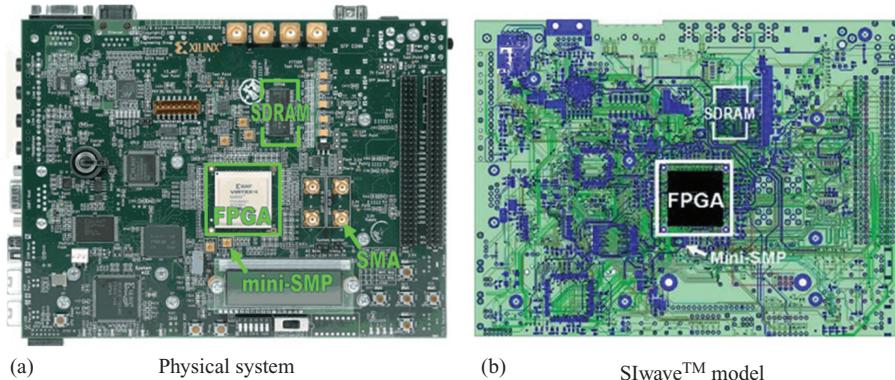


Figure 8.5 (a) Xilinx Virtex-4 FPGA physical test board; (b) extracted test board using the SIwave™ software hybrid simulation tool by Ansoft at Pittsburg, PA.

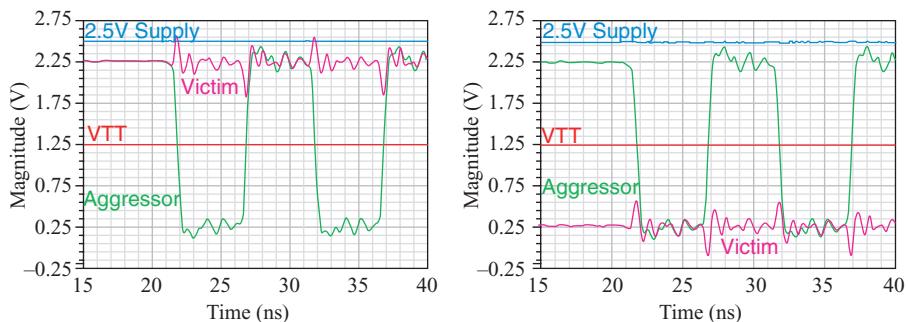


Figure 8.6 Circuit simulation showing the effects of simultaneous switching noise from a 32 bit SDRAM memory interface using the extracted hybrid model from SIwave™ within the Nexxim™ circuit simulation environment by Asoft Corporation of Pittsburg, PA.

analyzed independently, if at all. The hybrid results are often exported as SPICE “net lists” or Touchstone s-parameter files for use with circuit simulators. A common problem that necessitates this type of analysis occurs with memory applications where simultaneous switching noise is a problem caused by multiple drivers switching off the same power and ground sources at the same time. Noise is often introduced into the power delivery system that may have significant impact on timing margins and silicon reliability.

An example⁸ of the effects simultaneous switching output (SSO) noise can have on signals is shown below in Figures 8.5 and 8.6. This example shows the Xilinx, Inc. of San Jose, CA Virtex-4 FPGA test board and its extracted model using a hybrid simulation tool. The results of the 32-bit synchronous dynamic random access memory (SDRAM) interface show significant coupling from aggressors onto a victim signal and slight coupling onto a 2.5-V power supply. The extracted model was simulated in the time domain by using a circuit simulation tool.

Conclusion

Different modeling tools using 2-D, 3-D methods, and hybrid techniques provide the pieces required to perform parameterized system-level simulations within the time domain using a circuit simulator.

8.2 CIRCUIT SIMULATION

As discussed in sections 3.7 and 3.8, PSpice was developed by the Electronics Research Laboratory of the University of California at Berkeley and made available to the public in 1975.⁹ Donald O. Pederson could be called the father of SPICE¹⁰ because of his research and commitment that information in the public domain should be used by the engineering community. Many electrical engineering undergraduate programs require the usage of a SPICE simulator, while some use PSpice or Multisim created by the National Instruments Electronics Workbench group of Austin, TX, which have been available at no cost in student versions.

As described in section 8.1, eye diagrams are useful tools to help answer one of the fundamental questions of signal integrity: “If a sequence of ones and zeros is transmitted into a channel, separated in time by a specified UI, what are the chances of *correctly* detecting the data at a given point within the channel?” As mentioned above, an eye diagram takes the waveform generated at a selected location within the channel and overlays multiple copies of the data, each shifted in time by UI. A simple example of an eye diagram is shown in Figure 8.7 to demonstrate its usefulness. Here, a 50Ω , single-ended driver is feeding a 5.5-inch stripline (parameterized as a tabular w -element) on FR-4 with $\epsilon_r = 3.321$ and $\tan \delta = 0.0231$ at 1 GHz using a resistor capacitor (RC) load for the receiver with $R_{load} = 50\Omega$ and $C_{load} = 5\text{ pF}$, as was shown in section 3.8.

Fundamentally, the purpose of an eye diagram is to indicate the allowable window for reliably distinguishing bits from one another at the receiver end. There is a nonzero eye width required because receive jitter makes the time location of the bit imprecise, and setup and hold times also increase the width of the margin window. The required height of the window is usually specified by the noise margin

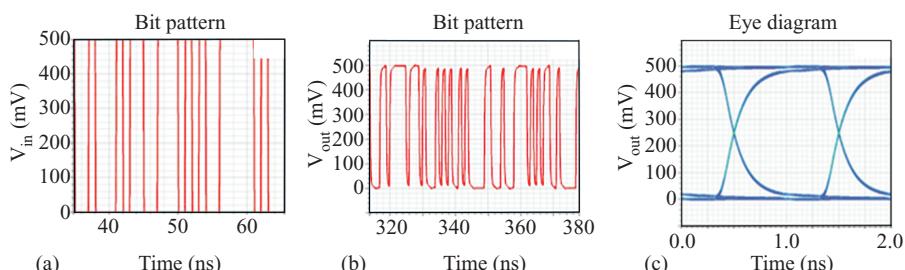


Figure 8.7 Creation of an “eye diagram”: (a) the input bit pattern, (b) the output bit pattern at the RC load, and (c) the eye diagram at the RC load.

of the receivers. The required width is often determined by the performance of clock data recovery, phase locked loop, and phase interpolator characteristics.

The number of times a waveform “violates” or crosses into a given margin window is an important metric because it predicts a signal logic error. This is the bit-error rate, or BER, which may be determined by

$$\text{BER} = \frac{\text{Number of Errors}}{\text{Number of Bits}} \quad (8.1)$$

Traditionally, eye diagrams were measured in the lab, or parametrically simulated in the way described above: The waveforms were overlaid with multiple time-shifted copies to form an output like that shown in Figure 8.2. However, as speeds increased, particularly in the case of high-speed serial links, the acceptable BER required a significant decrease (often to a level of 10^{-9} – 10^{-12}). This decrease, in turn, led to a great increase in the number of bits (10^9 – 10^{12}) that were needed to be simulated in order to predict the BER. Such lengthy transient simulations are impractical and have led to predictive techniques that rely upon the assumption of linear time invariance.¹¹

8.3 TRANSIENT SPICE SIMULATION

SPICE transient analysis combines traditional circuit analysis methods learned in undergraduate Electrical Engineering courses with microprocessors that have the ability to perform millions to billions of numeric calculations per second. This allows for an extremely accurate analysis of complicated nonlinear circuits that represent actual circuit behavior. A basic and brief overview of SPICE transient analysis is shown in the flow chart of Figure 8.8 to help the reader understand the differences and limitations between techniques such as fast convolution analysis, statistical transient analysis, and peak distortion analysis. Readers are referred to *Computer Design Aids for VLSI Circuits*¹² and *The Designer’s Guide to SPICE & SPECTRE*¹³ for a more in-depth discussion on SPICE analysis.

The first step to performing a SPICE transient analysis is the creation of the “net list” whether performed by means of a graphic user interface or by a text editor using the SPICE programming language.

The graphical creation of the schematic, Figure 8.9, produces a SPICE syntax “net list,” as described in section 3.7, that is then parsed to create a matrix of unknown equations, as shown in Figure 8.10.

After the SPICE “net list” is created, a direct current (DC) solution is computed. The “net list” is comprised of nonlinear differential equations assuming capacitor **currents**, and inductor **voltages** are zero (this is acceptable because the derivative of a constant is zero).

$$\textcolor{blue}{i}_L = L \frac{di(t)}{dt} \text{ and } \textcolor{red}{v}_C = C \frac{dv(t)}{dt} \quad (8.2)$$

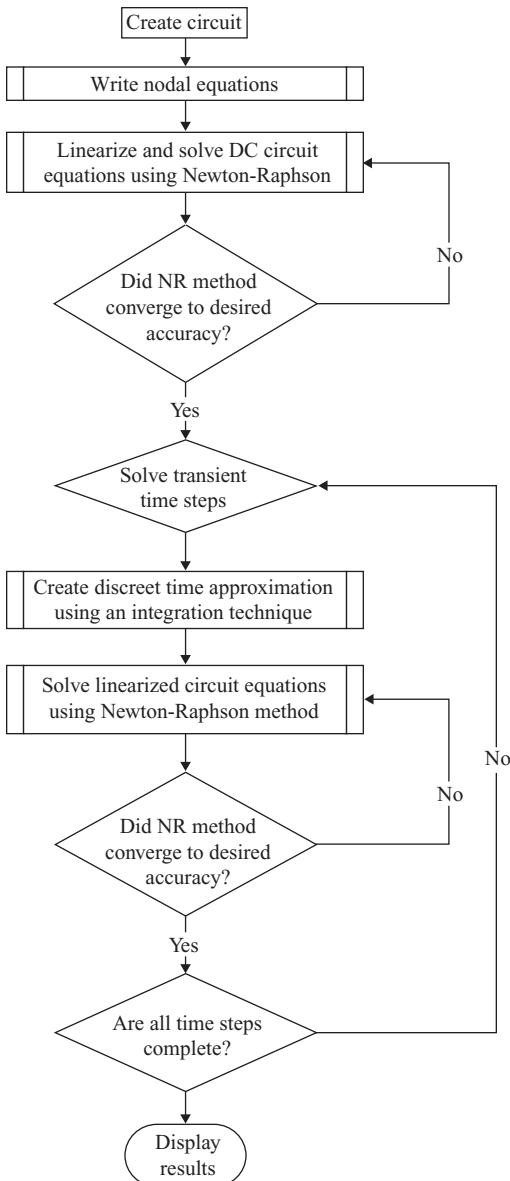


Figure 8.8 Flowchart detailing the steps required to produce transient analysis results.

The nonlinear differential nodal equations are discretized by using the Newton-Raphson (NR) method to form a series of linear algebraic equations that are generally solved by using a form of Gaussian elimination (GE). The NR method repeats itself until the convergence criteria set forth by the user are met and a DC operating point has been established.

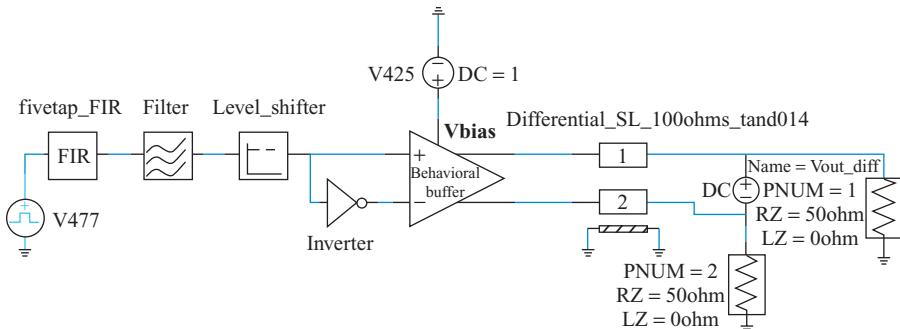


Figure 8.9 Graphical implementation of a high-speed serial driver using Ansoft's circuit simulator **Nexxim™**.

```
*****
*          Nexxim netlist
*          created by Ansoft Designer
*****
.option PARHIER='local'
.param $pre=0
.param $post1=0
.param $post2=0
.param $post3=0

* begin toplevel circuit
.global G_0

.inc E:\Program Files\Ansoft\Designer4\Examples\Nexxim Circuit\circuit_models.inc
.param UI=1.25e-010
.param trf=1.25e-011
.param pre_lvl=0
.param post1_lvl=0
.param post2_lvl=0
.param post3_lvl=0
.param Trise=1e-011
.param Tfall=1e-011
.param Period=1e-010

.inc "E:\Program Files\Ansoft\Designer4\Examples\Nexxim Circuit\SL_100ohms_tand014.sp"
.inc "E:\Program Files\Ansoft\Designer4\Examples\Nexxim Circuit\SL_85ohm_7v_6s.sp"

X410 net_9 net_0 "fivetap FIR" UI='UI' pre='$pre' post1='$_post1' post2='$_post2' post3='$_post3'
X411 net_0 net_4 "FILTER" transition_time='trf/UI' crf='1e-012 rtune='10*trf/UI/0.2'
X412 net_4 net_6 "LEVEL_SHIFTER" sumtaps='1 - (pre_lvl + post1_lvl + post2_lvl + post3_lvl)'
X414 net_6 net_47 "INVERTER"
V425 net_10 0 DC=1
V435 net_45 net_46 0 Port1 Port2 N=2 L=0.75 TABLEMODEL=Differential_SL_100ohms_tand014
X464 net_6 net_47 net_45 net_46 net_10 "CML_DRIVE" imax=0.02 Rtermmp=50 Rtermnn=50 ctermnn=7.5e-013 ctermmp=7.5e-013
V477 net_9 0 PULSE(0 1 0 'Trise' 'Tfall' 'Period/2 - Trise' 'Period')

RPort1 Port1 0 PORTNUM=1 RZ=50 IZ=0
.PORT Port1 0 1 RPort1
RPort2 Port2 0 PORTNUM=2 RZ=50 IZ=0
.PORT Port2 0 2 RPort2

* end toplevel circuit
.end
```

Figure 8.10 Top-level simulation program with integrated circuit emphasis (SPICE) “net list” for a schematic. Note that SPICE is a hierarchical programming language and the complete “net list” calls several subcircuit routines using the “x” call.

The initial conditions of a transient solution are generally taken from the DC solution computed in the previous step unless specifically provided by the user. Options are available to allow a user to input initial conditions; the reader is referred to Kundert¹³ for further discussion. The circuit equations must undergo a discreet time approximation to allow for a solution to the nodal equations. This is why a user selects the time step for the circuit simulator to aid it in evaluating the time domain derivative. Numerically integrating the differential equation is commonly referred to as the integration method. Several common numerical integration techniques may be utilized, while the most commonly implemented method is trapezoidal numerical integration.¹⁴ However, many practical circuits have parasitics that are decades apart in value. For instance, a common “net list” may include bypass capacitors that have a value of $0.1\text{ }\mu\text{F}$ but, at the same time, have silicon parasitic capacitances that are approximately 0.1 pF . The difference of six decades is referred to as a *stiff* problem. A stable method such as the backward difference formula, also referred to as Gear’s method,¹⁵ and the numerical differentiation formula¹⁶ are well suited for the integration of *stiff* differential equations by using a variable time step.

Once the discretized problem is created, all the nonlinear circuit elements must be linearized around an operating point by means of the NR method similar to that discussed for the DC solution. Then Gaussian elimination or a modified form called LU decomposition is performed to solve for the unknowns. The solutions are checked against the convergence criteria, and, if convergence is met, the solution is saved. The process repeats itself for all time steps until, finally, the complete solution is saved and displayed. It is important for the reader to understand that the intent of creating discretized linear elements is to ensure that traditional linear algebra techniques can be used to solve for the unknowns at multiple time steps.

8.4 EMERGING SPICE SIMULATION METHODS

Simulation methods that take advantage of linear time invariance (LTI) are becoming commonplace to create solutions for high-speed serial applications. These methods combine a single transient step or pulse response to determine the circuit’s system response by convolving an input bit pattern with the derivative of the step or pulse response. The assumption of a LTI system is used often in circuit theory because it greatly simplifies the mathematics and allows for quick answers that offer acceptable accuracy. Using superposition within a circuit allows for a large reduction in circuit simulation time. Many nonlinear and time-variant systems are approximated into simpler, special-case LTI systems for this purpose. The limits of these approximations in the case of some important, signal integrity-related circuitry will be discussed along with the tools used to analyze these circuits.

A linear system is one in which the output is a linear function of the input. In the time domain, this means that the signal at each point in time is multiplied by the same constant. In the frequency domain, it means that, for a given input at a certain

frequency, no other frequencies can be generated; the output frequencies are the same as the input frequencies, whose amplitudes may be different.

The limitations of a linear system can be illustrated by a simple example of a single amplifier, with a single sinusoidal frequency at the input. If the amplifier is operating linearly, the output will also be sinusoidal, with only a change in the amplitude. Once the amplifier reaches a certain maximum output voltage, the signal will start to “clip” in the time domain, which corresponds to the generation of frequencies at the output that did not exist at the input. Even though an amplifier almost always exhibits this behavior, the nonlinearities can be restricted in such a way as to make them insignificant.

A linear system possesses the property of superposition; in other words, the system possesses both the additive and homogeneity properties; that is, if

$$\begin{aligned} X_1(t) &\Rightarrow Y_1(t) \\ X_2(t) &\Rightarrow Y_2(t) \end{aligned} \tag{8.3}$$

then, by the additive property,

$$X_1(t) + X_2(t) \Rightarrow Y_1(t) + Y_2(t) \tag{8.4}$$

and by the homogeneity property, $aX_1(t) \Rightarrow aY_1(t)$, where a is a constant.¹⁷

A time-invariant system is one in which the output does not depend on the time, except for a shift or delay in time. In the time domain, the input is exactly recreated at the output, except for a shift in scale or time:

$$X_1(t - \tau) \Rightarrow Y_1(t - \tau), \tag{8.5}$$

where τ is constant.

8.5 FAST CONVOLUTION ANALYSIS

One emerging simulation method is fast convolution analysis. This technique performs a transient SPICE analysis for a step (rising and falling) or a pulse. The derivative of the transient response is then convolved with an input bit pattern to determine the system response. The principle of superposition is used with convolution to create the system response and requires the system to be LTI for accurate analysis (Figure 8.11).

This method provides a great savings in simulation time; a transient solution took 49 min and 30 s, while the fast transient analysis took 13.7 s. Strictly speaking, the entire system must be LTI in order to obtain an accurate analysis. However, Mellitz et al.¹¹ and Barnes et al.¹⁸ have shown that the assumption of linearity can be relaxed for differential buffers and receivers without a great loss of accuracy (Table 8.1).

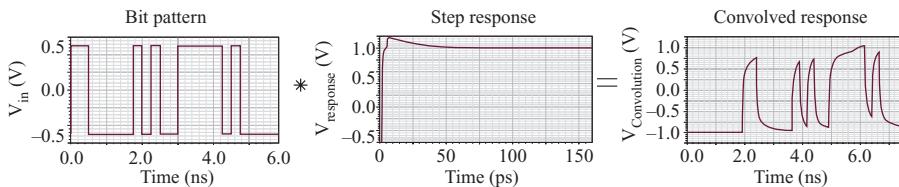


Figure 8.11 Fast transient analysis. The input bit pattern is convolved with the derivative of the step or pulse response of the system yielding the system response.

Table 8.1 Differences between fast convolution and transient solutions for a 12-inch transmission line with via transitions. The output resistances of each driver buffer leg is complementary and varies between $10\Omega \leq R_{out} \leq 90\Omega$

Trace characteristics	Transient	Fast transient	% Difference
Simulation time(s)	2970	13.7	198
Bits simulated	98,304	98,304	0
UI (ps)	125	125	0
Vdiff input swing	1	1	0
Eye level zero (mV)	-225	-217	3.86
Eye level one (mV)	205	210	-2.58
Eye amplitude	430	427	0.746
Eye height (mV)	369	369	0.076
Eye signal to noise ratio (SNR)	21.1	21.9	-4.12
Eye opening factor	0.942	0.954	-1.27
Eye width (ps)	108	110	-2.30
Eye P2P jitter (ps)	15.3	14.3	6.78
Eye root mean square (RMS) jitter (ps)	2.87	2.45	15.7
Eye rise time (ps)	46.0	45.85	0.392
Eye fall time (ps)	46.0	45.8	0.440

Another simulation technique uses statistical methods with a step or pulse response to determine the BER of the system. The concept behind statistical analysis is that, in order to generate an eye diagram and bathtub curve for a channel, including the effects of jitter, it is not necessary to run a long transient simulation, implied by the required BER of the channel. By combining the statistics of the bit stream with the variation in transitions caused by jitter, it is possible to generate the information needed with much less computation time.¹⁹

First, consider a particular point on the step response waveform described above. That point is the sum of all the voltage excursions caused by the various transitions from high to low or low to high at bit interfaces before the time point in question. This is where the statistical concept may be applied. Rather than calculate

the voltage excursions for all possible combinations of bits, a probability distribution may be calculated for the sum of all the excursions.

To explain this concept, consider this in terms of what are known as “cursors,” the deviations from the ideal waveform. If the channel were perfect, then the response would be identical to the input; the voltage at each point in time would be either +1 V or -1 V, depending on the bit in question.

Referring to Figure 8.7b, compare what the waveform would look like if there were a very large number of 1s in a row, versus a large number of 0s, followed by a transition to a 1. In the first case, the waveform would have time to settle to its correct final value of +1 V. In the second case, the waveform would be in transition from -1 V to +1 V because of imperfections in the channel. The difference between those two waveforms is a “cursor,” as shown in Figure 8.12.

ISI can now be calculated statistically. Assume that the current bit is a 1. This can happen in two different ways: either the previous bit was a 1, in which case there was no transition between them, or the previous bit was a 0, in which case there was a low-to-high transition between the bits. The probability of a transition is 0.5 if the bits are independent. In the first case, the cursor is 0; in the second case, it has some significant negative value corresponding to the slow rise time of the step response at the end of the channel. Statistically, therefore, the waveform has a 50% chance of having no deviation, and a 50% chance of a negative deviation, equal to the cursor value.

It is clear that this process may be performed both forward and backward, considering each “postcursor” and precursor in turn. The primary difficulty is that, even if the bits are independent, the transitions are not. A high-to-low transition cannot be followed by another high-to-low transition; there must be a low-to-high transition in between. However, this constraint can be handled by the appropriate application of conditional probabilities. The results are probability distribution

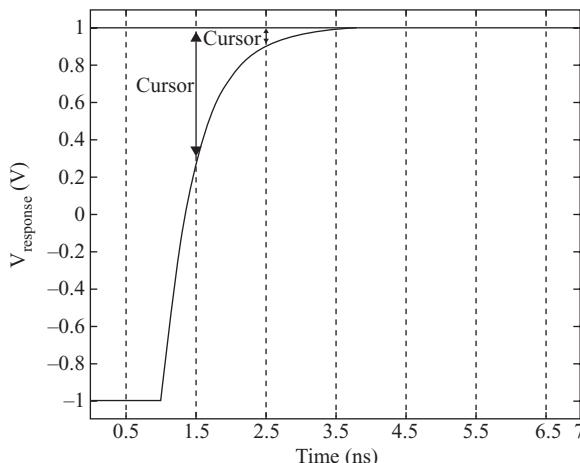


Figure 8.12 Determination of cursors from a rising edge of an RC circuit.

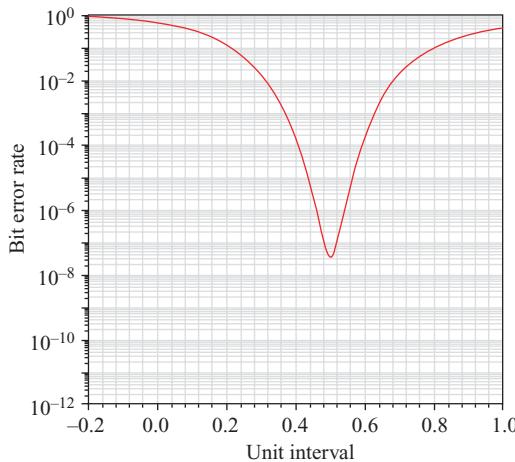


Figure 8.13 Bathtub curve showing bit error rate.

functions for the voltage value of the waveforms of high and low bits (see *Maxwell's Equations*, Appendix A). These functions can be combined into cumulative distribution functions, contours of which give the traditional eye diagram.

Another measure of the signal integrity of a channel is the so-called “bathtub curve” (Figure 8.13). This is a measure of the width of an eye opening at a certain voltage level, usually halfway between the high- and low-voltage levels. The bathtub curve turns out to be particularly easy to generate by using statistical methods: it is simply a slice through the cumulative distribution function determined above.

An advantage of the statistical technique is that the effects of random transmit jitter may be easily incorporated, without resorting to Monte Carlo methods. This is accomplished by the application of the Gaussian probability distribution function to the time location of each cursor. The cursors are, therefore, not just impulses in voltage but are spread out because of the Gaussian distribution in time, as shown in Figure 8.14.

The advantages of edge-based over pulse-based statistical eye calculations are primarily in two areas. First, by separating the rising and falling edges of the pulse, random jitter is truly random because the timing of the edges can be statistically independent. Additionally, effects of duty cycle distortion may be included, which can cause the width of pulse to vary. Another advantage is that the rising edge of a buffer can have different characteristics over that of a falling edge.

8.6 QUASI-STATIC FIELD SOLVERS

Another important type of signal integrity simulation tool is the class of quasistatic field solvers. These types of field solvers restrict the frequency of analysis to the regime of *good* conductors where charge redistribution is fast enough to neglect time

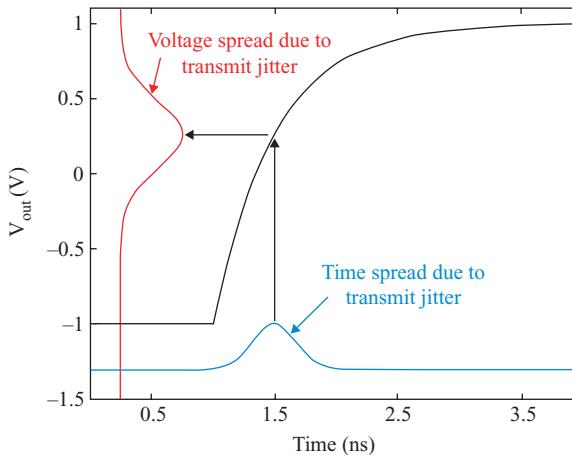


Figure 8.14 Pictorial representation of transmit random jitter smearing for statistical analysis.

derivatives of the electric field intensity so that $\vec{\nabla} \times \vec{E} \approx -\partial \vec{B} / \partial t$ and $\vec{\nabla} \times \vec{H} \approx \vec{J}$. In most of these applications, linear, isotropic media constitutive relations $\vec{D} = \epsilon \vec{E}$ and $\vec{B} = \mu \vec{H}$ are used. Quasistatic solutions are important tools to a signal integrity engineer because, when used properly, solutions are provided that yield 2-D and 3-D field solutions with minimal computer resources. Ansoft's Q3D ExtractorTM simulation tool consists of a quasistatic 2-D and 3-D field solver using a graphic user interface to create the geometries to be solved.

In order to create an electromagnetic field solution, Q3D ExtractorTM employs a combination of the FEM and the method of moments (MoM). In general, the FEM divides the full problem space into thousands of smaller regions and represents the field in each region (often referred to as an element) with a local function. The MoM divides up the surface of conductors and dielectrics into many triangles to represent the charges and currents on those surfaces. The choice of which method is used depends on the quantity being calculated. DC conductor problems use the FEM to model current flows within the conductors, while inductance and capacitance problems are solved by using the MoM.²⁰ Note that the simulation tool handles DC conduction problems along with AC conduction problems. Data rates in the multi-gigabit per second range may suffer because of the quasistatic nature of the 3-D field solver.

In addition to the visualization of the quasistatic electromagnetic fields, a SPICE representation of the circuit behavior may be created that can be solved by using circuit simulation techniques (Figure 8.15).

2-D quasi-static field solvers allow visualization of multiple conductors from within a PWB. They provide a means for creation of accurate RLGC matrices that can be used with circuit simulators. These RLGC matrices have the ability to create transmission line models that account for frequency-dependent effects such as dielectric dispersion and surface roughness losses, as covered in previous chapters.

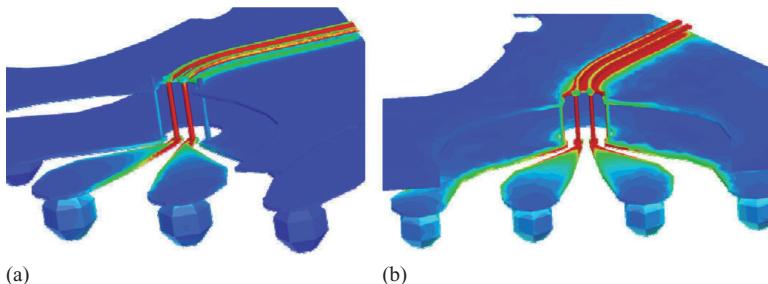


Figure 8.15 Q3D simulation by Ansoft of Pittsburg, PA of a differential pair within a ball grid array (BGA) package: (a) differential excitation of the pair; (b) single-ended excitation of each trace using ground as the return path.

These matrices are used in conjunction with the tabular w -element call that provides fast solutions to complex problems using circuit simulators. This type of simulation assumes a uniform cross section of the transmission line along its length; any discontinuities associated with bends, junctions and vias are not accounted for. This results in electric and magnetic fields lying in the x - y plane and not in the direction of propagation (z) except possibly for a small electric field component due to conductor losses in the direction of propagation.

In Figure 8.16, a sample stripline structure was created by using Ansoft's 2-D Extractor simulation tool that consisted of three differential pairs. Each differential pair was designed to have a characteristic impedance of 100 ohms, made out of FR-4. A simplistic rectangular model was drawn to show the overall effects of interaction between differential pairs. In this example, the dielectric height is 12 mils, with each trace width being 4.5 mils with an intrapair separation of 6.25 mils and interpair separation of 36 mils. Each conductor was excited with 1 A of current, with each conductor in the pair having a 180° phase difference to create a differential pair.

Conclusions from these field plots are as follows:

1. At both DC and 10GHz, the magnetic field does not interact with the other pairs (shown in B and C).
2. At DC, the magnetic field penetrates the conductors completely and penetrates into the ground planes (shown in D–K).
3. At 10GHz, the magnetic field crowds the edges of the conductors with no magnetic field in the center of the conductors (shown in L–S).
4. At 10GHz, it appears that there is an abrupt change in the magnetic field at the ground planes, but this is a result of the magnetic field barely penetrating the ground planes (top and bottom). The magnetic field is also distributed along the length of the ground plane (shown in L–S).

Similarly, the electric field may be plotted to gain an understanding for the behavior of the electric field intensity within the PWB (Figure 8.17).

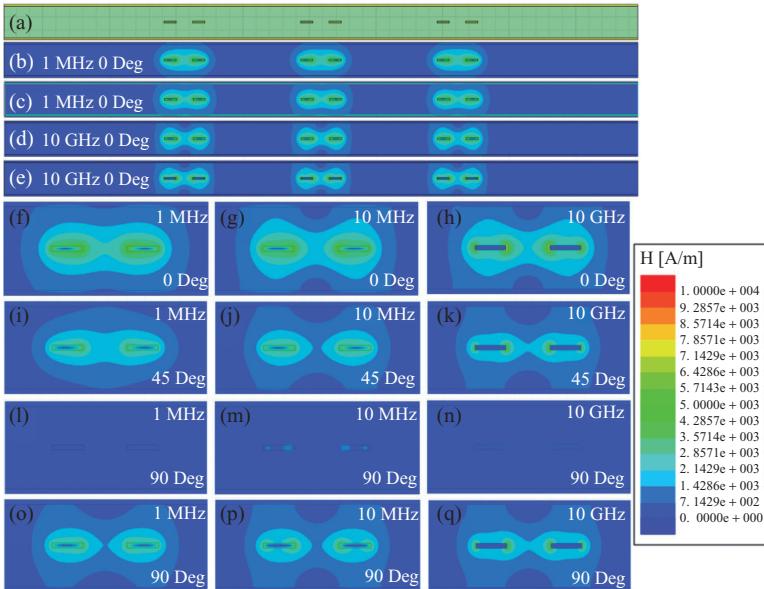


Figure 8.16 (a) Two-dimensional extractor model of three differential stripline pairs; (b) Magnetic field intensity at (DC) and 0° phase; (c) Magnetic field intensity at 10GHz and 0° phase; (d) DC and 0° phase; (e) DC and 22.5° phase; (f) DC and 45° phase; (g) DC and 67.5° phase; (h) DC and 90° phase; (i) DC and 112.5° phase; (j) DC and 135° phase; (k) DC and 157.5° phase; (d) 10GHz and 0° phase; (e) 10GHz and 22.5° phase; (f) 10GHz and 45° phase; (g) 10GHz and 67.5° phase; (h) 10GHz and 90° phase; (i) 10GHz and 112.5° phase; (j) 10GHz and 135° phase; (K) 10GHz and 157.5° phase.

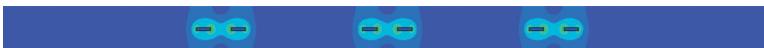


Figure 8.17 Electric field intensity plot of three differential pairs at 10GHz with a phase of 157.5° .

From the same simulation information such as the frequency dependence of inductance, resistance, capacitance, and characteristic impedance may be plotted. The simulation tool allows the user to define the geometric object using variables that can then be optimized automatically to allow convergence based upon the engineer's need.

Figure 8.18 shows some information available to a signal integrity engineer. It shows the transmission line characteristic impedance over the specified frequency range so matching networks that minimize reflections can be created. However, the curves show frequency dependency, thereby resulting in a causal model that will produce accurate time domain results. If any of the curves were constant across frequency (specifically the conductance matrix caused by the frequency-dependent dielectric losses), a noncausal model would be created that result in inaccurate simulations. This loss of accuracy becomes important above 1Gb/s.^{21,22,23} The characteristic impedance over frequency can be calculated by using

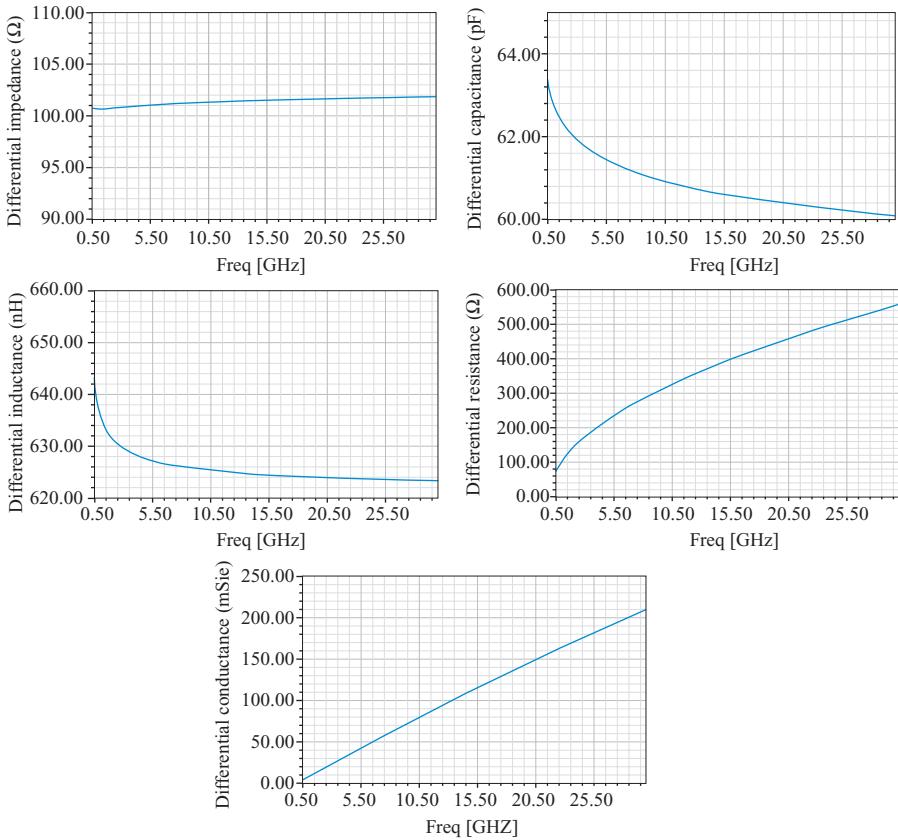


Figure 8.18 Plot of the victim's circuit parameter dependence over frequency.

$$Z_{0,odd} = Z_{0,odd1} + Z_{0,odd2} = \sqrt{\frac{R + j\omega L}{G + j\omega C}}_1 + \sqrt{\frac{R + j\omega L}{G + j\omega C}}_2 \quad (8.6)$$

This model does not account for any surface roughness attenuation. The loss of a real transmission line would thus be greater than that shown in Figure 8.19. A time domain pulse response for the tabular w -element described above is shown in Figure 8.19; notice that there are not causality issues at the launch of the waveform (the waveform starts at 0 V and returns to 0 V).

8.7 FULL-WAVE 3-D FEM FIELD SOLVERS

A characteristic of gigabit per second (and beyond) simulations is the modeling of discontinuities caused by 3-D geometries. One way to accurately capture the

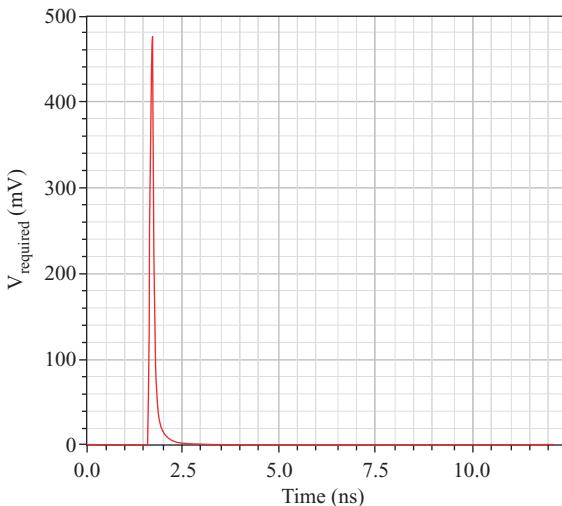


Figure 8.19 10 Gb/s pulse response to the tabular w-element shown in Figures 8.16 through 8.18. The length of the transmission line was set to 10 inches, with a rise time of 15 ps and a fall time of 15 ps.

effects of complicated 3-D structures is through the use of full-wave 3-D field solvers. This section will concentrate on a very specific type of simulator that uses the FEM to create electromagnetic models of arbitrary geometries. For an in-depth introduction to computational electromagnetics and the FEM, the reader is referred to *Computational Electromagnetics for RF and Microwave Engineering*.²⁴

Components that are commonly created in 3-D analysis for signal integrity are vias, connectors, and packages. These components are directly affected by the z -direction and therefore require more synthesis than can be obtained by using a one-dimensional or 2-D modeling approach. This section will focus on Ansoft's HFSS™. HFSS™ is not limited to solving signal integrity problems because the meshing algorithms may be applied to electromagnetic problems such as antennae designs, RF designs, and filter synthesis (Figure 8.20).

The basic operation is that a tetrahedral mesh that conforms to the arbitrary shape of the object to be modeled is created. Depending on the basis function used, Maxwell's equations are solved at the intersection of the tetrahedron, ensuring that the boundary conditions are satisfied. This means that the accuracy of the results is directly related to the mesh size and number of tetrahedron within the model.

The strength of HFSS™ is that the simulator will create an initial mesh that can be adaptively refined without the user having to guess what type of mesh will provide an accurate solution as shown in Figure 8.20. The adaptive mesh converges based upon the criteria set forth by the user. Generally, the convergence criteria are related to the maximum delta in the s-parameters because of successive mesh solutions.

Simulation of via structures is important in order to account for the interaction of the electromagnetic waves in the PWB. Several different solution types are avail-

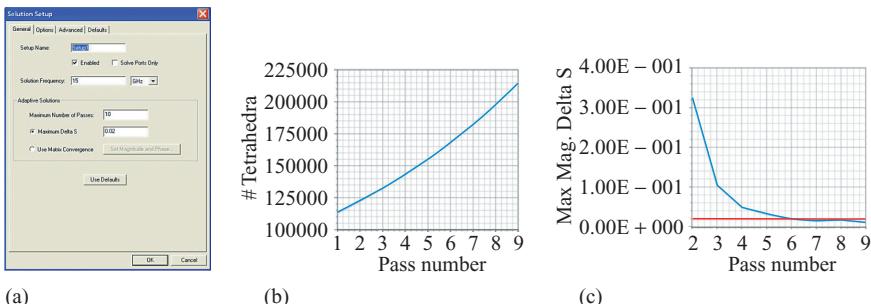


Figure 8.20 (a) Setup of users input for the adaptive mesh refinement process in HFSS™; (b) plot of the number of tetrahedron increases for each successive mesh refinement; (c) plot of the magnitude of delta s converges for successive mesh refinements.

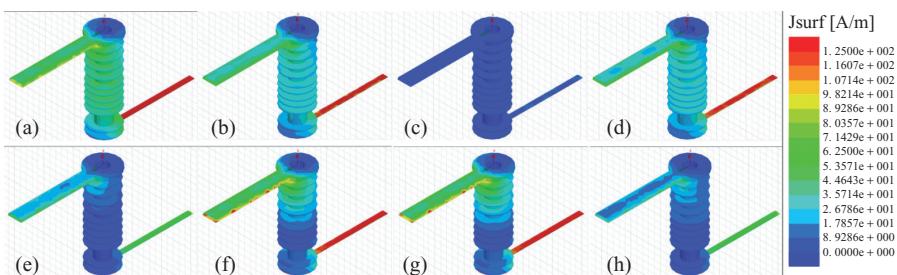


Figure 8.21 (a-d) Surface current on a simple via cross-section at 10 MHz with phase values of 0°, 45°, 90°, and 135°, respectively; (e-h) surface current on a simple via cross section at 1 GHz, with phase values of 0°, 45°, 90°, and 135°, respectively.

able, Driven Modal, Driven Terminal, and Eigenmode Analysis, along with two types of port solutions, Wave Port and Lumped Port; for tutorials on these terms see <http://www.ansoft.com/ots/utraining.cfm>. In order to see voltages and currents, a driven terminal solution is chosen in Figure 8.21. However, the selection of a port type is important as well. For non-TEM solutions such as a microstrip, a wave port will yield better solutions, assuming the port is set up correctly. However, wave ports are generally limited to an exterior face of the object that drives the need for lumped ports for interior analysis.

In order to determine if the wave port has been correctly set up, a “port only” solution should be run, which will allow the user to look at the electric field lines. The boundary of the wave port can be considered to be a perfect electrical conductor, which forces the any remaining electric fields tangential to the port edge. In order to ensure accurate simulations, the amount of energy forced by the port edges should be minimal (ideally zero). Shown in Figure 8.21 is a simple thru hole via model with 11 PWB layers. Each PWB layer is created by using a frequency-dependent FR-4 dielectric material with $\epsilon_r = 4.4$ and $\tan \delta = .02$ at 1 GHz.

For Figure 8.21, an analysis was performed from DC to 10GHz, looking at a simple via model. This model shows the surface current on the via barrel and microstrip sections. Notice the change in the distribution of surface current between 10MHz and 10GHz.

Another simple example, shown in Figure 8.22, is a differential via with two grounding vias offset by 20 mils to each side. This via design contains some large cavities within the PWB, which is common when filler material is needed to meet the common PWB thicknesses, for example, 0.225 in.

The traces start as microstrips and end as striplines coming out on layer 3. This leaves a very large via stub that can cause reflections that in turn cause discontinuities, as shown in Figure 8.23. The differential return loss and insertion loss show resonances occurring at 12.57, 27.25, 7.27, and 22.04GHz, respectively. Notice that, at DC, the return loss is zero, showing that the differential via exhibits an impedance of 100 ohms differential, but, as frequency increases, the matching becomes poor, causing large discontinuities for signals flowing through these via stubs. Resonances in the return loss yield better matching and lower insertion loss, which is favorable; however, the resonances in insertion loss yield additional attenuation of the output signal along with poor impedance matching.

Further investigation of the surface current provides insight to what is occurring within the via. At 1GHz, the insertion loss is less than -1 dB, with the return loss of around -14 dB and most of the current passes through the signal lines; however,

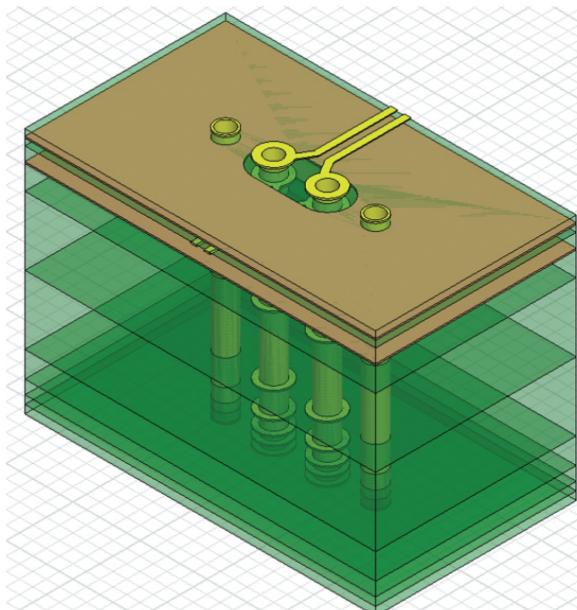


Figure 8.22 Differential via with grounding pins and 173.6 mil via stub.

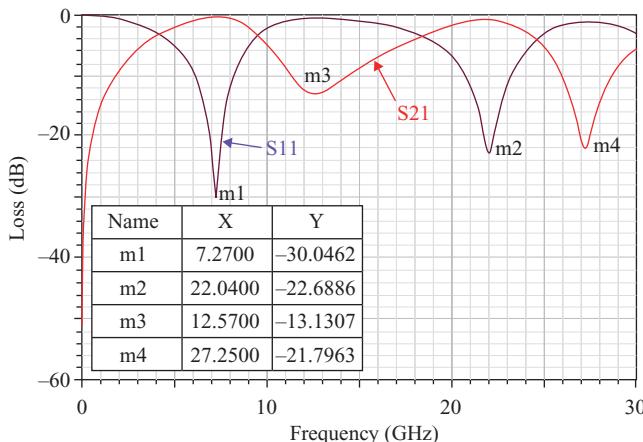


Figure 8.23 Differential return and insertion loss of a via designed to have a nominal differential impedance of 100 ohms.

at the 7.27-GHz resonance, the through signal is greatly attenuated by current dissipating in the barrel of the via stub. These effects are shown in Figure 8.24.

A topic that was not discussed here is the tools that allow importing of mechanical CAD drawings into the electrical modeling tools. This reduces the amount of work the electrical engineer has to do; however, modifications to the models will then have to be reflected into the mechanical drawings.

8.8 CONCLUSIONS

Chapter Conclusions

Simulation tools permit signal integrity engineers to design modern-day computers, personal electronics such as peak distortion analyses, cell phones, video game consoles, and even radar system electronics through the use of solutions to Maxwell's equations that cannot be handled with analytic theory. The theory developed in Chapters 1–7 has been applied to several examples with complex boundary conditions to exhibit some numerical tools that can be used to analyze high-speed electronic systems. Real-world systems have hundreds of buses that contain tens of thousands of nets in high-speed electronics. Without numerical solution techniques, engineers could not analyze the electrical currents and field intensities produced by high-speed electronic designs, and complex circuits as we know them today would not exist.

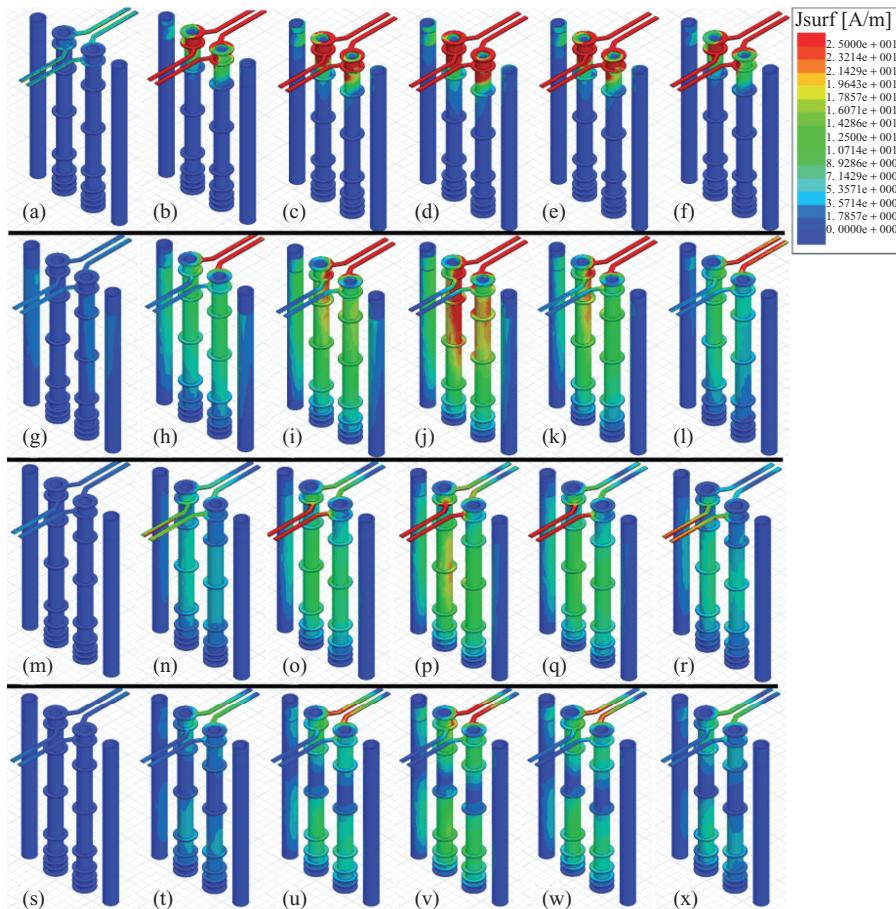


Figure 8.24 Differential via surface current plots: (a–f) Excitation at 1 GHz with phases of 0° , 22.5° , 45° , 90° , 135° , and 157.5° , respectively; (g–l) excitation at 7.27 GHz with phases of 0° , 22.5° , 45° , 90° , 135° , and 157.5° , respectively; (m–r) excitation at 12.57 GHz with phases of 0° , 22.5° , 45° , 90° , 135° , and 157.5° , respectively; (s–x) excitation at 22.04 GHz with phases of 0° , 22.5° , 45° , 90° , 135° , and 157.5° , respectively.

Book Conclusions

This book is not a how-to-use-simulations book and not a book for dummies. It assumes that the engineer has a good mathematical background and that he or she is able to learn complex subjects. The book is also not a rule-of-thumb book; rather, it provides the foundation about how those rules rest on a foundation described by *Maxwell's Equations*. It aims to provide a forefront engineer or physicists a means to evaluate and test emerging software that may make many (sometimes hidden) assumptions by comparing results to a solid theory based on analytical solutions

with simple boundary conditions. After confirming that the simulation tools correctly and causally predict a desired characteristic (such as time retardation or pulse dispersion), then the user may employ the tool with confidence that it will work with an extension of parameters or for more complex boundary conditions. Eventually, it is hoped that the software developers of the simulation tools will employ some of the analytic results described in this work (such as surface roughness) to permit even greater extensions to real-world applications.

ENDNOTES

1. Paul G. Huray, *Maxwell's Equations* (Hoboken, NJ: John Wiley & Sons, 2009).
2. L. W. Nagel and D. O. Pederson, *SPICE (Simulation Program with Integrated Circuit Emphasis)*, Memorandum No. ERL-M382, University of California, Berkeley, April 1973.
3. K. S. Kundert, *The Designer's Guide to SPICE and SPECTRE* (Boston: Kluwer Academic Publishers, 1998).
4. S. H. Hall, G. W. Hall, and J. A. McCall, *High-Speed Digital System Design: A Handbook of Interconnect Theory and Design Practices* (New York: John Wiley & Sons, 2000), 178–92.
5. S. Krooswyk, “Scattering Parameter Channel Analysis,” Master’s thesis, University of South Carolina, 2005.
6. S. H. Hall, S. G. Pytel, P. G. Huray, D. Hua, A. Moonshiram, G. Brist, and E. Sijercic, “Multi-GHz, Causal Transmission Line Modeling Methodology Using a 3-D Hemispherical Surface Roughness Approach,” *IEEE Transactions on Microwave Theory and Techniques* 55 (2007): 2614–24.
7. TouchStone® File Format Specification Rev. 2.0, Government Electronics and Information Technology Association (GEIA), 2008.
8. M. Brenneman and M. Alexander, “Power Integrity: IC, Package, and Board Co-Design,” in *Leading Insight, Ansoft Applications Workshop for High-Performance Design*, 2006. <http://www.ansoft.com/leadinginsight/pdf/High%20Performance%20SI-PI%20Design/Power%20Integrity-IC,%20Package,%20Board%20Co-Design-Xilinx.pdf>.
9. J. W. Nilsson and S. A. Riedel, *Introduction to PSpice® Manual for Electronic Circuits*, 6th ed. (Upper Saddle River, NJ: Prentice-Hall, 2002).
10. T. Perry, “Donald O. Pederson,” *IEEE Spectrum* 35 (1998): 22–27.
11. R. I. Mellitz, M. Tsuk, T. Donisi, and S. G. Pytel, “Strategies for Coping with Non-Time Invariant Behavior for High Speed Serial Buffer Modeling,” paper presented at DesignCon, February 4–8, 2008.
12. P. Antognetti, D. O. Pederson, and H. de Man, *Computer Design Aids for VLSI Circuits* (Boston: Martinus Nijhoff Publishers, 1984).
13. K. S. Kundert, *The Designer's Guide to SPICE & SPECTRE®* (Boston: Kluwer Academic Publishers, 1995).
14. R. L. Burden and J. D. Faires, *Numerical Analysis*, 7th ed. (Pacific Grove, CA: Brooks/Cole, 2001).
15. C. W. Gear, *Numerical Initial Value Problems in Ordinary Differential Equations* (Upper Saddle River, NJ: Prentice-Hall, 1971).
16. L. F. Shampine and M. W. Reichelt, “The Matlab ODE Suite,” *SIAM J. Sci. Comput.* 18, no. 1 (1997): 1–22.
17. A. V. Oppenheim, A. S. Willsky, with S. Hamid Nawab, *Signals and Systems*, 2nd ed. (Englewood Cliffs, NJ: Prentice-Hall, 1997).
18. G. Barnes, R. I. Mellitz, M. Tsuk, R. Holoboff, and S. G. Pytel, “Statistical and Transient Channel Modeling for Crosstalk, Bit Error, Jitter, and EMI,” *IEEE EMC Symposium on Electromagnetic Compatibility*, Detroit, MI, August 18–22, 2008, pp. 1–6.
19. A. Sanders, A. M. Resso, and J. D. Ambrosia, “Channel Compliance Testing Utilizing Novel Statistical Eye Methodology,” paper presented at DesignCon 2004, Santa Clara, CA (6).

20. Ansoft Corporation of Pittsburg, PA, http://www.ansoft.com/products/si/q3d_extractor/ Q3D Extractor® technical notes.
21. P. G. Huray, S. G. Pytel, R. I. Mellitz, and S. H. Hall, “Dispersion Effects from Induced Dipoles,” *10th Annual IEEE SPI Proceedings*, Berlin, May 9–12, 2006, pp. 213–16.
22. S. G. Pytel, G. Barnes, D. Hua, A. Moonshiram, G. Brist, R. I. Mellitz, S. H. Hall, and P. G. Huray, “Dielectric Modeling and Characterization up to 40 GHz,” *11th Annual IEEE SPI Proceedings*, Portofino, Italy, May 13–66, 2007.
23. P. G. Huray, F. Popoola, S. G. Pytel, R. I. Mellitz, D. Hua, and S. H. Hall, “Response Function from Induced Dipoles above 10 GHz,” paper presented at the IEEE SoutheastCon 2007, Richmond, VA, March 22–5, 2007.
24. D. B. Davidson, *Computational Electromagnetics for RF and Microwave Engineering* (Cambridge: Cambridge University Press, 2005).