

DAT110 ALU

0.1

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Chapter 1

Design Unit Index

1.1 Design Unit List

Here is a list of all design unit members with links to the Entities they belong to:

entity ALU	5
architecture rtl	6

Chapter 2

File Index

2.1 File List

Here is a list of all documented files with brief descriptions:

alu.vhd	32-bit ALU	7
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Chapter 3

Class Documentation

3.1 ALU Entity Reference

Entities

- [rtl](#) architecture

Libraries

- [ieee](#)

Use Clauses

- [std_logic_1164](#)

Ports

- [Clk](#) in **std_logic**
System clock.
- [Reset_n](#) in **std_logic**
Active low synchronous(?) reset.
- [A](#) in **std_logic_vector(31 downto 0)**
Input A.
- [B](#) in **std_logic_vector(31 downto 0)**
Input B.
- [Op](#) in **std_logic_vector(3 downto 0)**
Operation select signal.
- [Outs](#) out **std_logic_vector(31 downto 0)**
Output.

3.1.1 Member Data Documentation

3.1.1.1 `ieee` [Library]

Uses the following instruction opcodes (aliases):

- 0000: add A+B (signed)
- 0001: add A+B (unsigned)
- 0010: sub A-B (signed)
- 0011: sub A-B (unsigned)
- 0100: bitwise OR
- 0101: bitwise AND
- 0110: bitwise XOR
- 0111: bitwise NOR
- 1000: shift left
- 1010: shift right (logical)
- 1011: shift right (arithmetical, signed)
- 1110: SLT (Set on Less Than)
- 1111: SLTU (Set on Less Than Unsigned)

3.1.1.2 `std_logic_1164` [Package]

Authors: John William Croft

The documentation for this class was generated from the following file:

- [alu.vhd](#)

3.2 rtl Architecture Reference

The documentation for this class was generated from the following file:

- [alu.vhd](#)

Chapter 4

File Documentation

4.1 alu.vhd File Reference

32-bit [ALU](#)

Entities

- [ALU](#) entity
- [rtl](#) architecture

4.1.1 Detailed Description

32-bit [ALU](#)

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