Digital assist / enhancement for ADCs and DACs

DAT116, Dec 20 2018

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Recap slide

E_{ADC} vs E_{NAND}

SNDR (dB)	E_{ADC}	E_{ADC} / E_{NAND}
30	21 nJ	4700
50	168 nJ	38000
70	1.35 uJ	300000
90	10.8 uJ	2400000

- Complete ADC energy per conversion (in 2008) vs energy of one NAND-gate logic transition in 90-nm CMOS
- Digital logic more “affordable” for higher resolutions!
  - Even more in newer technologies
- Increasingly attractive to use digital methods to improve performance!

[Murmann, CICC 2008]

Assist? Enhancement?

- Techniques that rely on more-or-less complex digital techniques to improve converter performance
  - Every sample and/or on average
- Calibration
  - Redundant pipelined ADCs
  - Interleaved ADCs
  - Dynamic element balancing in DACs
  - ∑Δ ADCs, DACs

Improving every sample

Calibration

- Adjust “translation table” from analog to digital data (or conversely) to reduce errors
  - Main focus typically on INL errors
    - Large-scale errors cancelled using a few polynomial coefficients
- Two main categories of calibration:
  - Foreground / offline
  - Background / online

Foreground calibration

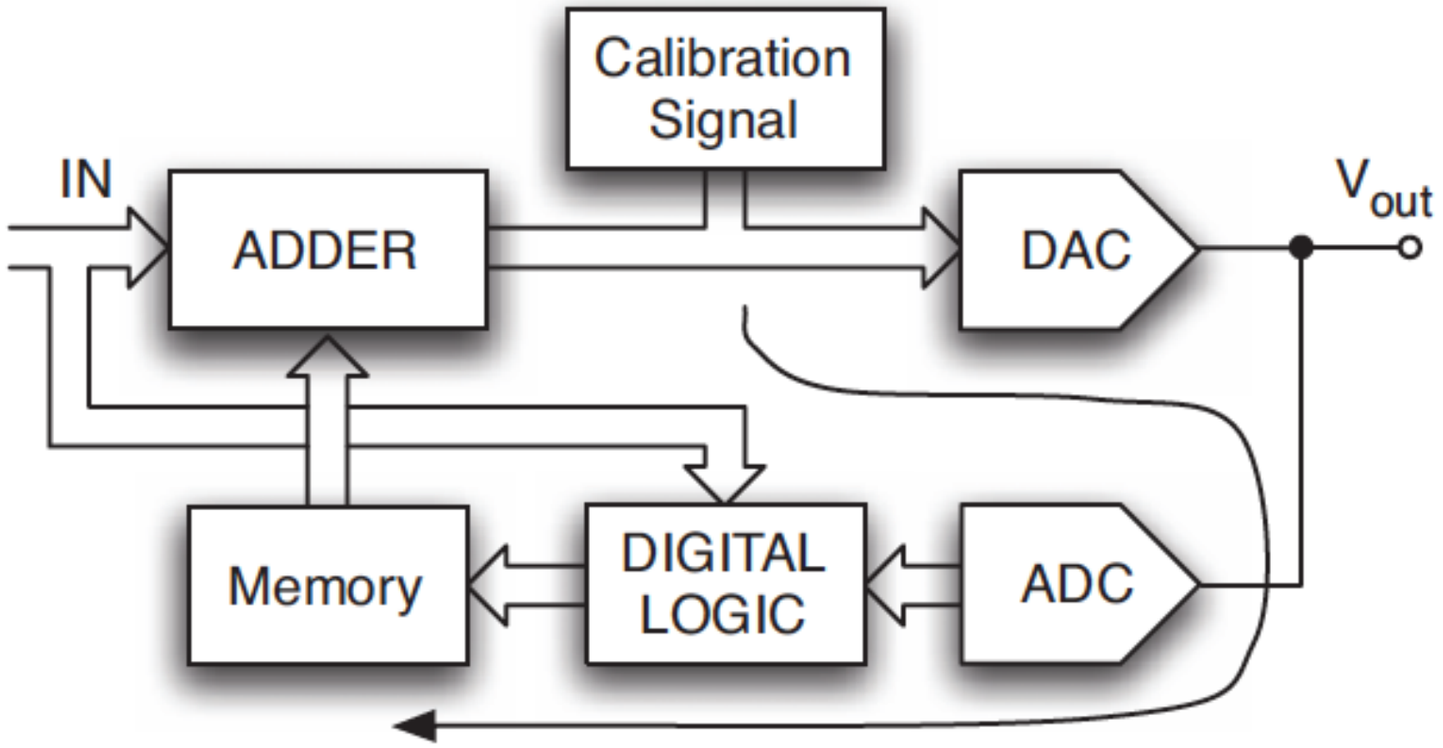


Figure 8.6. Conceptual scheme of a foreground calibrated DAC.

- Apply known calibration signal as input
- Observe output, compare with expected value
- Adjust “on digital side”

Background ADC calibration

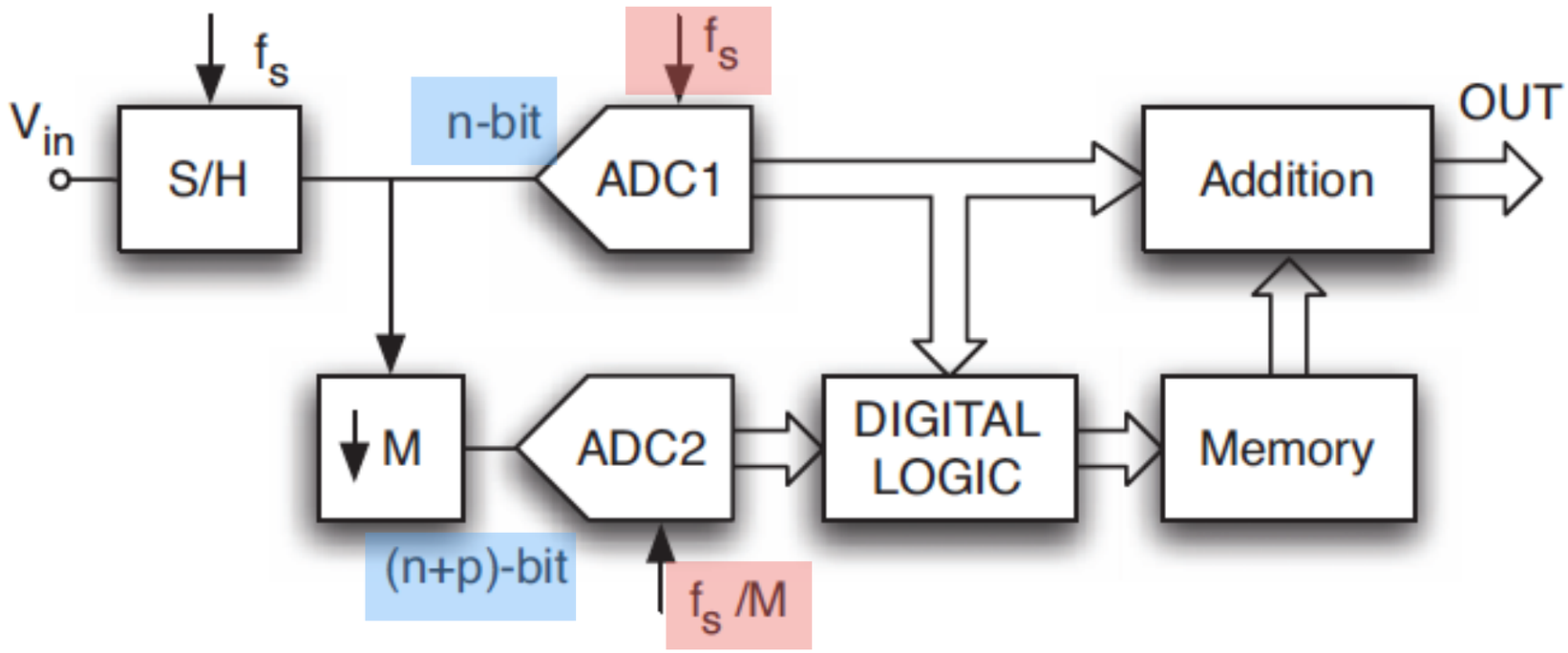
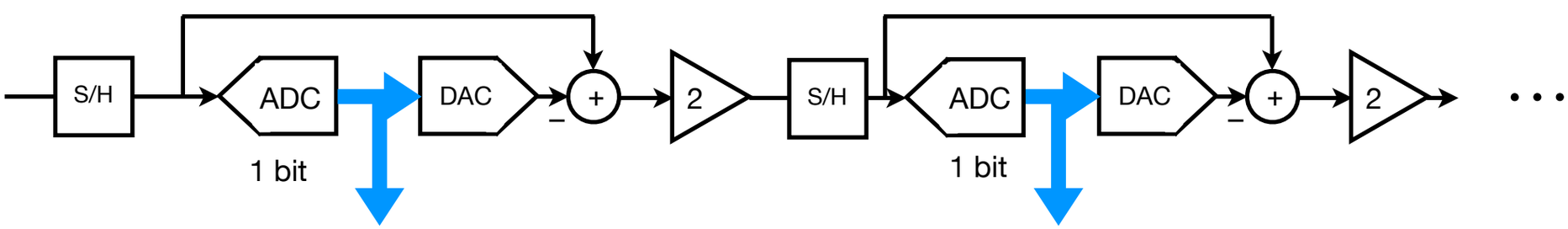


Figure 8.8. Calibration with a slow high-resolution converter.

- Auxiliary converter (ADC2) for calibration only
  - Higher accuracy, but slower
- An example; other methods possible

1-bit pipelined ADC

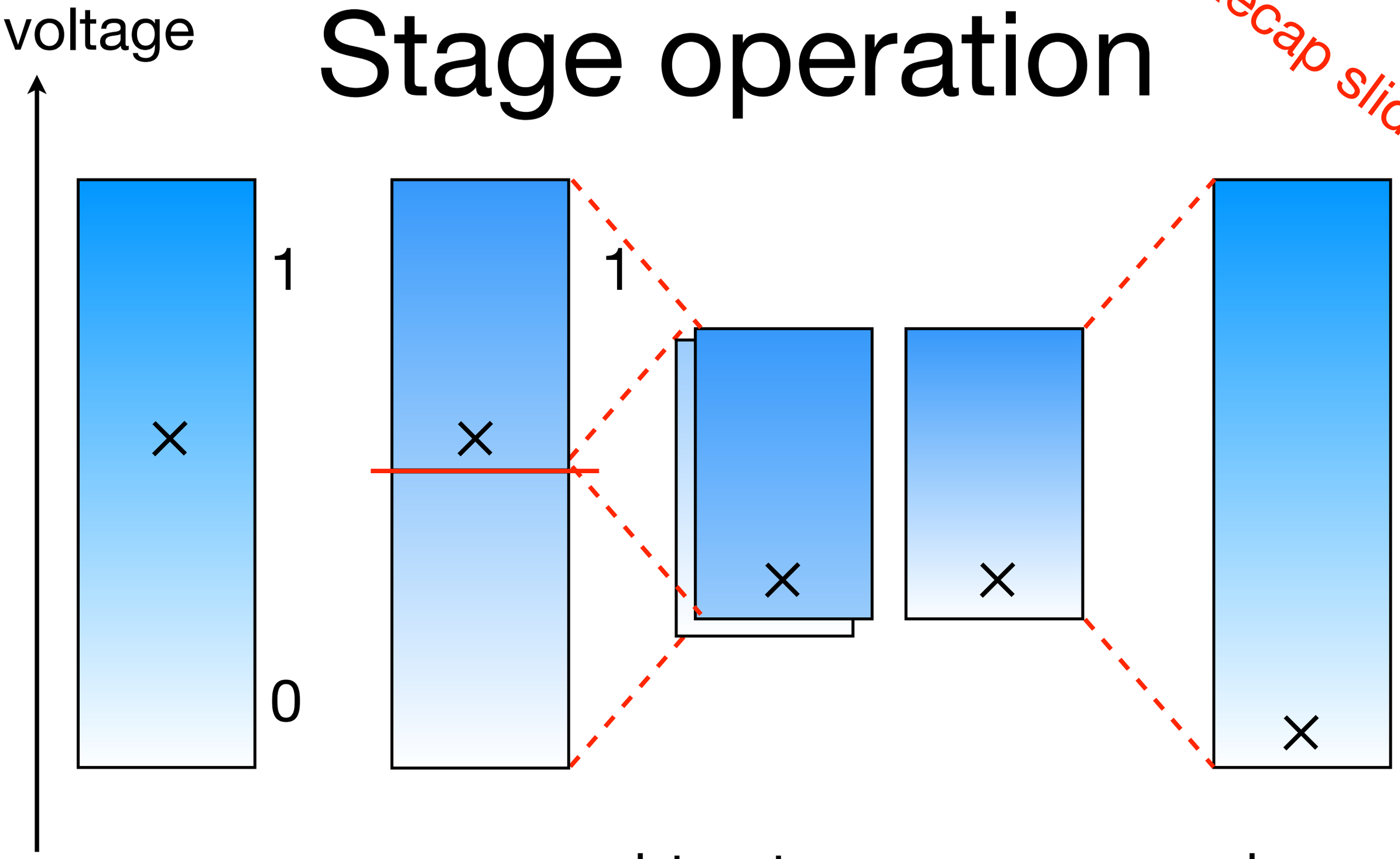


- Decide on MSB (i.e., make a 1-bit AD conversion)
- Convert bit back to analog
- Subtract from original value
- Multiply residual by 2
- Repeat for next bit, etc.

Add redundancy for error correction!

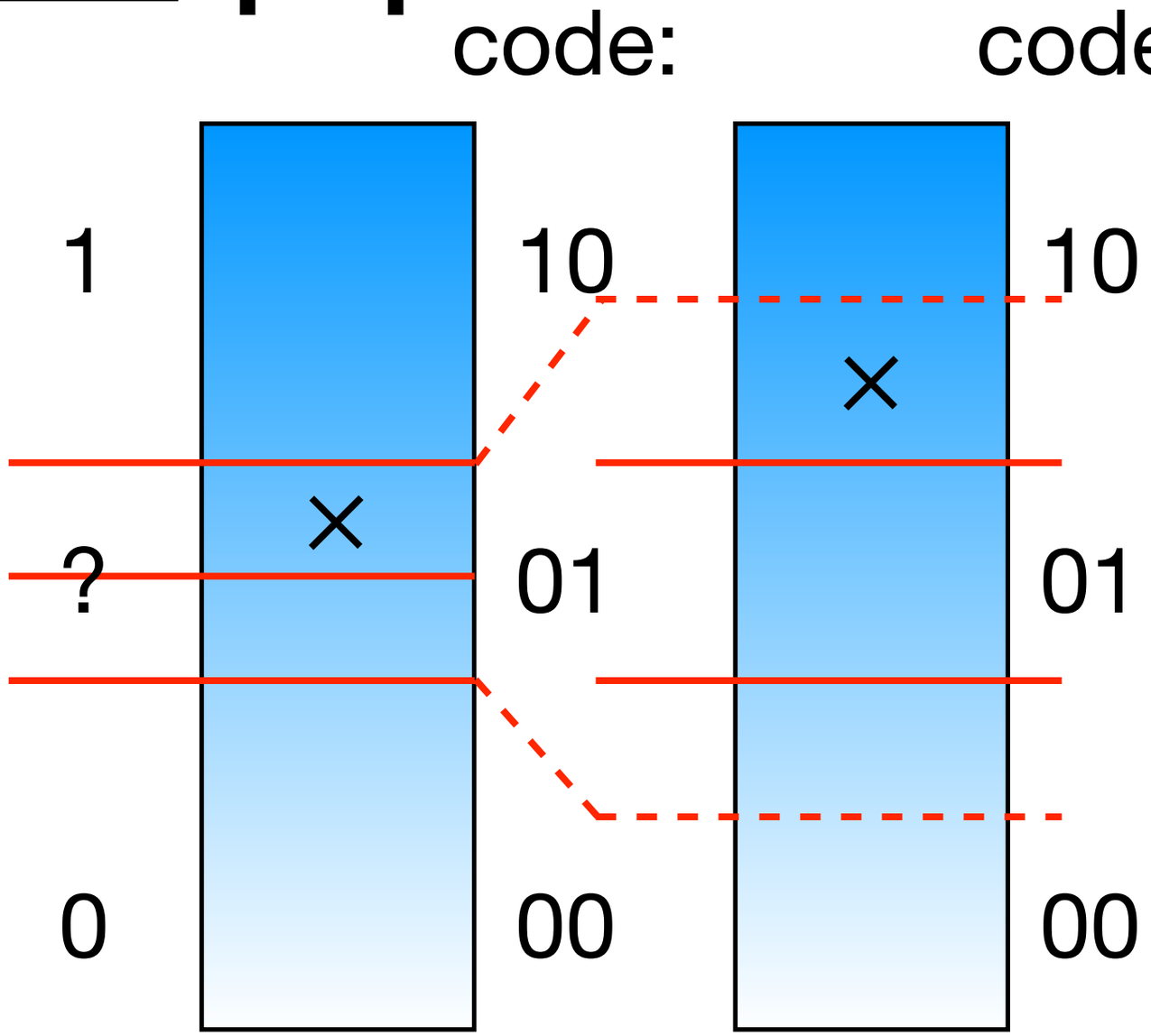
Stage operation

Recap slide



Redundant pipeline

- Idea: postpone bit decision if value close to border!
- If so, don't subtract anything, just expand
  - Now value farther from border!
- Look again after next gain stage
- Smart codes make calculation of final value trivial



0 1

1 0

1 0 0

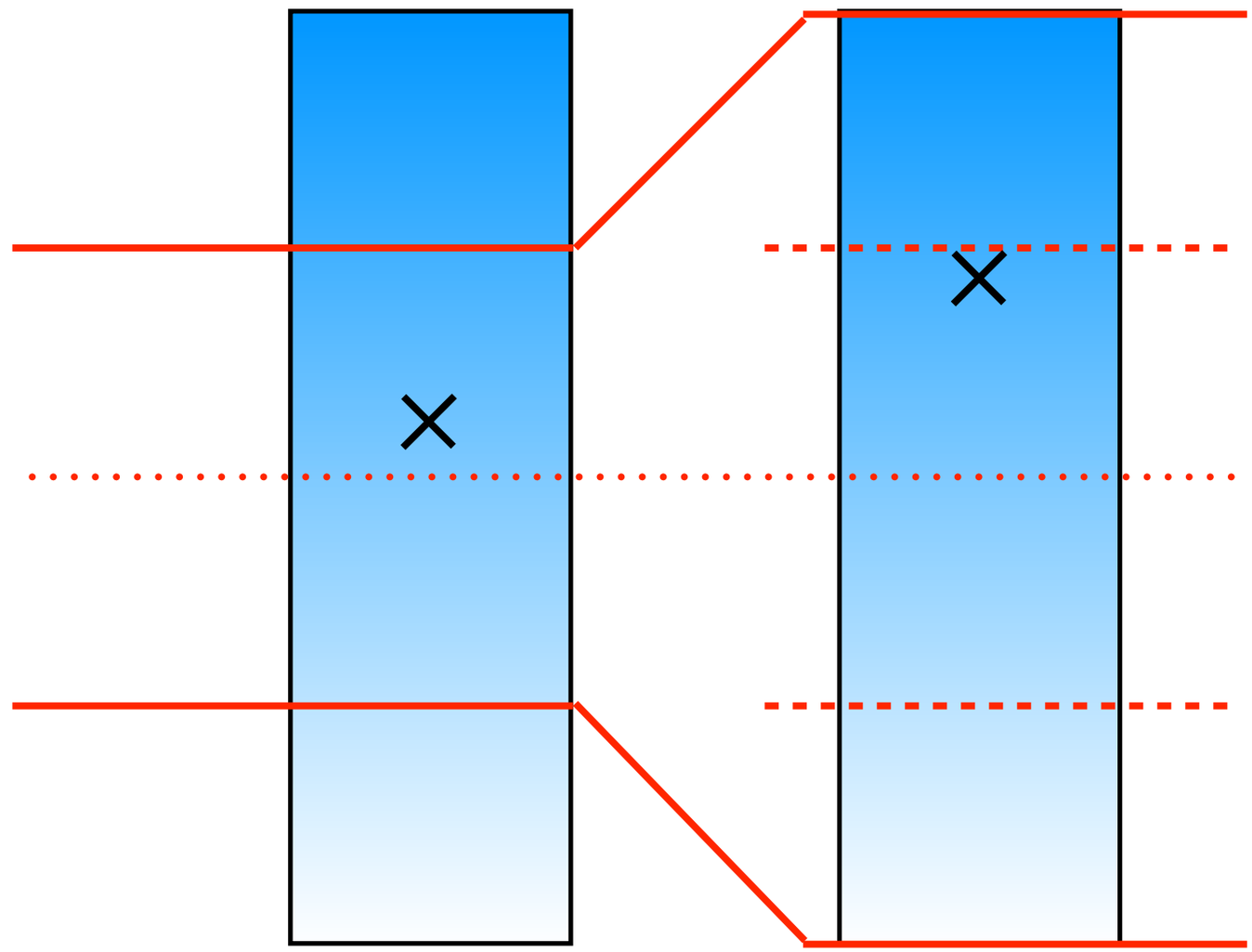
Addition!

Redundant pipeline

- Redundancy: two decisions, eventually one bit
- Two comparators / decision levels per stage
  - Still no nonlinearity!
  - Gain, offset errors
  - “1.5 bits”
    - Between 1 bit and 2 bits :-/
- No redundancy in last stage
  - Cannot be corrected since no next stage!
- Typically 1 or 2 bits in last stage

Limits?

- Delay decision for all values less than <u>half of full swing</u>!
- Allows <u>very</u> large decision errors ($\pm V_{FS}/4$)
- Very simple comparator sufficient
- 2nd delayed decision means 2-step carry in addition (etc)



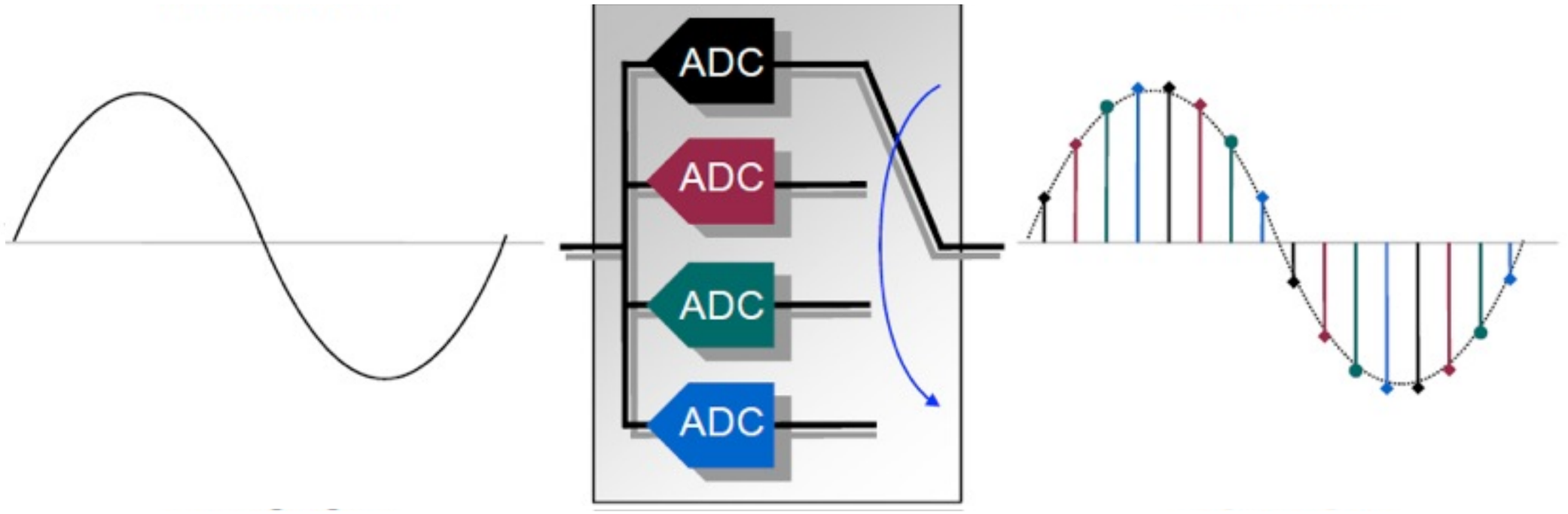
x2 gain

Benefits/drawbacks

+ One bit per stage, so #stages ~ N
+ Very insensitive to offsets
+ High sample rates
+ Simple digital parts

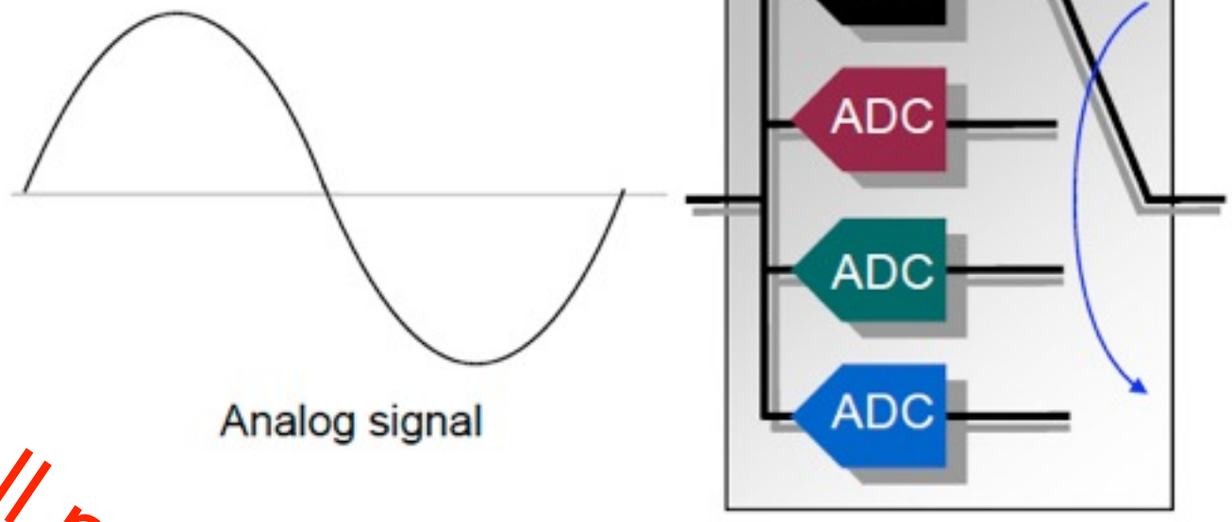
– Still depends on accurate x2 amplifier
– Latency

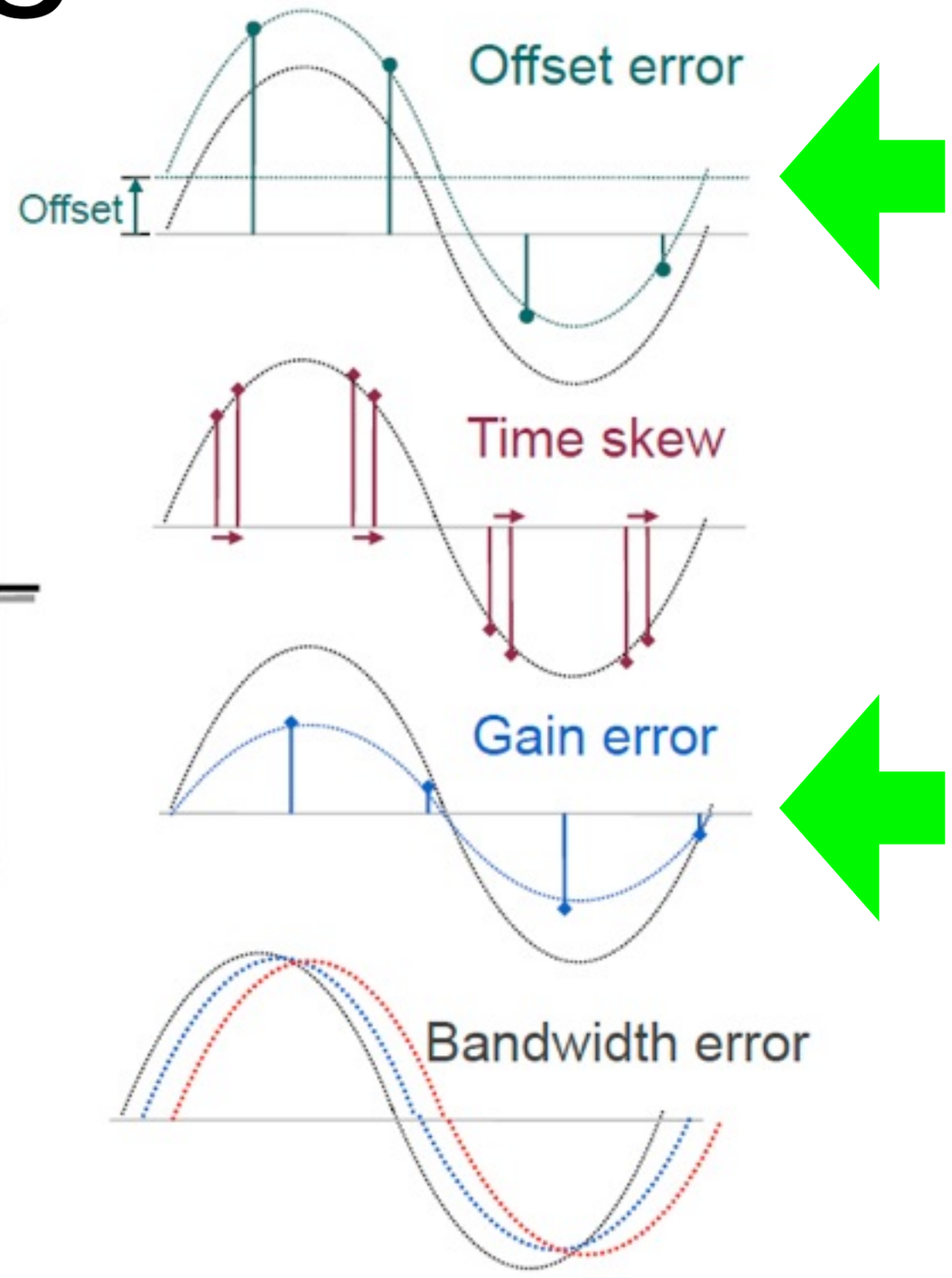
Time-interleaved ADC



- N (here: 4) parallel ADCs, each at f_S
- Round-robin sampling @ N times f_S
- Problem: ADCs not identical in practice
  - Systematic errors of several kinds

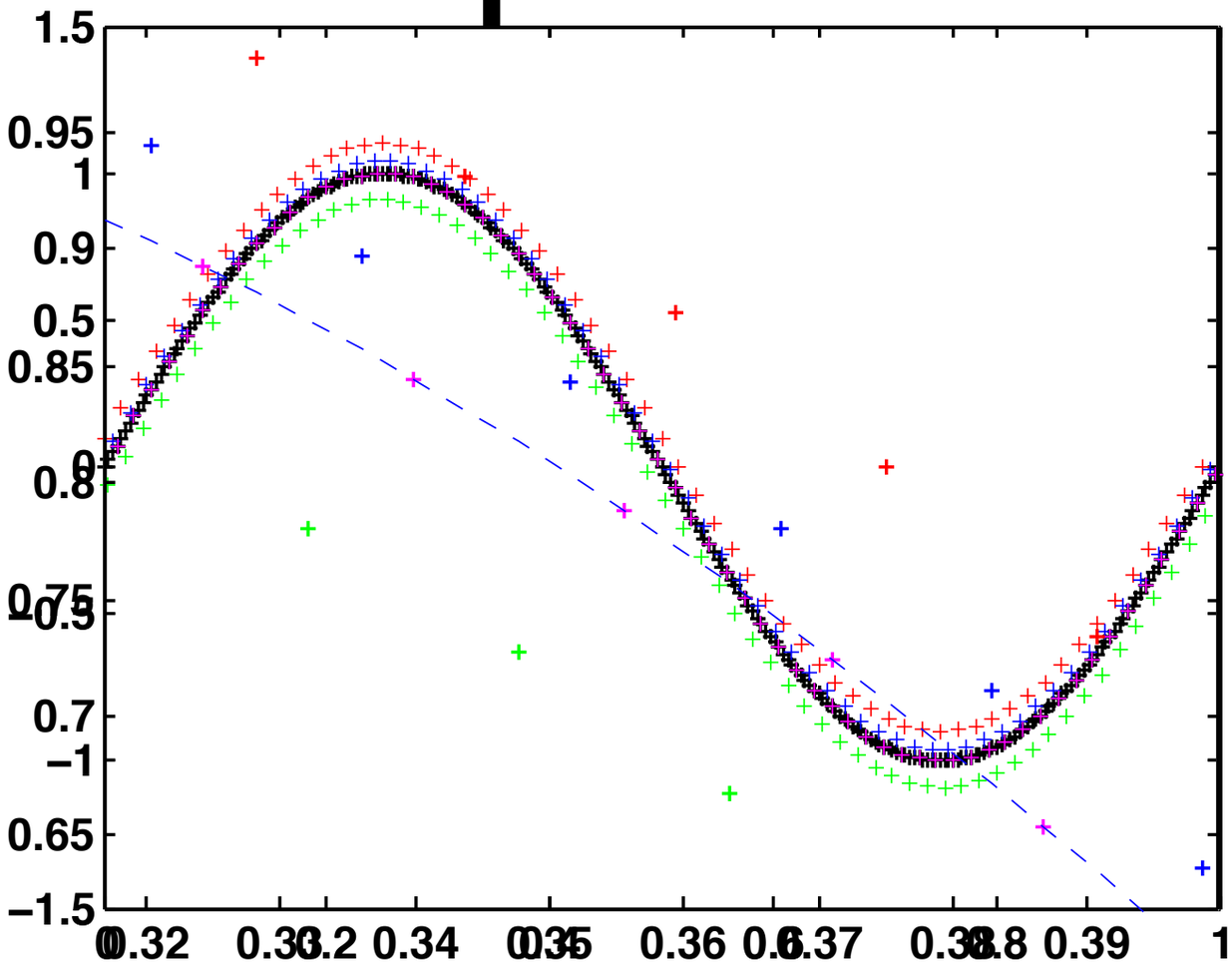
Interleaving errors





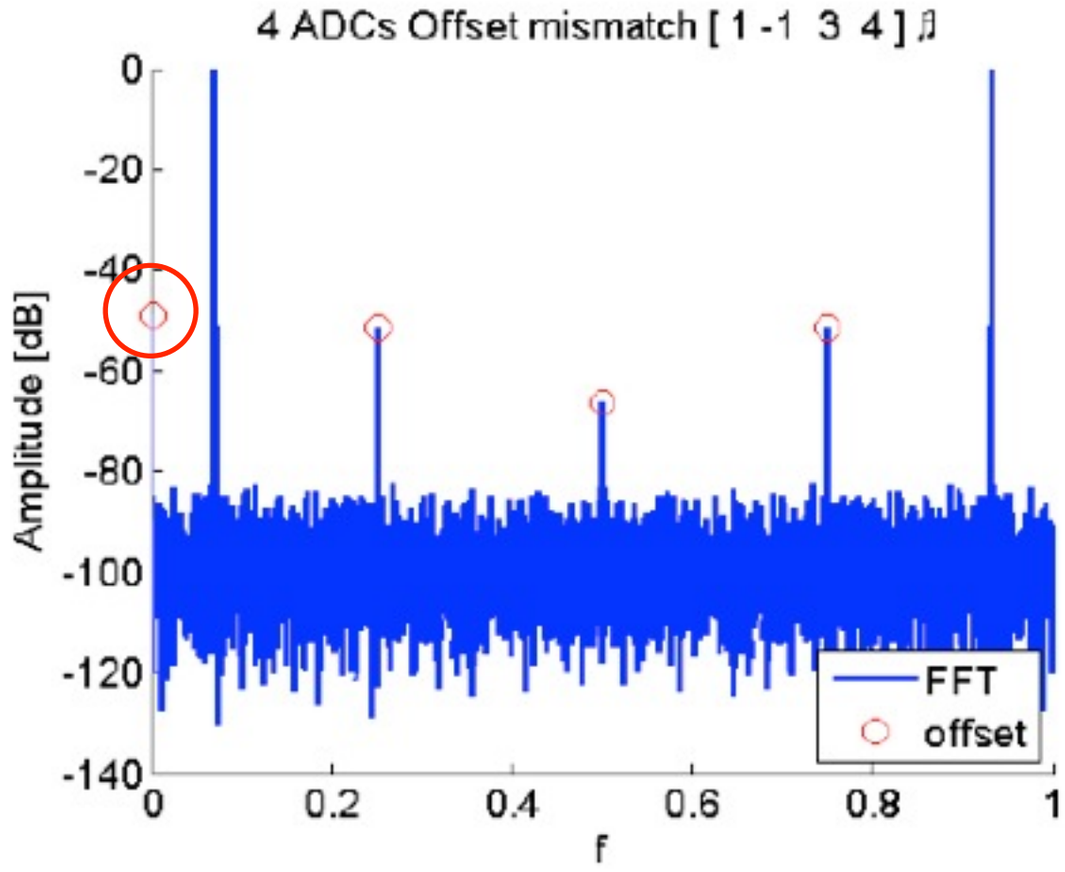
All possible to handle.

Example: offsets



- Offset of each ADC path affects sampled and converted values
- Repeating sequence of offset values added to signal
  - …O_1 O_2 O_3 O_4 O_1 O_2 …

Offsets in spectrum

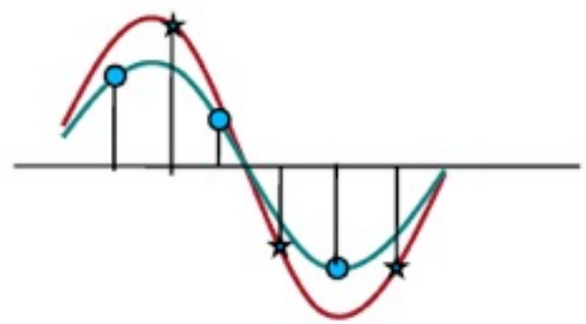


- In spectral domain, will show as spur components at $n \cdot f_S/N$, $n = 0 \ldots N - 1$
- Note: spur frequencies <u>unrelated</u> to signal frequency!
  - Occur also with no input signal!

Example: gain error

- Two paths:

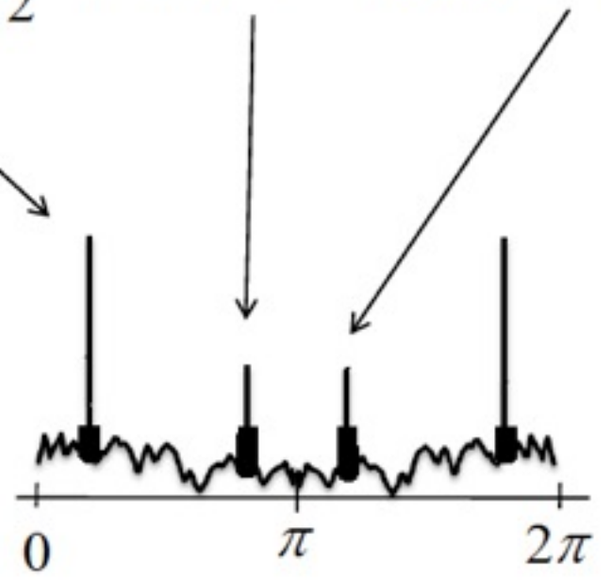
$$s(nT) = \begin{cases} A_1 \sin(\omega nT) & n \text{ even} \\ A_2 \sin(\omega nT) & n \text{ odd} \end{cases}$$



$$s(nT) = (\alpha + \beta \cos(\pi n)) \cdot \sin(\omega nT)$$

± 1

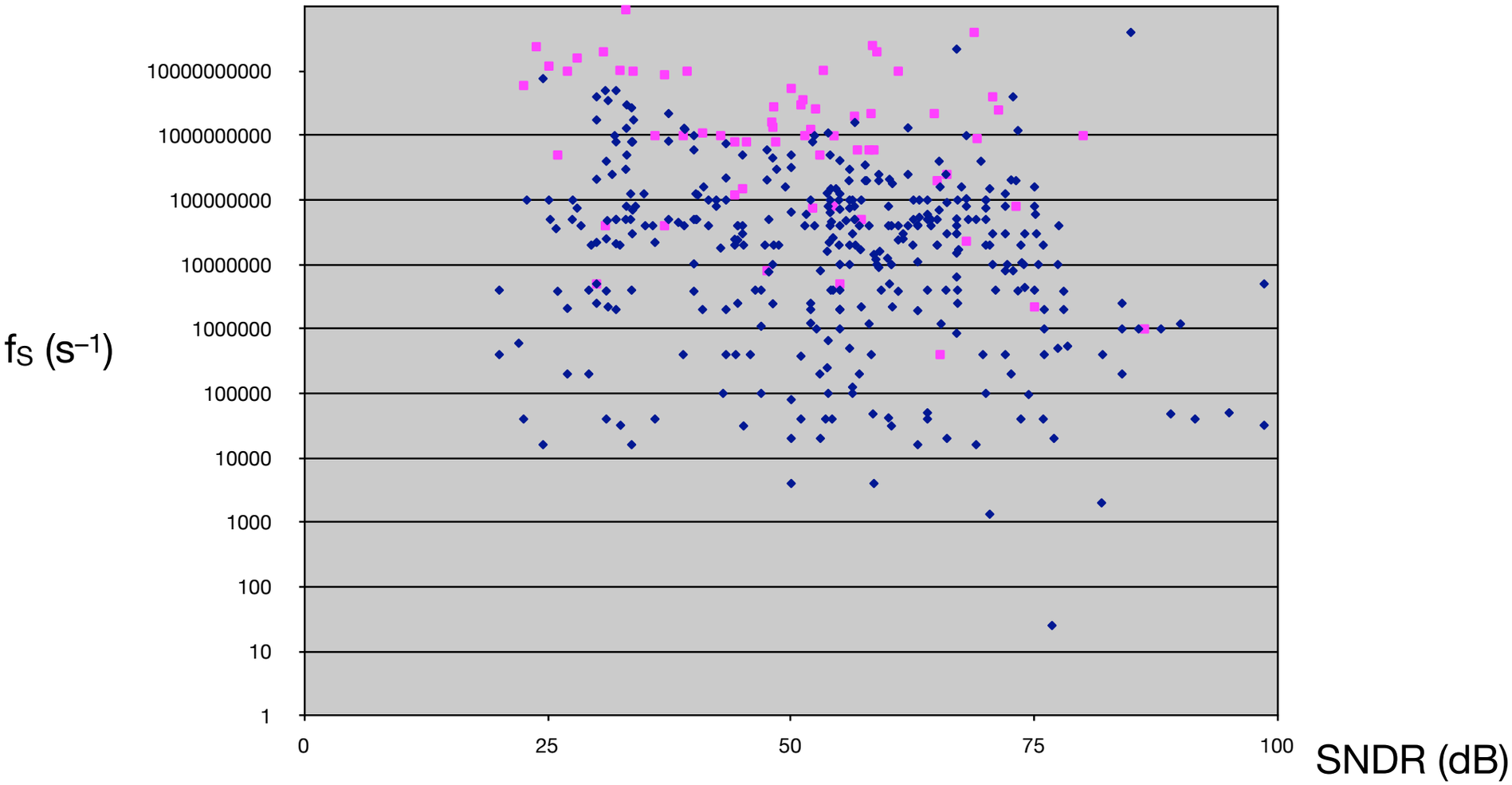
$$s(nT) = \alpha \cdot \sin(\omega nT) + \frac{\beta}{2} \cdot (\sin((\omega T - \pi) \cdot n) + \sin((\omega T + \pi) \cdot n))$$



spurs centered around $f_s/2$

depend on input f

When useful?



- Magenta dots for time-interleaved converters
- High sample rates regardless of SNDR

[Murmann data]

Why use interleaving?

- Increase sample rate!
  - Possibly by factor N with N converter paths
- Improve speed/power relation
  - Choose more frugal architecture for substituent path converters
  - Hope for less than N · (1/N) overall power
  - Digital correction circuitry is “free” 😀

Literature

First publication

- W. C. Black Jr. and D. A. Hodges, "Time Interleaved Converter Arrays," IEEE International Conference on Solid State Circuits, Feb **1980**, pp. 14–15.

Examples!

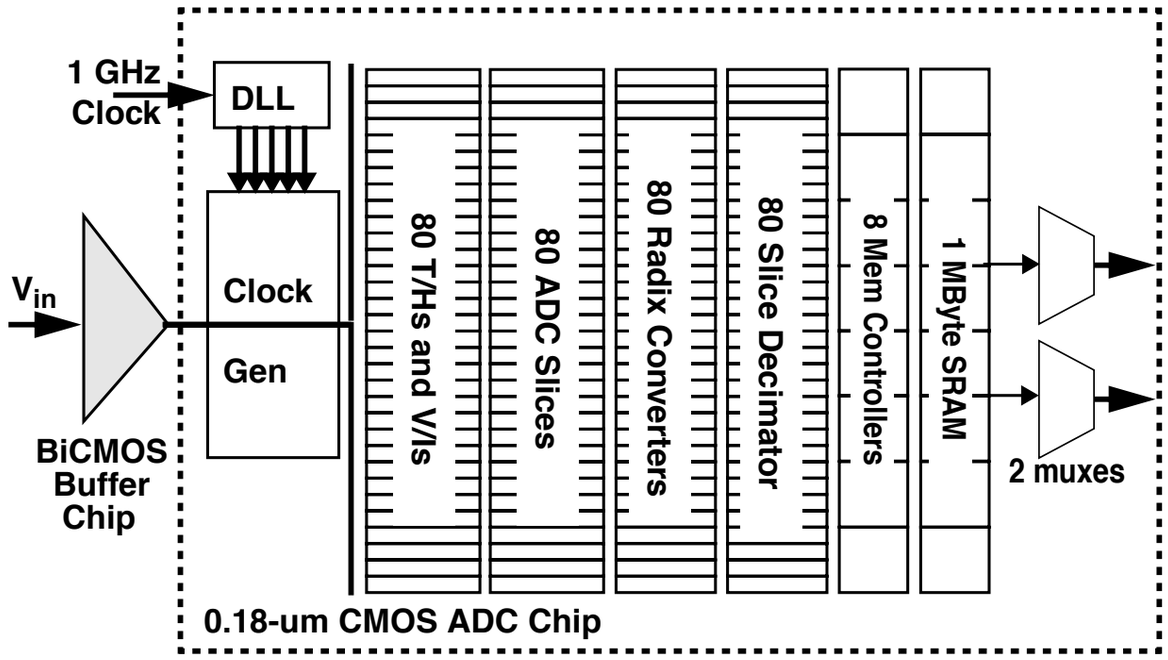
Use IEEExplore!

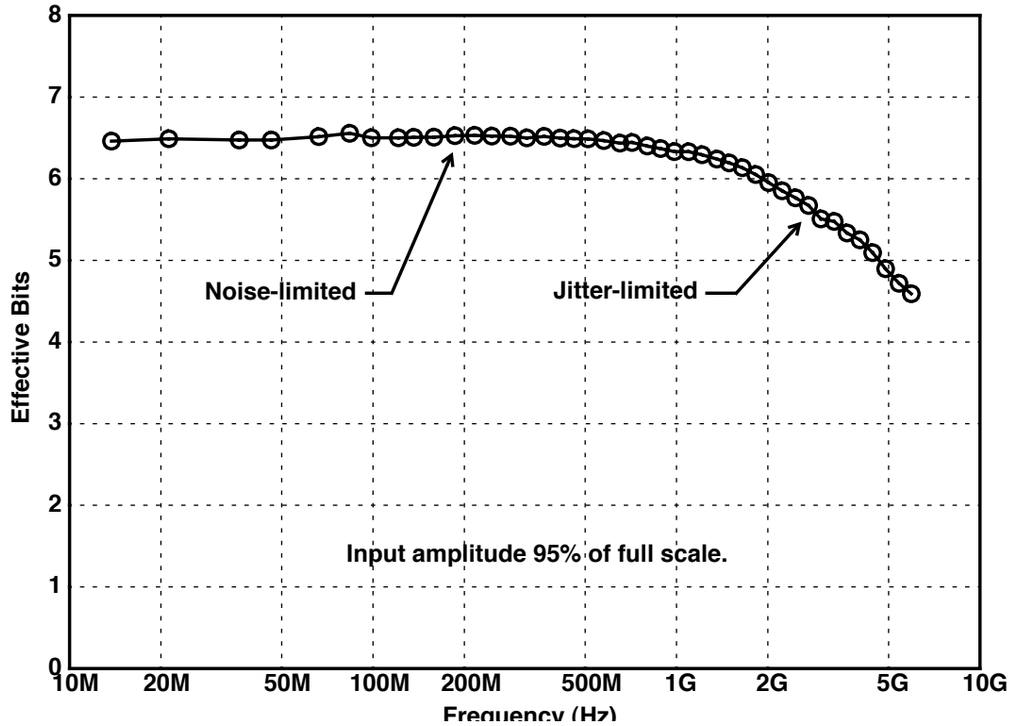
Prof. Murmann's data!

ISSCC2008 typical paper references:

- [1] K. Poulton, R. Neff, B. Setterberg, et al., "A 20 GS/s 8 b ADC With a 1 MB Memory in 0.18µm CMOS," *ISSCC Dig. Tech. Papers, pp. 318-319, Feb.* **2003**.
- [2] S. Gupta, M. Inerfield, and J. Wang, "A 1-GS/s 11-bit ADC With 55-dB SNDR, 250-mW Power Realized by a High Bandwidth Scalable Time-Interleaved Architecture," *IEEE J. Solid-State Circuits, vol. 41, pp. 2650*-2657, Dec. **2006**.
- [3] D. Draxelmayr, "A 6b 600MHz 10mW ADC Array in Digital 90nm CMOS," *ISSCC Dig. Tech. Papers, pp. 264-265, Feb.* **2004**.
- [4] B. P. Ginsburg and A. P. Chandrakasan, "500-MS/s 5-bit ADC in 65-nm CMOS With Split Capacitor Array DAC," *IEEE J. Solid State Circuits, vol.* 42, no. 4, pp. 739-747, Apr. **2007**.

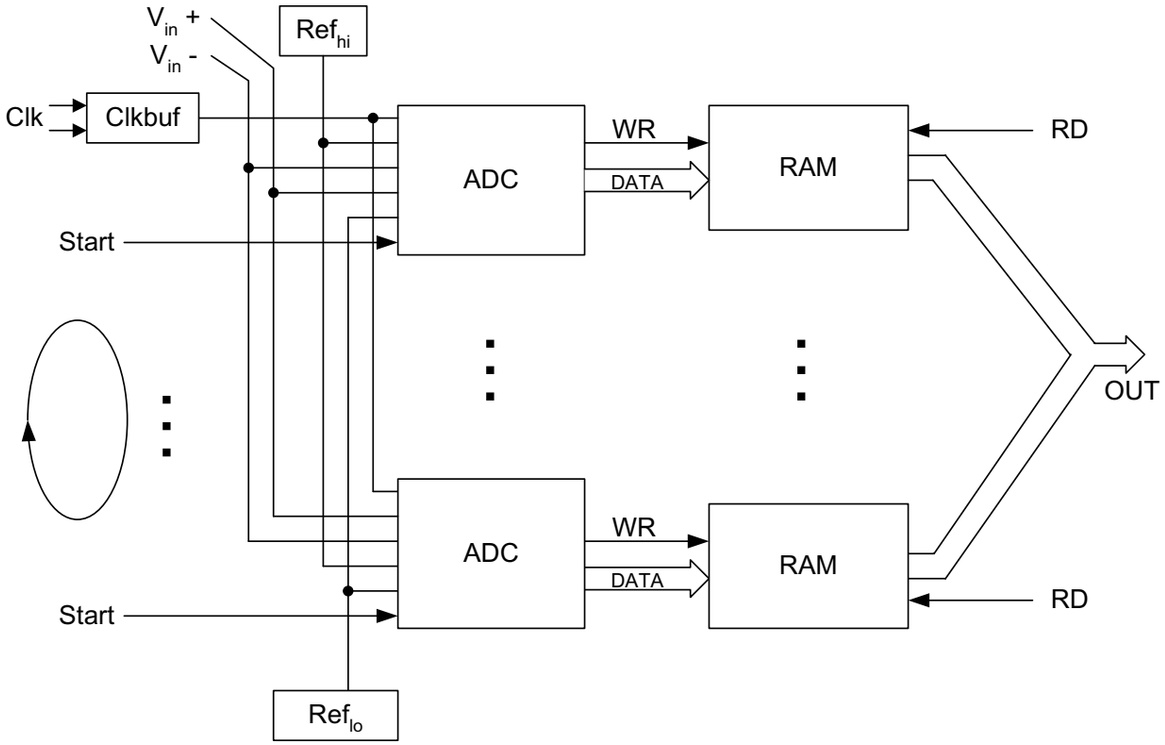
Poulton 2003

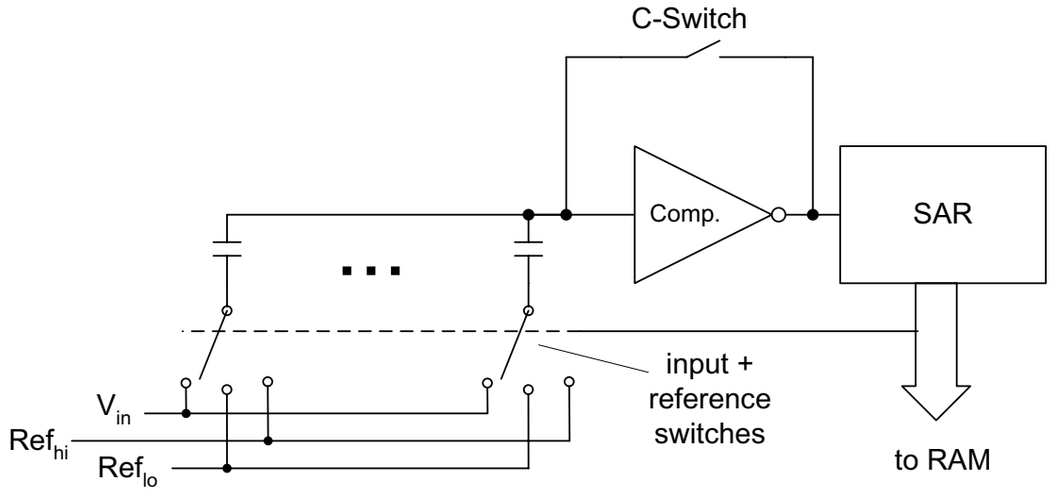




- 80 interleaved 12-stage pipelined ADCs
- 1.5 bits / stage, reduced to 8 bits w/ corrections
- 8 bits @ 20 GS/s, ≤6.5 ENOB
- 1 W (buffer) + 9 W (ADC) = 10 W

Draxelmayr 2004





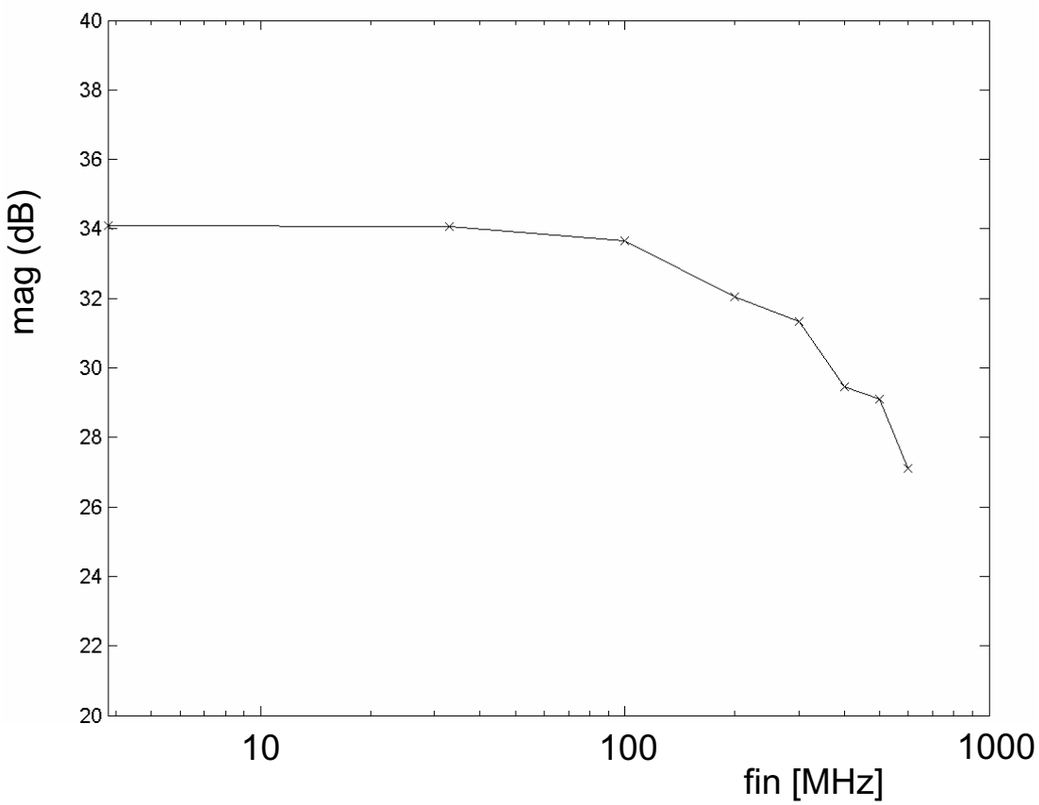
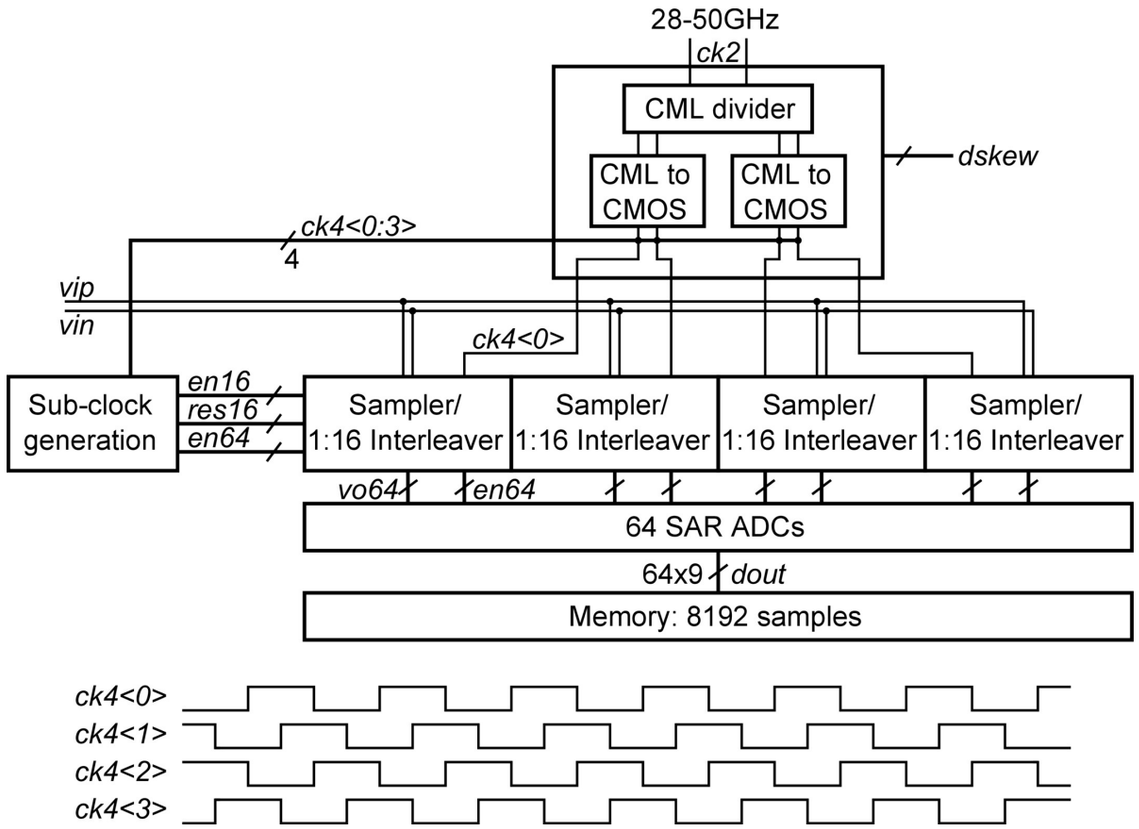
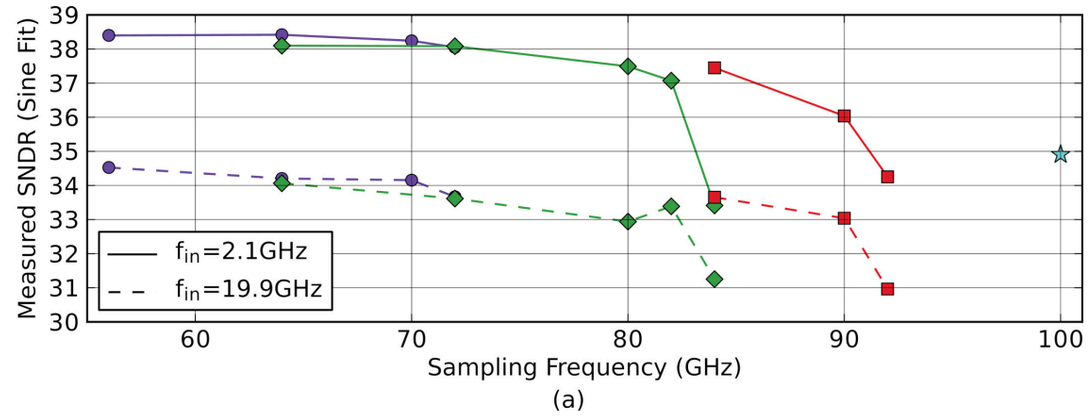


Figure 14.7.6: SINAD vs. fin at fc=600MHz (offset corrected).

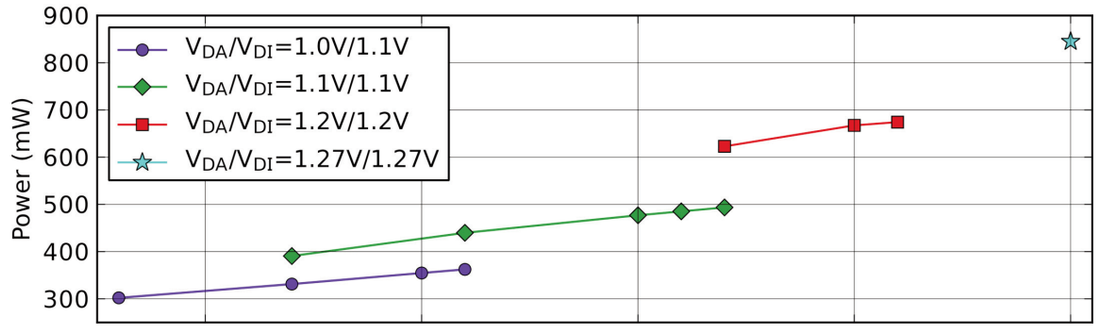
- 6b, 8-way interleaved
- SAR sub-converters
- 10 mW @ f_S = 600 MHz

Kull 2014





(a)



(b)

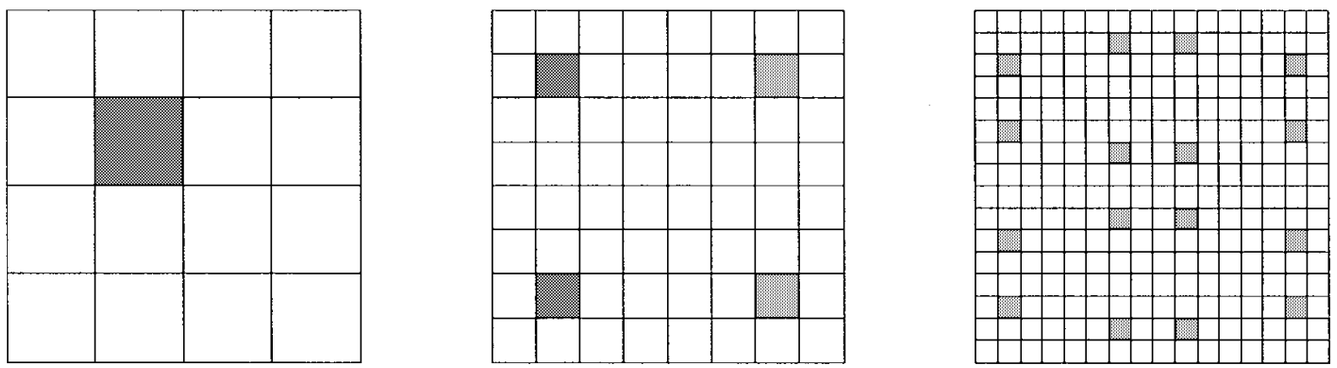
- 90 GS/s, 8b, 667 mW
- 64 SAR sub-converters
- Current world record for ADC sample rate

[L. Kull et al. A 90GS/s 8b 667mW 64× Interleaved SAR ADC in 32nm Digital SOI CMOS. ISSCC 2014.]

Improving on average

D/A converter errors

- Thermometer-coded, unary-scaling current-source D/As very popular
  - Large number of sources (2^N)
    - Large area
  - Mfg gradient errors cause harmonics
    - Improve matching with <u>common-centroid layouts</u>
      - Split sources in groups with common center
      - More switches, etc



(a) (b) (c)

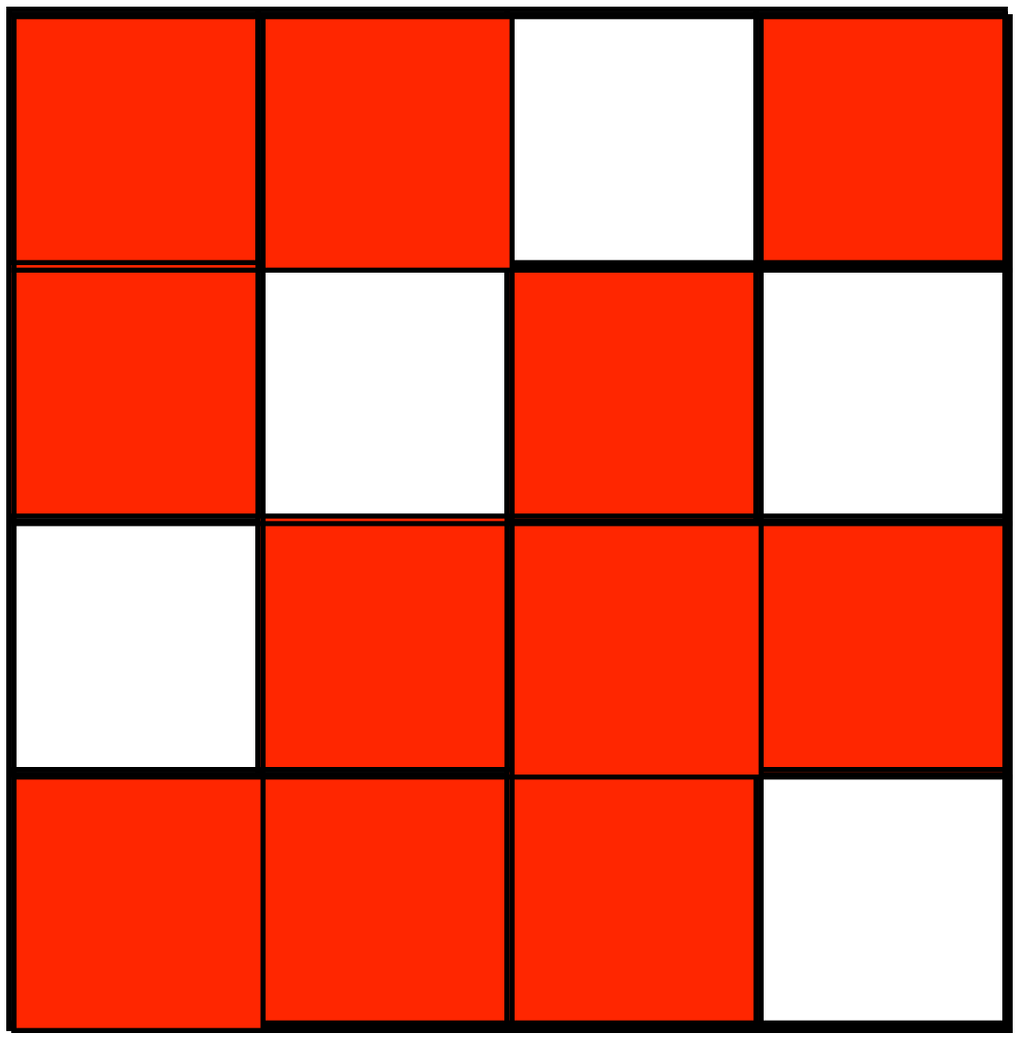
[Van der Plas 1999]

Errors vs distortion

- Remaining INL/DNL will cause harmonic distortion of sinewave input
  - Spurious tones in output
  - Often undesirable (depends on application)
- INL/DNL diagrams show the error at each output value
  - Error is well-defined since always the same set of current sources (with same set of deviations) for same converted value

Randomization

- Idea: use <u>different</u> set of sources for each conversion!
- Select e.g. by pseudo-random sequence
- “Dynamic element matching”
- Distortion -> noise
- Better SFDR!
- Esp. useful for feedback DACs in ∑Δ ADCs



[L. R. Carley. Noise-shaping coder topology for 15+ bit converters. IEEE Journal of Solid-State Circuits, April 1989]

Poulton 2011

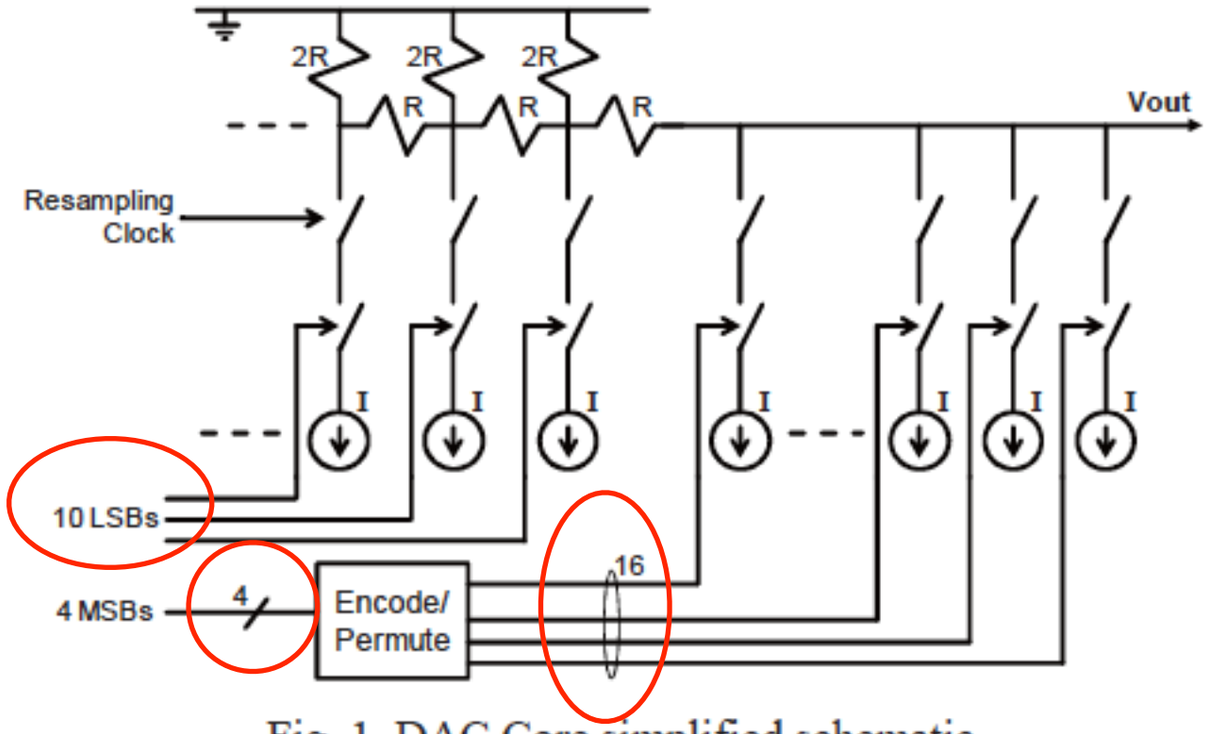


Fig. 1 DAC Core simplified schematic

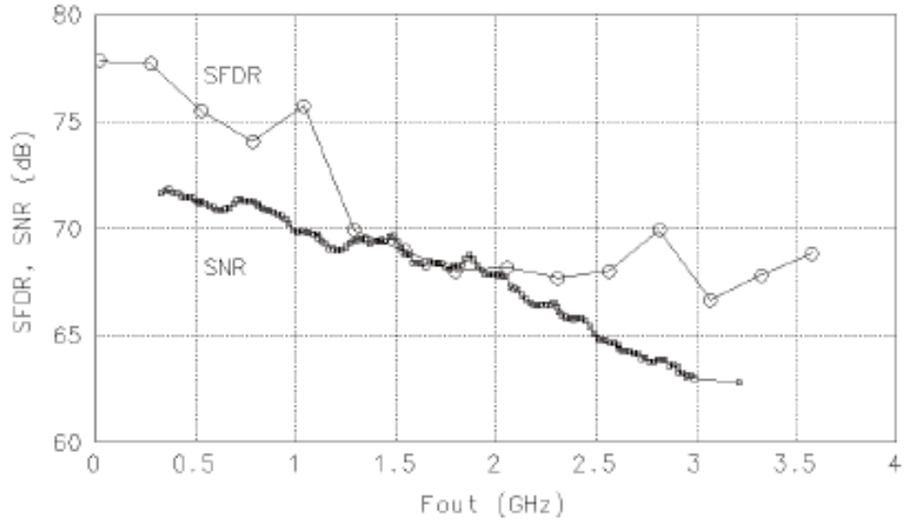


Fig. 5 SFDR (including harmonics) and SNR vs. Fout at 7.2 GSa/s

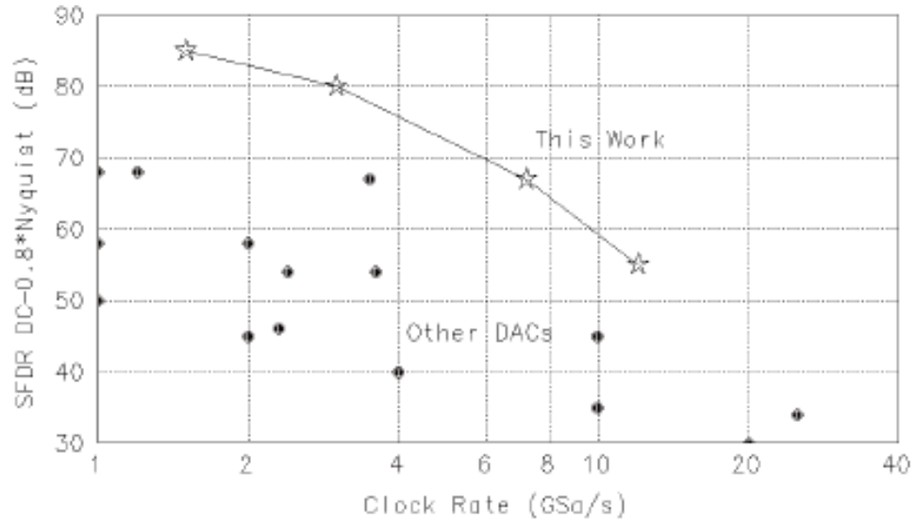
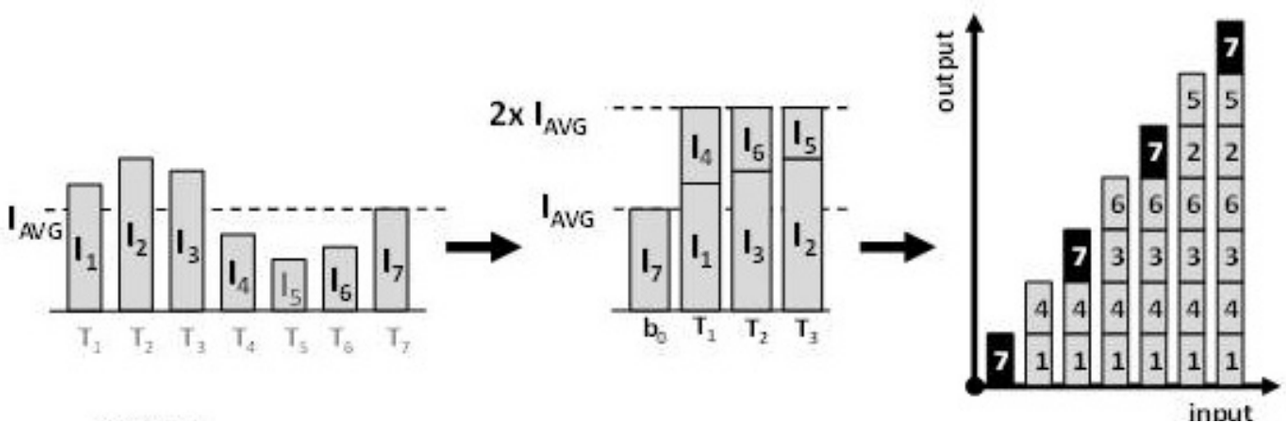


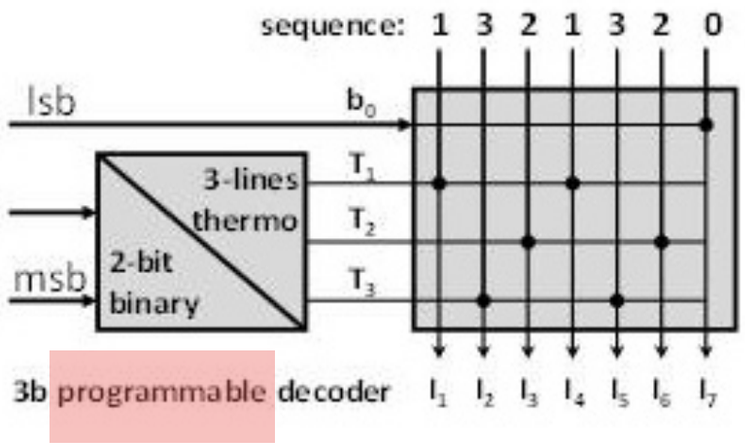
Fig. 6 SFDR over Nyquist vs clock rate for this DAC and other DACs (published papers and datasheets)

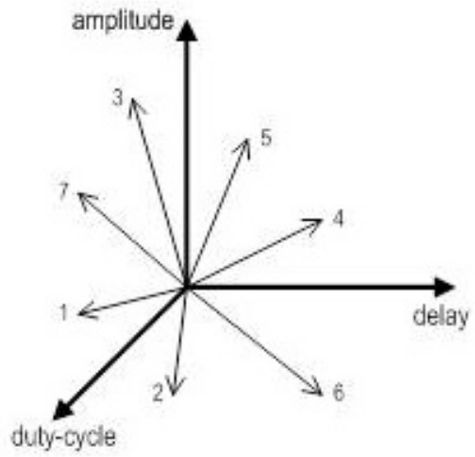
- 14b, 7.2 GS/s
- Unary scaling for 4 MSBs, binary scaling for the rest
  - MSBs randomized
- SFDR ~10 dB better than comparable DACs
- 4.6 W (ugh)

[K. Poulton et al. A 7.2-GSa/s, 14-bit or 12-GSa/s, 12-bit DAC in a 165-GHz f_T BiCMOS Process. SVLSI 2011.]

“De-randomization”







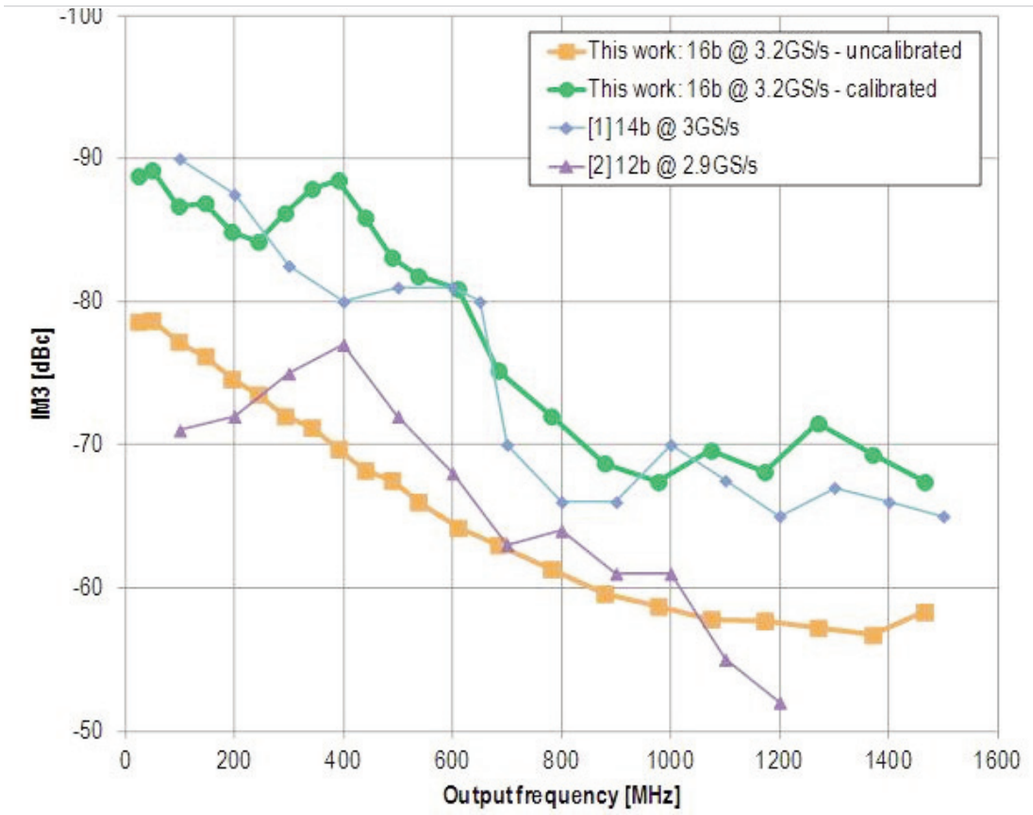


Figure 11.7.4: IM3 versus output frequency with and without 3D-SC calibration compared to state-of-the-art multi-GS/s CMOS DACs.

- Rather than random combination, select <u>best</u> combo
- Several dimensions (amplitude, delay, duty cycle)

[Van de Vel et al. A 240mW 16b 3.2GS/s DAC in 65nm CMOS with <-80dBc IM3 up to 600MHz. ISSCC2014]

Summary

- Digital techniques highly useful to compensate for many kinds of conversion errors
  - Per sample and/or on average
    - Performance far beyond what is possible with “ordinary” techniques
- Digital gets cheaper over time (Moore!)
  - Suggests trend towards simpler analog and more sophisticated digital processing (cf. Murmann)