Technology parameters for 0.065-μm (65-nm) process 2013

Note: The design rules and electrical parameters presented in this document are representative for a 0.065-μm CMOS process, and are intended for teaching purposes only. $V_{DD} = 1.2V$ normally.

For svtlp transistors					
	Transistor type				
	nMOS		pMOS		Unit
Gain factor L < 10 μm	$k'_n(\mu_n C_{ox})$	300	$k'_p(\mu_p C_{ox})$	100	$\mu A/V^2$
Threshold voltage	V_{t0n}	0.29	V_{p0n}	-0.27	V
Early voltage, L = 1 μm	V_{An}	10	V_{Ap}	10	V
Early voltage, L = 10 μm	V_{An}	20	V_{Ap}	20	V
Saturation current / width (L = 0.06 μm)	I_{DSATn}	0.60	I_{DSATp}	0.30	$mA/\mu m$

Capacitances (layer to substrate)				
	Area $fF/\mu m^2$		Perimeter $fF/\mu m$	
gate oxide capacitance	C_{ox}	20		
gate-diff (S/D) overlap			C_{gso}	0.2
n+ diff (0 V)	C_{j0n}	1.2	C_{jswn}	0.04
n+ diff (0 V) - gatewall			C_{jgwn}	0.12
p+ diff (0 V)	C_{j0p}	1.2	C_{jswp}	0.04
p+ diff (0 V) - gatewall			C_{jgwp}	0.12

Sheet resistance		
Layer		$\Omega/\square$
poly	R_{sp}	15
metal1	R_{sm1-4}	0.15
metal2-6	R_{sm1-4}	0.11
metal7	R_{sm5}	0.024
n+ diff (S/D)	R_{sdn}	12
p+ diff (S/D)	R_{sdp}	15
n-well	R_{snw}	800

Contact resistance		
Layer-layer		Ω / cnt
metal1-n+ diff	R_{cdn}	37.5
metal1-p+ diff	R_{cdp}	37.5
metal1-poly	R_{cp}	37.5
via1-5	R_{via1-5}	1
via6	R_{via6}	0.5

Diffusion cap voltage-dep. parameters				
		nMOS	pMOS	
Bottom junction pot.	V_{jb}	0.7	0.75	V
Bottom grading coeff.	m_{jb}	0.3	0.3	
Sidewall junction pot.	V_{jsw}	1.0	2.0	V
Sidewall grading coeff.	m_{jsw}	0.3	0.3	
Gate sidew. junction pot.	V_{jg}	1.8	2.0	V
Gate sidew. grading coeff.	m_{jg}	0.95	0.95	

Latch-up prevention

1. All wells must have at least one contact to VDD.
2. Place well and substrate contacts whereever possible.
3. Maximum distance between well/substrate contacts is 30 μm.