Chapter 2: The MOSFET

The aim of chapter 2 is to consider the MOSFET in more detail and to provide the reader with a simple electrical model of its current-voltage characteristics. We will be reminded that the field-effect is a capacitive effect, and that a certain minimum input voltage is needed to turn the MOSFET ON. Starting from the first lecture assumption of a MOSFET being just a simple switch, we will learn that the MOSFET is a switch, but not a perfect switch. First, since the off resistance R_{OFF} is not infinite, there is a certain subthreshold leakage current, I_{OFF}, flowing when the MOSFET is OFF. Second, the MOSFET shows a built-in current-limiting behavior causing the output current to saturate at a maximum value, I_{DSAT}. This means that the MOSFET, when ON, can operate either in its linear region, or, beyond a certain voltage, in its saturation region. A simple long-channel square-law MOSFET model will be used to predict MOSFET current/voltage characteristics. Even though the long-channel MOSFET model is not fully accurate for detailed modeling of today´s short-channel devices, it is quite easy to handle and it has the property of providing the most basic insight into MOSFET circuit behavior. Furthermore, many short-channel models are based on the long-channel model, and provides the necessary accuracy by second-order add-on equations.

In this lecture, we will introduce an equivalent circuit model to describe the electrical behavior of the MOSFET, a circuit model similar to that of the relay (an electrically operated switch, commonly used in automotive applications). See Fig. 2.1 for a circuit model of the saturated MOSFET. As opposed to the relay, that has an inductive input, the MOSFET (being a field-effect transistor, FET) has a capacitive input with a certain gate capacitance, C_G. Furthermore, the device has a parasitic output capacitance, C_D, due to the drain and source output terminals. In electrical circuit models, current saturation is shown by using a voltage-controlled current source, I_{DSAT}.

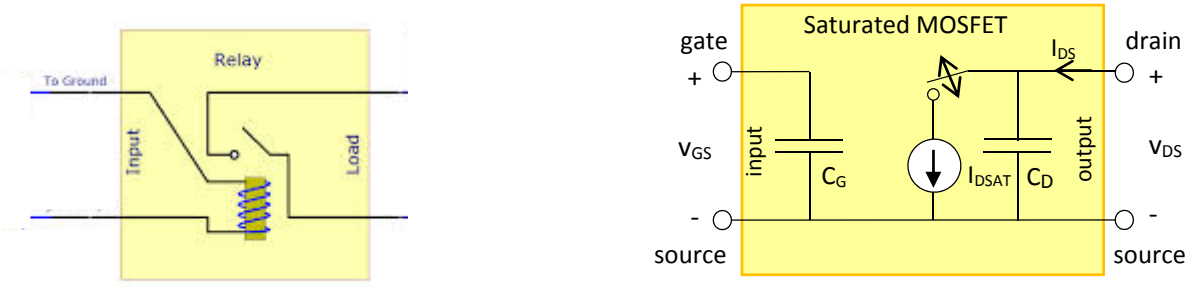
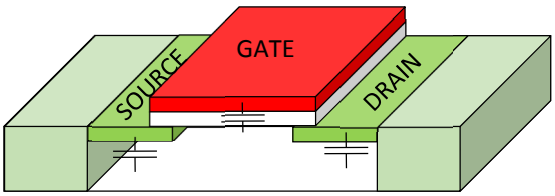


Fig. 2.1. Electrical circuit models for relays and MOSFETs.

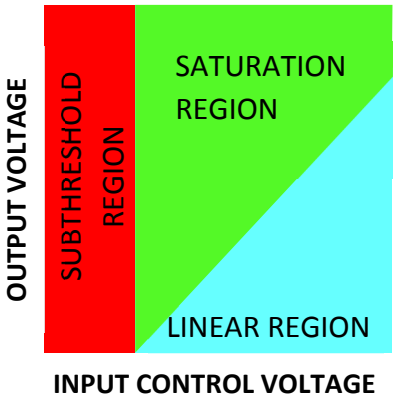
The next figure, Fig. 2.2, shows a cross-sectional view of the MOSFET, indicating the gate, source and drain capacitances. Also in this figure, the long-channel square-law MOSFET model equations are given. The model has two model parameters (the transconductance parameter, k, and the threshold voltage, V_T) for the ON region, and two model parameters for the OFF region (OFF current I_{OFF}, and subthreshold ideality factor, n). The MOSFET drain current is controlled by the input gate-source voltage, V_{GS}, or more precisely by the gate voltage overdrive, $V_{GST}=V_{GS}-V_T$. In saturation, the drain current is independent of the drain-source voltage, V_{DS}.

In a very simple approximation, the gate capacitance can be calculated by multiplying the channel area (as defined by the MOSFET channel width, W, and the channel length, L) with the oxide capacitance per unit area, C_{ox} (typically 20 fF/μm^2 for a 65 nm CMOS process), which is parameter supplied by the

manufacturer. The regions where the subthreshold, linear and saturation region models are valid are indicated in the red-blue-green V_{DS}/V_{GS} voltage plane to the right. This is an important graph for future understanding of the CMOS inverter, for instance.



$$I_{DS} = \begin{cases} I_{OFF} e^{V_{GS}/nV_{th}} = I_{OFF} 10^{V_{GS}/S} & \text{subthreshold region} \\ k\left(V_{GST} - V_{DS}/2\right)V_{DS} & \text{linear region} \\ kV_{GST}^2/2 & \text{saturation region} \end{cases} \quad (2.1)$$



$$\text{MOSFET caps} = \begin{cases} C_G = WLC_{ox}, \text{ input gate capacitance} \\ C_D = pC_G, \text{ parasitic drain capacitance} \end{cases} \quad (2.2)$$

Fig. 2.2 MOSFET cross-section, current and capacitance models, and regions of model validity.

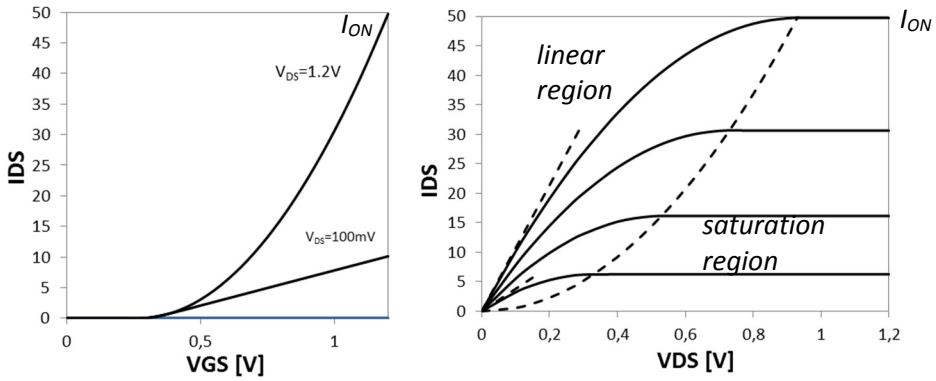


Fig. 2.3. MOSFET transfer characteristic (left) and output characteristics (right).

The MOSFET current-voltage transfer (left) and output characteristics (right) are shown in Fig. 2.3. The replot of the transfer characteristic on a semi-logarithmic scale in Fig. 2.4 shows the MOSFET behavior in the subthreshold region. The exponential subthreshold dependence of the drain current on the gate-source voltage in the OFF region is clearly visible. The subthreshold current is characterized by two parameters, the OFF current, I_{OFF} (V_{GS}=0, V_{DS}=V_{DD}), and the subthreshold swing (or slope) S=nV_{th}ln10, a typical swing value being 100 mV/decade. The I_{ON}/I_{OFF} ratio between the maximum available drain current (V_{GS}=V_{DD}, V_{DS}=V_{DD}), and the OFF current, is an important performance parameter of a MOSFET, and should be at least on the order of 10^6.

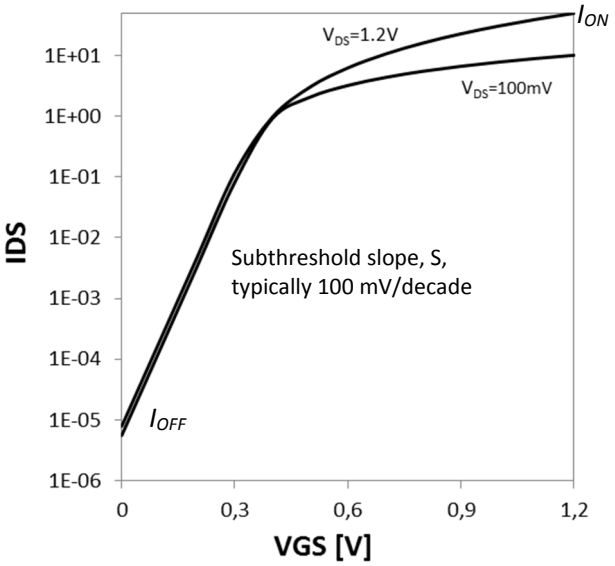


Fig. 2.4. MOSFET subthreshold behavior.

We will come back to the importance of a low OFF currents in a later chapter when discussing the static, or leakage, power dissipation. It should also be pointed out that if the threshold voltage is decreased in order to increase the gate voltage overdrive, V_{GST}, then the subthreshold leakage current, I_{OFF}, increases as can be seen by shifting the I/V curves to the left.

For a 65 nm CMOS process, the maximum currents that one micron wide n-channel and p-channel MOSFETs can deliver is shown in Fig. 2.5. For later use, we will also these I/V graphs to define the effective MOSFET resistances as $R_{eff}=V_{DD}/I_{ON}$,i.e. 2 kΩ·µm and 4 kΩ·µm for the n-channel and p-channel MOSFETs, respectively. The effective resistance is scalable, the wider the MOSFET, the lower the effective resistance.

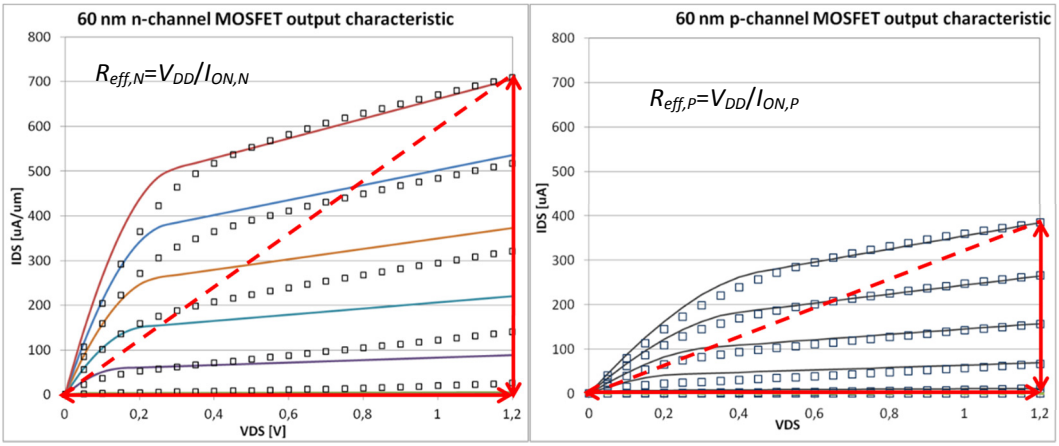


Fig. 2.5. Determining the effective resistances for n-channel and p-channel MOSFETs.

Finally, the MOSFET transconductance parameter, k, can be shown to be the product of the design parameter W/L, and the technology parameter $k'=\mu C_{ox}$ (k-prime) supplied by the manufacturer,

$$k = \frac{W}{L}\mu C_{ox} . \qquad (2.3)$$

A digital circuit designer almost always choose the minimum channel length of the available technology to obtain the maximum speed, and plays around with the channel width to obtain the desired current driving capability. On the other hand, the analog circuit designer has other preferences and often chooses longer than minimum channel lengths to obtain good current saturation.

Exercises

Exercise 2.1. Calculate the effective resistances for two MOSFETs delivering maximum currents of 500 µA and 750 µA, respectively, at a supply voltage of 1 V!

Exercise 2.2. Calculate the gate capacitance for a 1 mm wide MOSFET in the 60 nm CMOS process if its insulator capacitance per unit area is given as 20 fF/µm^2!

Exercise 2.3. If the effective resistance of a MOSFET in a certain technology is specified as 2 kΩ·µm, what would be the effective resistance of a) a 5 µm wide MOSFET, and b) of a 280 nm wide MOSFET?

Exercise 2.4. In the "regions of operation" diagram in Fig. 1.7, what would be the equations for the borderlines between the different regions?

Exercise 2.5. Draw a similar "regions of operation" diagram for a p-channel MOSFET!

Exercise 2.6. The model parameters, k and V_T, for a certain MOSFET technology are given by k=900 µA/V^2 and threshold voltage V_T=0.30 V.

a. Calculate the gate voltage overdrive V_{GT} if the supply voltage is 1.2 V?
b. Calculate the saturation current, I_{DSAT}, for $V_{GS}=V_{DD}$!
c. Calculate the saturation voltage, V_{DSAT}!

Exercise 2.7. Determine the gate voltage V_{ON}, where the subthreshold current model and the saturation current model are equal and their derivatives are equal as well! Mark this border line in the "regions of operation" diagram! The ideality factor is n=1.75 (and hence the subthreshold swing S=100 mV/decade).

Exercise 2.8. Determine I_{ON}/I_{OFF} for a 65 nm CMOS technology with n=1.6, V_T=0.28 V and V_{DD}=1.2 V!

Exercise 2.8. Determine V_T for a 28 nm CMOS process if I_{ON}/I_{OFF} >10^6 is required with n=1.6, and V_{DD}=0.9 V! Is V_T scaled by the same factor 1.33 as V_{DD} compared to the 65 nm process?