Home assignment 2

MCC092
Introduction to
Integrated Circuit Design

Chalmers University of Technology

2018-10-09
Power & adder
problems

Home assignment #2 Due Monday October 15 2018 @ 23.59 (midnight)

Task #1 Dynamic power – Tapered buffers for clock tree

Consider the tapered buffer you designed in prelab 4. In this task assume that the clock frequency in the clock tree is 500 MHz. Here we consider only the case when the resistances in the clock tree are set to 0.

a) Calculate the dynamic power of the clock tree capacitances themselves. (You calculated the total capacitance as part of prelab 4).
b) Calculate the dynamic power consumption of the tapered buffer itself, that is not including the clock tree capacitances.
c) Some students designed a tapered buffer with 10 stages and a tapering factor of 2.61. What is the dynamic power of that tapered buffer? What is the resulting delay for this buffer?
d) Calculate the area needed for the two tapered buffers, your own and the one with 10 stages. You can approximate the area with the transistor areas only.
e) Fill in the numbers in the table below (or make a copy). What conclusions can you draw?

	My own tapered buffer from prelab 3	A 10-stage tapered buffer with stage effort = 2.61	The load capacitances themselves (only dynamic power)
Delay			
Dynamic power			
Tapered buffer area (only transistor area)			

Task #2 Dynamic power – activity factors

When the dynamic power is to be computed for non-clock signals, we also have to consider the activity factors of the signals. The probability P_Y that the output of some basic 2- and 3-input logic gates is "1" is shown in Table 5.1 in Weste and Harris (repeated below). What if we needed also the probabilities that the outputs of the AOI21 and OAI21 gates are "ones", how could we calculate them? What would the resulting values be if we assume $P_A = P_B = P_C = 0.5$? What are the resulting activity factors for the gate outputs?

TABLE 5.1 Switching probabilities

Gate	P_Y
AND2	$P_A P_B$
AND3	$P_A P_B P_C$
OR2	$1 - \bar{P}_A \bar{P}_B$
NAND2	$1 - P_A P_B$
NOR2	$\bar{P}_A \bar{P}_B$
XOR2	$P_A \bar{P}_B + \bar{P}_A P_B$

Task #3 Static power – power gating

In Figure 5.24 in Weste & Harris (repeated below in Figure 1) a pMOS header switch for power gating is seen. Such a switch is used to turn off the static power consumption when a block is not in use. The header switch should be designed such that it does not cause too large an increase in the delay when the gated block is operating. Suppose the pMOS transistor has an ON resistance of 2.5 kΩ·µm and the block being gated has an equivalent ON current of 100 mA. V_{DD} is 1.2 V for our process, as ususal. In the figure four transistors are shown, but you can assume that you are calculating the width of one single transistor, that represents the total switch width, even though in practice the switch probably has to be implemented as multiple transistors.

a) How wide must the header transistor be to cause less than a 2% increase in the delay of the block when it is ON?
b) Assuming the pMOS gate capacitance is the same as in our 65 nm process what is the gate capacitance for the header switch?
c) How much energy is required to use the header switch once (that is, turn it on and off once)?

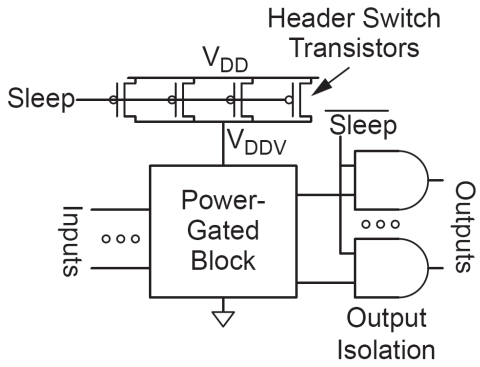

Figure 1. A power-gating arrangement with a pMOS header switch.

Task #4 Ripple-carry cell reconsidered

This task is a what if-task where you are to investigate the use of the pre-computed generate, G, and propagate P, signals in the carry chain from labs 2 and 3 on the schematics level as a complement to the in-class excel exercise you did on Tuesday October 9. Assume that we use our usual 65-nm CMOS process.

a) What are the logical expressions for generate, G and propagate, P?

b) Write the logical expressions for c_{out} as a function of c_{in}, P and G. For completeness also write the function for the sum signal, even though we do not use it in the

c) Using the logical expression from b) to redraw your carry cell from labs 2 and 3, using the propagate, P, and, generate, G, signals, rather than input bits A and B.

d) From the schematics drawn in c) calculate the logical effort for carry gate's c_{in} signal and the parasitic delay, p, for the carry gate.

e) Consider the case where there is an inverter between each carry cell. Derive the inverter size, relative to the carry gate c_{in} input capacitance, for minimum delay.

f) With the scaling of the inverter you derived in task d), what is the resulting delay for the carry chain in a 16-bit adder?

Task #5 The Dot operator or PG logic

Task 4 was about using P and G signals in ripple-carry adder. As a preparation for the adder exercise on October 16 you are also to investigate how P and G signals can be computed for more than one bit; that is not only for one pair of A and B bits at the time.

Consider the case when you have two pairs of consecutive A and B bits: A_{i+1} and B_{i+1} and A_i and B_i. Assume that we have pre-computed P_{i+1}, G_{i+1} and G_i, P_i using the logic functions you derived in task 4 a).

a) What is the logical expression for computing the propagate signal for the pair of inputs from the bitwise P and G signals? This so-called block propagate signal is usually denoted $P_{i:j}$ in the general case where i and j are any bit indices (as long as $i \geq j$). Here we have the case $P_{i+1:i}$.

b) What is the logical expression for computing the generate signal in a similar way as for the propagate signal in task a). That is the block generate signal $G_{i+1:i}$.

c) Draw the transistor-level schematic for the cell needed to compute the G signal in task b).

d) In a) and b) you showed how pairwise P and G signals are computed. Suppose you have computed these two pairwise signals for pairs i+3:i+2 and i+1:i. What are now the logical functions needed for combining these "pair signals" so that you as a result get $P_{i+3:i}$ and $G_{i+3:i}$.

Read page 436, section 11.2.2.2 in Weste and Harris carefully when you solve this problem. Chapter 11 of the Weste and Harris book can be downloaded from cmosvlsi.com. Look under "Look inside" in the menu to the left.