Prelab assignment
Lab 1

MCC092
Introduction to Integrated Circuit Design

Chalmers University of Technology

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2018

Pre-lab assignment introduction

About pre-lab assignments to the Cadence hands-on laboratory exercises

This course comprises a series of four lab exercises where you are introduced to some of the tools in the Cadence Electronic design automation (EDA) toolbox. The first lab is an introduction where you will design and simulate a CMOS inverter. You will investigate the inverter both statically (voltage-transfer curve) and dynamically (delay). The two following labs make up the core of the lab series; in these two labs you will design and verify a ripple-carry cell that could be use in a standard-cell library. In the fourth lab you will investigate some issues related to the on-chip wiring.

The design flow at the circuit level comprises the following steps:

- schematic entry and circuit simulation
- layout, design rule checking (DRC) and layout-versus-schematic (LVS) verification

For each lab there is a pre-lab assignment that you must solve and hand in prior to the in-lab session. These solutions are due in PingPong Friday at 1PM the week before the lab sessions take place.

Prelab assignment 1 due Friday September 14 2018 @ 1 PM

Pre-lab assignment to lab 1, the inverter lab

In this pre-lab assignment you shall calculate some values by hand so that you can compare these values with those you get in the much more detailed simulations you will run in the lab session. You shall also draw a couple of circuit diagrams so that you have thought them through before the in-lab session.

Task #1: **Getting to know Cadence**

Read the EESD Cadence crib sheet, except for section 8 on layout. (The crib sheet is available on the MCC092 PingPong page under `Documents -> Labs and EDA tools`).

Task #2: CMOS inverter cell schematics

Draw the circuit schematics for a CMOS inverter cell as it is to be entered in Cadence. In Cadence all transistors have four terminals (source, drain, gate and bulk). You must indicate how the bulk terminals should be connected for all transistors. Symbols for connection to global V_{DD} and GND are available inside a cell.

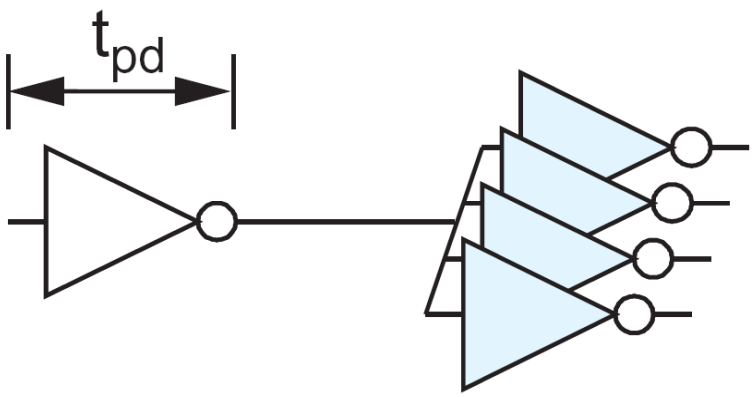

Figure 1: The fanout-of-four (FO4) setup with five identical inverters. (Figure from Weste & Harris).

Task #3: FO4 inverter delay for the standard-cell X4 drive-strength inverter

In all labs you will use components from a particular 65 nm CMOS process. There are several different types of transistors in this process. You will always use MOS transistors of the type "`svtlp`" which stands for "standard V_T, low power", where "V_T " stands for threshold voltage. In Cadence, the n-channel transistors you use will all have the type `nsvtlp` and the p-channel transistors the type `psvtlp`. According to the manufacturer of the CMOS process, the maximum current that these "`svtlp`" MOS transistors can deliver or sink for a gate-source voltage equal to V_{DD}, is 600 μA/μm for the n-channel transistors, and 300 μA/μm for the p-channel transistors. Furthermore, the gate-oxide capacitance, C_{ox}, is 20 fF/μm^2 for both pMOS and nMOS transistors. For both nMOS and pMOS transistors the parasitic drain capacitance is approximately 80% of the transistor gate capacitance. The supply voltage, V_{DD}, is 1.2 V.

In our digital gates all transistors have the minimum transistor length, that is L= 0.06 μm (60 nm), but the transistors widths vary among gates. In the standard-cell library, for which you are going to design your digital cells, the most narrow nMOS transistors used have the transistor widths W_n = 0.2 μm, and the corresponding pMOS transistors have the widths W_p = 0.4 μm. These widths correspond to the drive strength X2 (the unit-inverter strength, X1, is never used in

this library). Your inverter is to have the drive strength X4; that is, it should be twice as strong as the X2 inverter. What transistor widths should you use for the nMOS and the pMOS transistors in the X4 inverter?

Use the information about the 65 nm process supplied above to calculate the expected fan-out-of-four (FO4) propagation delay for the standard-cell inverter with these X4 transistor widths; in the FO4 setup one assumes that one cell is connected to four similar cells (see Figure 1). In most texts this delay is just abbreviated as the FO4 delay, but more properly is should be called t_{pdFO4}.

There are two different cases for t_{pdFO4}. You should calculate both the FO4 fall and rise delays (t_{pdfFO4} and t_{pdrFO4})[1]. Does the scaling used in this cell library (that is, the one where the pMOS transistors are twice as wide as the nMOS transistors) make the falling and rising FO4 delays the same? If not, how could the pMOS scaling be changed to make them the same?

Task #4: Static characterization of the CMOS inverter – expected values

In the 65 nm process the transistors have the threshold voltages V_{TN} = 0.29 V and V_{TP} =-0.27 V. V_{DD} is 1.2 V. What is the CMOS inverter switching voltage, V_{SW}, if we assume $k_n=k_p$?[2]

These are the expressions for ($V_{OL,\max}$, $V_{IH,\min}$) and ($V_{OH,\min}$, $V_{IL,\max}$), for a CMOS inverter with $k_n=k_p$.

$$\left(\begin{array}{l} V_{OH,\min} = V_{DD} - \dfrac{V_{DD} + V_{TP} - V_{TN}}{8} \\ V_{IL,\max} = V_{sw} - \dfrac{V_{DD} + V_{TP} - V_{TN}}{8} \end{array} \right), \left(\begin{array}{l} V_{OL,\max} = \dfrac{V_{DD} + V_{TP} - V_{TN}}{8} \\ V_{IH,\min} = V_{sw} + \dfrac{V_{DD} + V_{TP} - V_{TN}}{8} \end{array} \right)$$

Use the expressions above to derive the expressions for the low and high noise margins NM_L and NM_H. Calculate the two noise margins NM_L and NM_H for a CMOS inverter with $k_n=k_p$ in our 65-nm process.

Task #5: Static characterization of the CMOS inverter – finding the values from the VTC

From the circuit simulator output, how can you find the values for V_{SW}, V_{OH}, V_{IL}, V_{OL} and V_{IH} from the CMOS inverter voltage transfer curve? Draw a clear figure of the VTC where you show all five voltages and also explain how you would go about finding them. Hint: The voltage gain is the derivate of the VTC with respect to the input voltage in each point and there is an easy way to calculate this derivate in the circuit simulator; however, creating a butterfly diagram is not that easy.

Reading suggestions: Weste and Harris, chapter 3 on Delay, sections 3.1-3.3 and section 3.4.4 about drive and section 2.5.3 on noise margins.

[1] Note that these are not the same as the rise and fall times with which they are often confused. Refer to Figure 4.1 on page 141 in Weste and Harris for the definition of t_{pdr} and t_{pdf}.

[2] Note that Weste and Harris use β to denote the current factor instead of the much more common notation k which we use here. See Section 2.2, page 66, in Weste and Harris for the definition.