Prelab assignment
Lab 4

MCC092
Introduction to Integrated Circuit Design

Chalmers University of Technology

2017-07-06

2018

Prelab assignment #4: Due by Friday October 5 2018 @ 1PM

Pre-lab assignment for the fourth lab exercise

In lab 4, you will investigate the characteristics of a clock network in the form of a three-level H-tree. You will design a tapered buffer to drive the capacitive load of the H-tree, investigate the impact of the H-tree resistance and insert inverters in the H-tree to decrease the delay and improve the waveform shape. You will also investigate the effect of load mismatch which causes clock skew between the leaves of the clock network.

Task #1 The tools: In lab 4, you will use Spectre (the same simulation tool you have used from within Cadence in labs 1-3) as a stand-alone tool, from the Linux command line. You need to know how to write the input file and how to run the program from the command line and view the results in a tool called ViVa (which is the same tool you have used before inside Vivado). Therefore, you need to read through document "How to run a Spectre simulation for the command line" before you do this lab (see the prelab 4 assignment folder in PingPong). A very basic Spectre netlist file can look like the one below, which represents a CMOS inverter:

```
//Spectre needs to know we provide a file with Spectre syntax
simulator lang=spectre

//We define two transistor models using mos1 (=Level 1, Schichman-Hodges)
model n mos1 type=n vt0=0.7 kp=110u gamma=0.4 lambda=0.04 phi=0.7
model p mos1 type=p vt0=-0.7 kp=50u gamma=0.57 lambda=0.05 phi=0.8

//To avoid the hassle of redefining VDD everywhere, we use a global parameter
parameters supplyv=2

//We define two transistors using the p and n models defined above
xp1 ( out in vdd vdd ) p w=0.2u l=0.06u
xn1 ( out in 0 0 ) n w=0.1u l=0.06u

//We define an output load capacitance
cload ( out 0 ) capacitor c=2.5f

//We define the power supply voltage source to be "vdd"
vvdd ( vdd 0 ) vsource dc=supplyv

//We define the input voltage source to be "in"
vin ( in 0 ) vsource type=pulse val0=0 val1=supplyv delay=0 rise=1n fall=1n
width=4n period=10n

//We instruct Spectre to run a transient simulation
analysis1 tran step=0.1n stop=30n method=gear2only
```

For task #1, complete the following assignments:

a) Explain what a transient simulation is.

b) What are the parameters defined for the transistor models?

c) What is the significance of node 0?

d) Draw a schematic diagram of the circuit represented in the netlist above.

Further reading: Kenneth S. Kundert & Paul R. Gray: The Designer's guide to SPICE and Spectre. Kluwer Academic Publishers, 1995. Particularly Appendix B Spectre Netlist Language. This book is available as an e-book from the Chalmers library. Just type "Kenneth Kundert" in

the search box at www.lib.chalmers.se and it shows up as the second hit. Appendix B is in the "Back matter" part of the book.

Chapter 8 in W&H is about SPICE. The SPICE level 1 MOS model is described in section 8.3.1.

The SPICE tutorial in W&H section 8.2.1-8.2.4 explains the parts of a SPICE file; these are the same in a SPECTRE file although the syntax differs a bit.

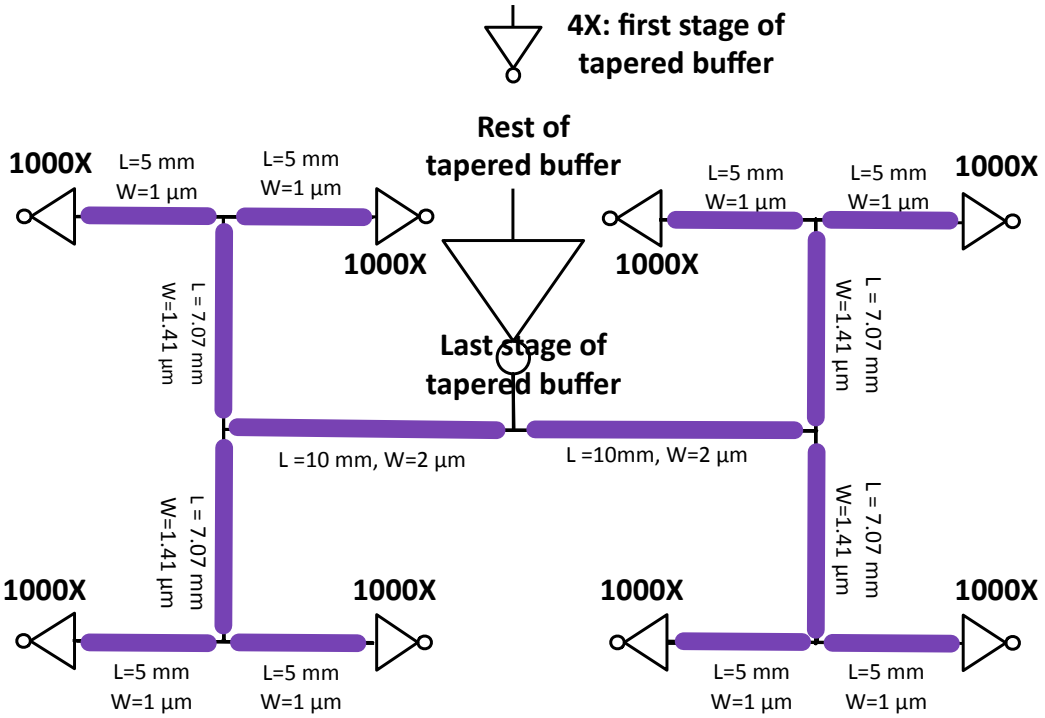

Figure 1: The H-tree with loading inverters at the leaves and a tapered buffer to drive the entire tree. The wire lengths are correct as stated above. The wires are very long.

Task #2 The lab Read through the lab memo for the lab, which is available on the course PingPong page.

Task #3 The Spectre netlist file To prepare for the lab you will need to write one of the required input netlist files in advance. Since a spectre input file is a text file, you can use any text editor to create and edit the file.

Download the template file called `template-spectreinputfile-2018.scs` from the prelab 4 assignment in PingPong:

- Rename it so that is has your name in the filename.
- Add the values for the parameters in the file (the places where it says `ADD VALUE`) that you can deduce from Figure 1.
- Also, add the netlist part with the circuit description of the H tree with non-zero R and C. Each wire shown in Figure 1 is to be explicitly modelled as one π link. Use a naming convention for the circuit nodes that makes is easy to understand which circuit node is which when using the result browser.

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You are to submit this text file separately, but before you do that you need to add some more lines to your file, which will be exaplained in tasks below. At each bullet point you need to add things to your file!

Task #4 The capacitances of the H tree Calculate the total capacitance of the H tree including the loading inverters at the leaves. In this task you should assume that the sheet resistance in the metal layer is 0, that is R_{SH} (called $R_{\square}$ in W&H) = 0 Ω/□, and that the capacitance of the wires is 0.2 fF/μm length for widths of 1 μm to 2 μm (see Figure 6.12 in W&H for a justification of this assumption). So, in this calculation all capacitance of the wires and the input capacitances of the inverters at the leaves are connected to one circuit node.

Suggested reading: Weste and Harris section 6.2.2 Capacitance.

Task #5 Design of the tapered buffer Design a scaled chain of inverters, that is, a so-called tapered buffer, to drive the capacitive load you calculated in task #2, aiming for as low a delay as possible. The first inverter should have 4X scaling. The scaling factor in each stage should be the same; it does not have to be an integer. Calculate the resulting delay with your tapered buffer loaded by the H-tree capacitance calculated in task #2. Also calculate the delay between successive stages in the tapered buffer.

- Add the netlist for your tapered buffer to your Spectre input file.

Tip: Since the sensitivity of the delay to the number of stages is quite low, see Figure 4.35 in W&H, is it a good idea to use a stage effort that is a bit higher than the optimum one and have fewer inverters. That way, you will save both chip area and energy. We do not recommend a stage effort higher than six though.

Suggested reading: Weste & Harris: Section 4.5.2 Choosing the best number of stages.

Task #6 The resistances (and capacitances) of the H-tree Now assume that the sheet resistance in the metal layer of the H-tree is non-zero: R_{SH} (called $R_{\square}$ in W&H) = 0.01 Ω/□ and that the capacitance of the wires is still 0.2 fF/μm per length (this means you can reuse your capacitance results from task #2). The widths of the wire segments are the ones shown in Figure 1. Calculate the value of the resistances for the wires segments at the three levels of the tree. Draw a figure of the H tree with the calculated resistances and capacitances and the load capacitances at the leaves shown clearly.

- Modify your spectre input file so that the resistances and capacitances of the H tree have the values you calculated in this task.

Suggested reading: Weste and Harris section 6.2.1 Resistance.

Task #7 Delay of the H tree with capacitance and resistance when driven by the tapered buffer Use the Elmore delay method to calculate the delay from the last inverter of your tapered buffer to one of the H-tree leaves, with the resistances and capacitances in the H tree that were the result from task #5. Draw a figure of the tree with one π link for each wire segment.

Tip 1: You can use the usual method with Elmore delay and the impact of branches to solve this problem. However, since the tree is fully symmetrical the delay to each leaf is the same, and it is possible to collapse the tree, so that two branches in parallel with capacitance R and C will yield one branch with R/2 and 2C. If you use this simplification there will not be any branches to consider, so it may be an easier calculation for you to perform.

Tip 2: Do not multiply with the factor 0.7 until at the very end of your calculation. It just obfuscates the calculations.

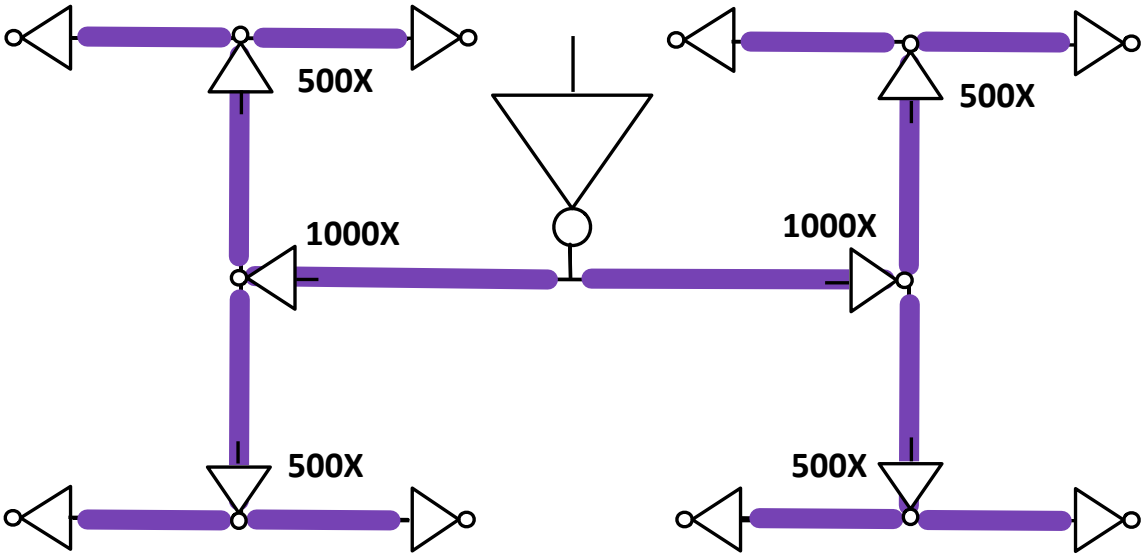

Figure 2: The H tree with added inverters. The tapered buffer should remain the same. Only the last stage of the tapered buffer is shown.

Task #8 Delay with inverters in the H tree driven by tapered buffer To decrease the delay, make the delay less sensitive to the load capacitance at the leaves, and make the transitions at the leaves more rapid we introduce inverters in the H tree. The inverters are to be placed as shown in Figure 2, which also shows the sizes of the inverters. Calculate the delay from the last inverter in your tapered buffer to one of the leaves for the tree shown in Figure 2. Note: For simplicity you are to keep the tapered buffer as it is, even though it probably is a bit overdesigned in this situati