MCC092 Integrated Circuit Design: Lab 3

Layout Entry and Verification for Ripple Carry Cell

Version 2018-10-01

2012-2018 (65 nm CMOS): Kasyab Subramaniyan, Stavros Giannakopoulos,
Per Larsson-Edefors and Lena Peterson
2008-2011 (130 nm CMOS): Goran Čengić, Lars Svensson,
Simon Kristiansson and Lena Peterson
Chalmers University of Technology

Contents

1 Lab Purpose

While the previous two labs were about schematic design and verification, this third lab is about the actual layout of the schematic cell. This layout is essential during design of digital circuits since it provides the blueprint for fabrication and since it allows accurate estimation of parasitic properties of wiring. In this lab, however, we will only perform the first steps of layout, i.e., drawing of layout, design rule checks (DRCs), and layout-vs-schematic (LVS) verification.

2 Pre-Lab Assignments

You will find the pre-lab assignment in a separate document available from the course home page in PingPong. You can find it most easily under the assignment called **Pre-lab preparation for lab 3**. This is also where you are to submit your solution to the pre-lab assignment. Note that even though you work in pairs in the lab you are to submit you own individual solution.

At the beginning of the lab you will get your pre-lab solution back with feedback from the teachers. Before you go ahead with the in-lab tasks, you should correct any mistakes you have made in the pre-lab assignment.

3 Lab Goal

During the lab you will carry out the instructions in this lab memo and show the results to the lab TA. If you do not manage to finish on time, you have to finish on your own and show the printed results to the lab TA at a later time (for example at the next lab session). What you should show is:

- Layout of your 1-bit ripple-carry cell.
- Output from the Calibre DRC tool that shows no errors.
- Output from the Calibre LVS that shows correct match.

4 Introduction

In this lab, lab 3, you will learn how to create the physical description—the *layout*—of the 1-bit ripple-carry cell, whose transistor schematic was designed in the previous labs. As before, we will use the Cadence Virtuoso design platform (CV for short). In a semiconductor process technology, the physical description of a circuit consists of different mask layouts for each layer in the process. In a CMOS process technology, the combination of different layers will produce nMOS and pMOS transistors, transistor gates, metal interconnects, and contacts between different layers. For a more detailed description of CMOS fabrication process technologies, see the course book.

When we are finished with the cell layout, we must make sure that the *design rules* for the process technology are respected. This procedure is called "Design Rule Checking" (DRC). Furthermore, we must also ensure that the layout really is a description of the intended circuit schematic. This procedure is called "Layout Versus Schematic" (LVS). Both these verification steps are to a large extent automated and can be carried out with certain tools either inside the CV environment or outside, using point tools from, e.g., Mentor Graphics.

First, start CV in the same directory that you used in the previous labs.

- Log into `heffalump` using `VNC` just like you have done for the previous labs.
- `Start a terminal window.`
- `Move to the working directory you used last time and initiate and start CV:`

```
> cd $HOME/MCC092/cadence
> /usr/local/cad/course/MCC092/Y2018/stm065
```

Open the library you created in the previous lab using the **Library Manager**.

The next step is to copy the layout view of the template which you are to use for the layout of the `ripple1` cell that you designed in lab 2. Note that this standard-cell template comprises both the compound carry gate and the X4 inverter which could be connected at the carry-gate output or at its input.

The templates are located in the library and path:

`MCC092_templates  /usr/local/cad/course/MCC092/Y2018/MCC092_templates`

To be able to copy the templates from this library you first have to make it available from inside the Library manager, and then copy the templates from it to you own library. Follow these steps:

- In the Library manager go to **Edit→Library path**.
- In the **Library Path Editor** window add the name and path of the library you want to copy (see information above; the first entry is the library name, the second is the path).
- In the **Library Path Editor** window do **File → Save as** .
- In the **File Save...** window under Selection insist on using file name set to `cds.lib` and say that it is OK to overwrite when asked.
- Close the **Library Path Editor**.
- You are now back in the **Library Manager**. Copying a cellview is done using **Edit→Copy...**, or by right clicking on the `layout` view for, for example, the 1-bit ripple-carry cell. Make sure you use the library `MCC092_templates`.

- In the **Copy View** form, under `To` type in the name of your own library, i.e., `labs`, and give the cell name of, e.g., your ripple-carry 1-bit standard cell, i.e., `ripple1` if you named your cells as was indicated in lab 2.
- Click on **OK**.
- If the form **Copy Problems** shows up, first press **Overwrite All** and then **OK**.

5 Layout Work

The incomplete layout—the layout template—of the ripple-carry cell contains twelve transistors. Your task is to connect the transistors so that they make up your cell according to your pre-lab assignment.

Start the layout tool:

- In the **Library Manager**, select the `labs` library, then select the `layout` view for of the `ripple1` cell (Note! you should already have copied the layout template to this cellview in the previous step). Double click on it to initiate the layout editor.

Observe that the layout template has been prepared in the fashion of a standard cell. This means that you are not allowed to change the height of the cell—the standard-cell pitch—or the widths of the power rails.

The first thing to do here is to hit `[shift-F]` in order to view the full design hierarchy.

While completing the connections for your 1-bit ripple-carry cell you are to use `M1` (metal layer 1) as far as possible. It is acceptable to use `M2` in case it is not possible to complete the connections using only `M1`. However, note that if you use `M2` to complete the interconnections within the cell this may have implications later on when the cell is used by the ASIC place-and-route tools. What might these be?

You can find layout predefined for entire components and contacts in the library `cmos065`. However, in this lab you will rarely need to access these libraries explicitly.

Adding Wires

You are to connect the transistors according to your plan. You accomplish this by drawing `M1` and in some cases `PO` (polysilicon) interconnect to connect the transistors. The different layers are connected, when necessary, through contacts which you have to add explicitly when needed.

There are several different commands for drawing metal and other layers. In this lab you should mainly use the Rectangle command (shortcut `[r]`), and possibly in special cases the Path command (shortcut `[p]`). While in rectangle mode, in the lower text field in the layout window the text `Cmd: Rectangle` appears. In the lower field it says `Point at the first corner of the rectangle`. **To exit this mode, press** `[ESC]`**.** Some more information regarding other commands is available in the Cadence Crib Sheet, Section 8.3.

Until now, we have ignored the other window opened by CV. This window, named **Layers** (or Layers Window), is described further in the Cadence Crib Sheet, Section 8.2. The Layers contains a menu of all available layout layers, which are VERY many in this process technology. All drawn layout will be drawn in the layer currently selected in the **Layers**. Most of the layers are not of any interest to us in this lab, so we will begin by sticking to the layers marked `drawing` or `drw`.

- Make sure that layer `M1 drw` is selected, by left clicking on it in the **Layers**.
- If the **Layers** contains more than 10 layers you should tick the option **used** at the top of the **Layers**, to hide any unused layers.
- Create a rectangle by pressing `[r]` and selecting the first and second corner of the rectangle.
- You can resize existing rectangles by using the Stretch command (`[s]`).

You may find it hard to complete some wires, since the contacts may not be placed in a way that allows wires to be added according to your plan. You can move objects such as contacts by first marking them—to mark several, press down `[shift]` while you left click on one more object—and then moving them using the mouse. Another move alternative is to use the Move command: Press `[m]` and then mark the object you want to move. Now you can move the object to the desired position. Lastly you can use the align command `[a]` if you need two or more contacts to align.

If you need to rotate existing contacts, edit the contact properties (press `[q]`) and use `R90` for `'Rotation'`. If you need to copy contacts or rectangles, press `[c]`.

During the layout work, it is often necessary to zoom in or out of the layout. There are several commands available for this.

- Move around in your layout using the arrow keys. Zoom in using the shortcut `[z]` and then choosing the area which to zoom into by left clicking the first corner of the zoom area rectangle, and then left clicking the second corner of the zoom area rectangle.
- Zoom out using the shortcut `[shift-z]`.
- If you like, you can always fit the entire layout on the screen (`[f]`).

A process technology requires the geometric shapes in a layout to fulfill certain minimum dimensions. This can be hard to ensure without help. Fortunately, you can add rulers to the layout window. These rulers are not part of the layout, so they are not saved when you close your work.

- Go into ruler-mode with the command **Tools→Create ruler** or by `[k]`.
- Add some rulers in your layout. Convince yourself that some of your `M1` interconnects are not too close according to the design rules.
- Leave the ruler mode by `[ESC]`.

- All rulers are removed by [shift-k].

The Delete command **Edit→Delete** ([DEL]) works like the one in the schematic tool: the command removes selected objects if there are any. Otherwise the tool enters the delete mode, where anything that is selected afterwards is removed.

With the commands that we now have gone through you can connect all transistors in the layout. After you are done, save your work using [F2]. **Be warned:** the undo command [u] can go back only up to the latest *save*.

Power Rails, Inputs and Outputs

The power supplies in the cell are commonly arranged by "rails" along two opposite edges of the cell. This way it is easy to feed several different cells by placing them next each other. In our standard cell template this is also the case.

In standard cells of this type, the routing to the cell is done in the upper metal layers. Using routing in M2 one can connect to any point in M1 inside the cell. However, each signal that is to be connected should only have to be connected to one point inside the standard cell, called a port. The inputs and outputs to the cell must be available even when the cell has been placed between other cells, in order to make power rail connections easier. Often this is most easily achieved by making the inputs and outputs in a metal layer *not* used for the power supplies.

- If necessary, add M1 interconnects that make sure the cell inputs only need to be connected to one port from the outside.

Pins and Labels

Next, we must specify which node in the layout corresponds to which pin in our circuit schematic from lab 2. "Shape pins" have a geometrical extension in a certain layer, so that automatic tools can use them for connecting different cells when placing the cells. A "Sym Pin" or symbolic pin is an instance of a pre-defined parameterized cell that represents a pin. In this lab we will use shape pins.

As in the schematic input, the pin name and type ("Direction" in schematic input but, inconsistently, "I/O Type" here) needs to be specified for each pin. Furthermore, we must specify "Access Direction". This parameter specifies from which direction a wire in the same layer can connect the pin. However, for standard cells that have their connection internally, this is not so important as for cells with connections at the edges.

- Issue the command **Create→Pin...** (shortcut [Ctrl-p]) in the layout window. The form **Create Symbolic Pin** appears.
- Under 'Mode' select manual. The 'Pin shape' of the pin should now be set to rectangle. Leave it as it is.

- Write the names for all the cells inputs (separated by a space) in the field `'Terminal names'`.
- Choose `'I/O Type'` to be `input`.
- Leave `'Access Direction'` as it is since we can access in any direction.
- Make sure that the box that says `'Create Label'` is checked.
- Click the `Options...` button next to `'Create Label'`. The form **Set Pin Label Text Style** form appears.
- Enter 0.2 for the `'Height'`.
- Ensure that `'Layer Name'` is set to `Same As Pin`.
- Ensure that `'Layer Purpose'` is set to `Pin`. Click on **OK**.
- In the **Layers** panel to the left Select the layer `M1 pin` by left clicking on it.
- Place the pin rectangle on top of the `M1` net which corresponds the input with the given name. *Note that the entire pin rectangle must be covered by the corresponding* `M1` *layer!* Place the text label as close to the center of the rectangle as possible by a final left click with the mouse.
- Repeat until all input terminals have been specified.
- Repeat the entire procedure with the output signals in your cell (which must be of `output` type).
- Save your work (with `[F2]`) when you are satisfied.

The physical representation of the cell is now complete. The cell also contains some information on how it may be connected when used together with (or as a part of) other cells.

Show your finished Layout to the TAs.

6 Verification of Layout

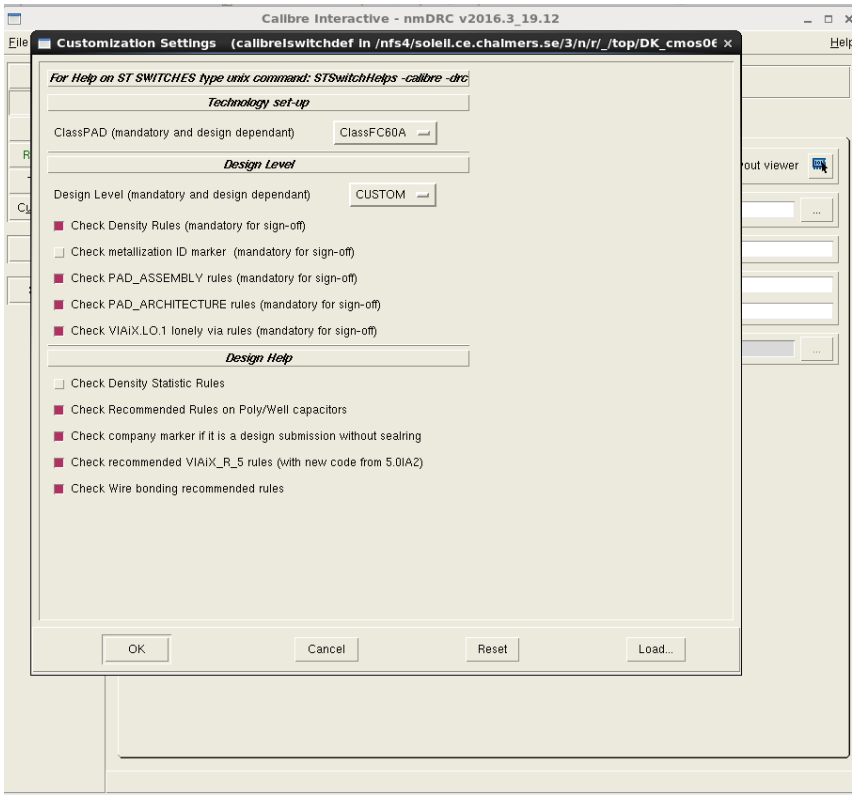
Verification of Geometry

During the layout work, we have tried to obey all the geometrical rules for the 65-nm process technology. However, without help from the tools it would be almost impossible to ensure that no mistakes have been made. Fortunately, it is possible to use automatic tools to check if any rules have been violated, commonly called DRC ("Design Rule Checking"). The tool used to perform DRC in these labs is Calibre-nmDRC from Mentor Graphics.

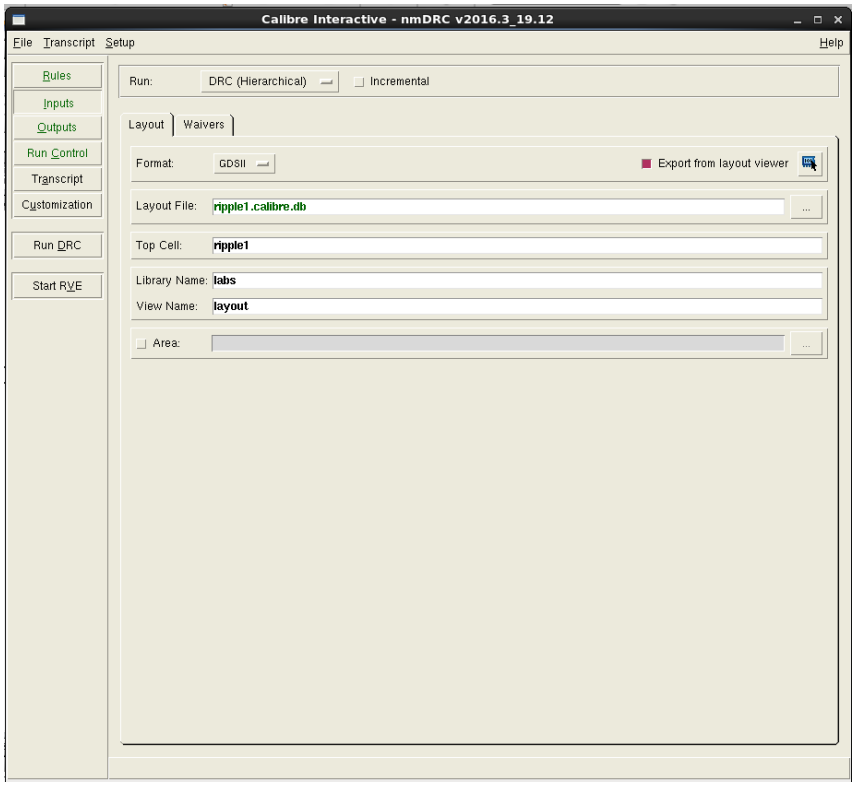
Invoking DRC can be accomplished from CV and its layout editor.

- Start Calibre from the layout editor window for the cell you going to check, using **Calibre→Run nmDRC**.
- In the pop-up window that then appears, click on **Run DK DRC**.

- After a few seconds a window called **Calibre Interactive - nmDRC** appears. Wait until another window titled **Customization Settings** also appears. See the image below for what to expect.

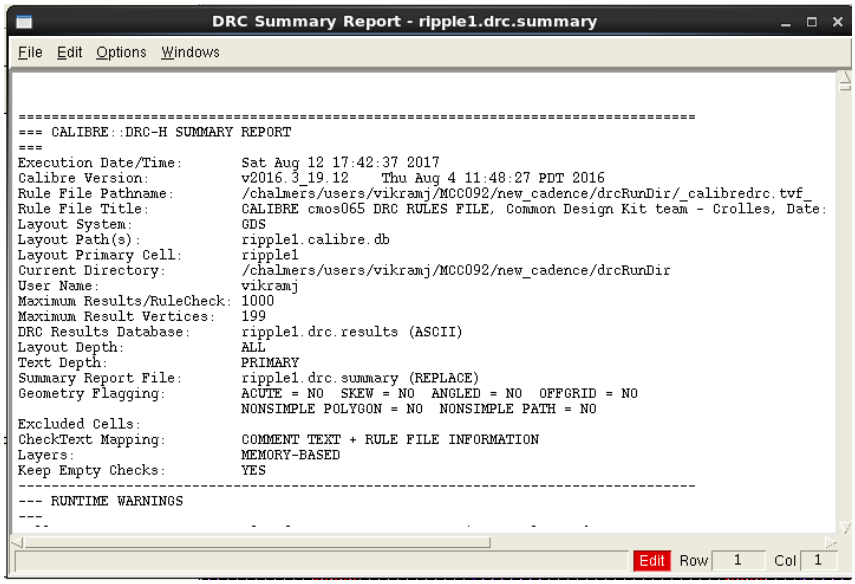


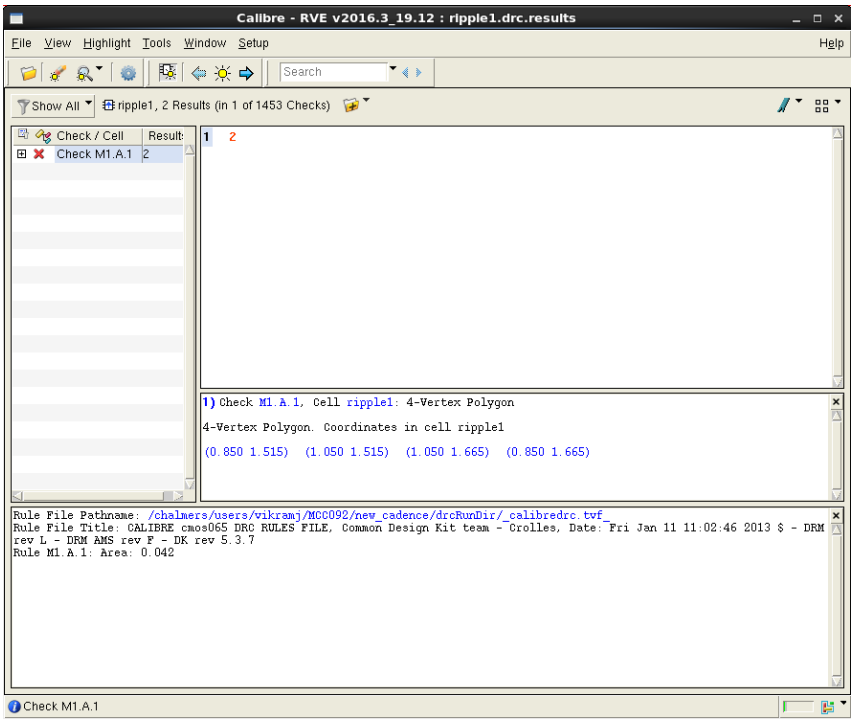
- In the **Customization Settings** window, uncheck the options:
  `Check Density Rules (mandatory for sign-off)`
  `Check VIAiX.LO.1 lonely via rules (mandatory for sign-off)`
  `Check company marker if it is a design submission without sealring`.
  Click **OK**.
- The first time DRC is invoked a **Question** box pops up asking if the directory where DRC is to be run should be created. Click **Yes**.
- In the **Calibre Interactive - nmDRC** window, the inputs tab is displayed by default (see image below). You may look at the other tabs on the left to explore the various options. No options need to be changed for this design.



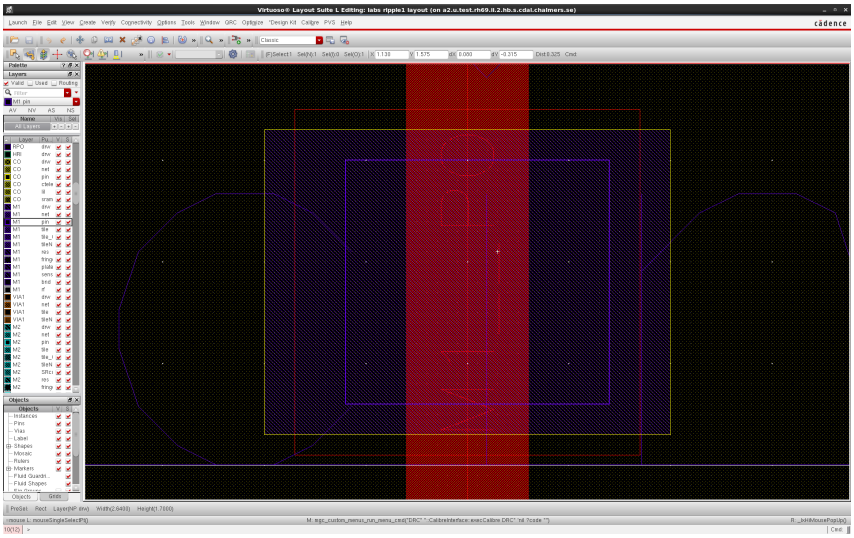
- Click the **Run DRC** button, at the left side of the window, to start the DRC process. If DRC is being run for the first time the netlist is extracted from the layout automatically. If DRC is being run incrementally, a pop up window asking if the existing netlist should be overwritten, appears. Choose **Yes**.

- Eventually two windows appear: The **DRC Summary Report** containing all the run statistics and the **Calibre - DRC RVE** window which shows the results of the DRC run. See the images below for what to expect.





- In the **Calibre - DRC RVE** window, choose **View** and uncheck the `Show empty checks` option if it is already checked.
- Errors appear sorted by the rule with a red box with a × in it and the number of failures for that particular rule. Passed checks are indicated by a green box with a ✓.
- Click the + sign at any failing check to display all the failures in the layout related to that check. Click a number (say 01) and then press the *H* button. The layout window zooms to the violating geometry. The **Calibre - DRC RVE** window contains the details of the rule and the minimum geometry for that run in the bottom panel. Below is an example of what it can look like when an error is displayed in the layout window:



- The layout window view may be refreshed using the shortcut `[Ctrl-r]`
- Fix the errors (or some of them at a time) and rerun the DRC until there are no errors left.
- Show your DRC-error free design to the TAs.

- Close all open windows. Choose **OK** for the **Confirm Exit** dialog box and **No** for **Save Settings** dialog box.

Schematic Comparisons

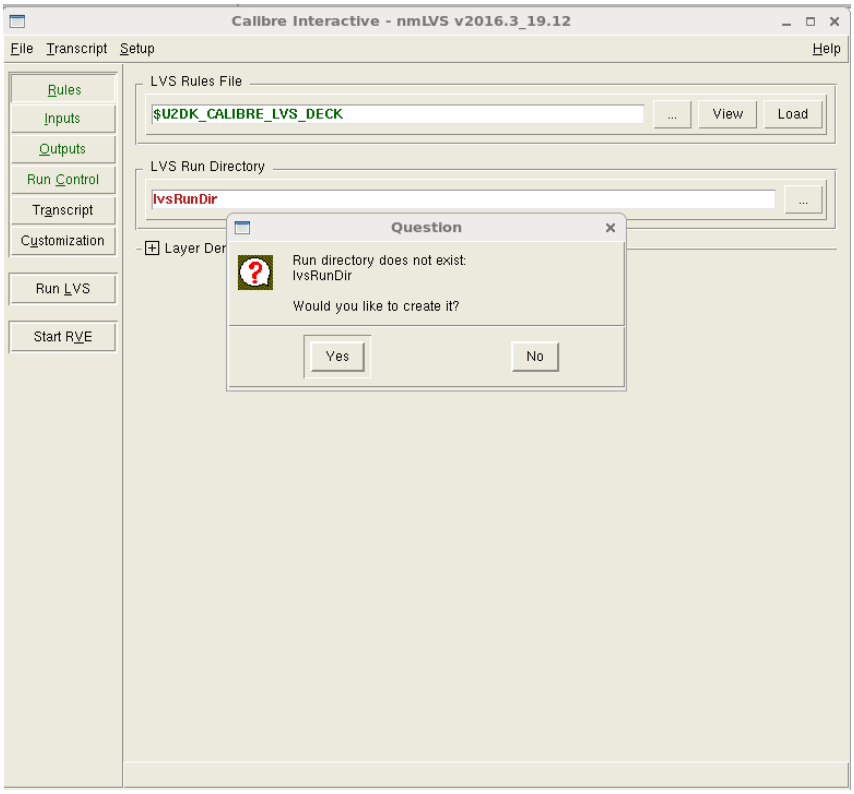
When the DRC no longer detects any errors, it is possible to manufacture the design. This means that the layout can be fabricated in the chosen process technology without any errors due to the fabrication steps. But, the absence of DRC errors does not imply that the layout will accomplish the intended function. We also have to verify that the layout corresponds to the circuit schematic implemented (and verified by simulation) in lab 2. This verification step is called LVS ("Layout Versus Schematic").

This process compares the netlist from the schematics with the netlist generated from the layout to see if they match. Note that the order of transistors matters, since it is the graphs corresponding to the two circuits that are compared, not their logical functions. So if you changed the order of the transistors from what you had in your schematics to get a better layout, you need to check that the ordering is the same in the schematics before you proceed.

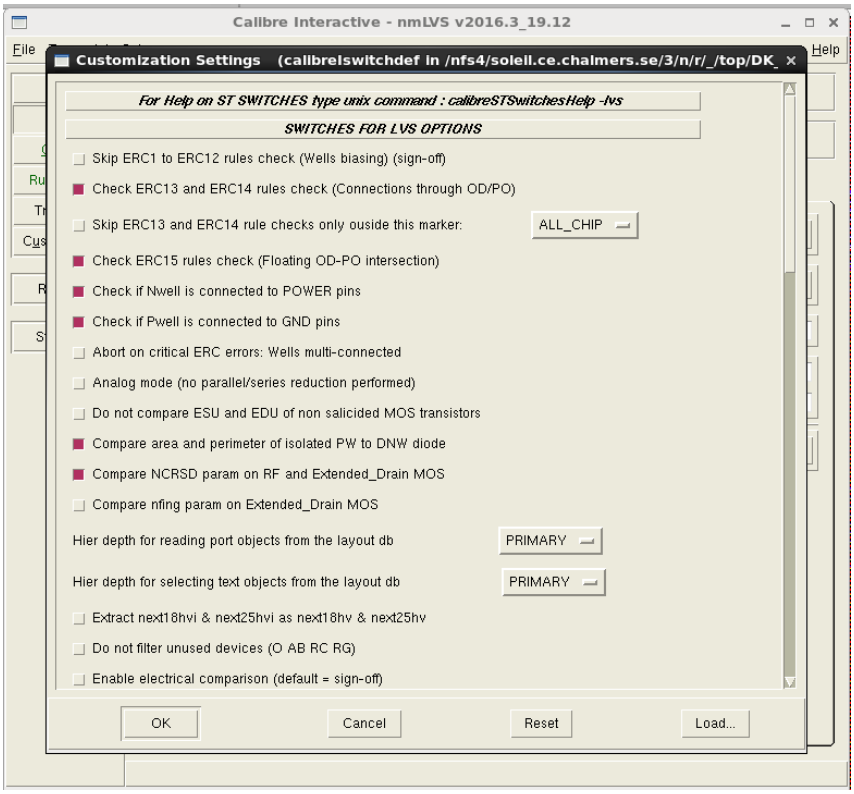
Before you start the LVS step also make sure that you have put labels and ports on all inputs in the layout of your ripple-carry cell. The power rails, vdd and gnd, are already taken care of in the template.

You will use Calibre-nmLVS from Mentor GRaphics to perform the LVS function in this lab.

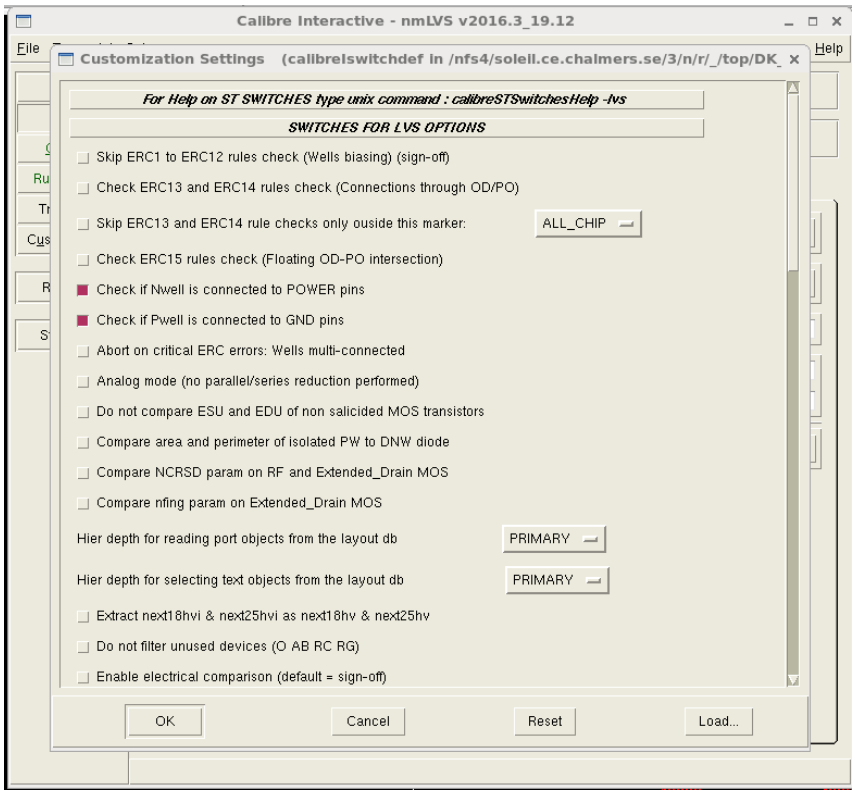
- Start Calibre from the layout editor window for the cell you going to check, using **Calibre→Run nmLVS**.
- After a few seconds a window called **Calibre Interactive - nmLVS** appears. See the image below. Wait until another window titled **Customization Settings** also appears.



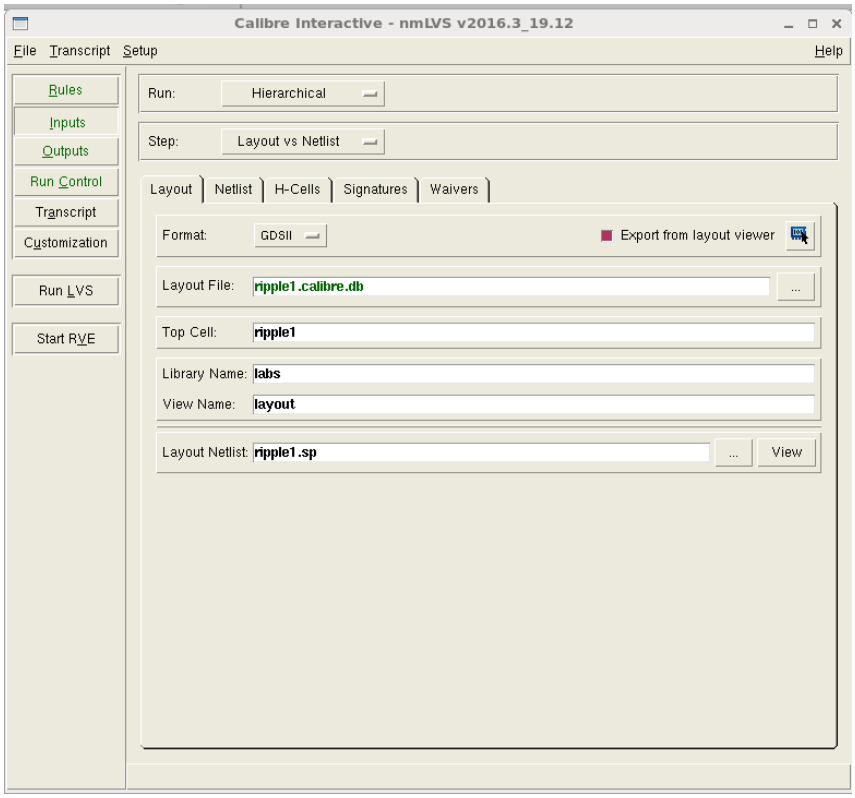
- The **Customization Settings** window appears and most likely looks as shown in the image below.



- Unckeck some options so that it looks as is shown below. Leave all the extraction options further down in the window as is. Click **OK**.



- The first time LVS is invoked a **Question** box pops-up asking if the directory where LVS is to be run should be created. Click on **Yes**.
- In the **Calibre Interactive - nmLVS** window, the inputs tab is displayed by default. Make sure that `Layout vs Netlist` is selected.

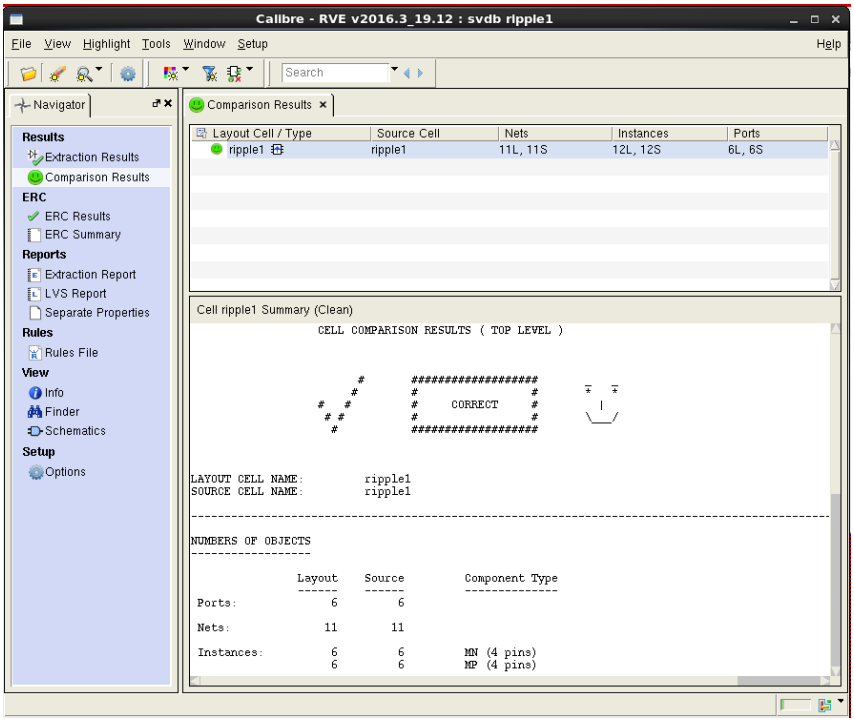


- You may look at the other tabs on the left to explore the various options. No other options

need to be changed for the current design.

- Click the **Run LVS** button to start the LVS process. If LVS is being run for the first time the netlists are extracted from the layout and schematic automatically. If LVS is being run incrementally, pop-up windows asking if the existing netlists should be overwritten, appear. Choose **Yes** for both.

- Eventually two windows appear: The **LVS Report File** containing all the run statistics and the **Calibre - LVS RVE** window which shows the results of the LVS run. Below is an image of how the **Calibre - LVS RVE** window looks when the LVS is performed sucessfully.



- In the **Calibre - LVS RVE** window check the results. If the designs don't match, drop down to the discrepancies by clicking on the + sign.

- Fix the errors (or some of them at a time) and rerun the LVS until there are no errors left.

- Show your LVS-error free design to the TAs.

- Close all open windows. Choose **OK** for the `Confirm Exit` dialog box and **No** for `Save Settings` dialog box.

7 Extra tasks

If you managed to go through the DRC or LVS process with no errors you can explore how an error shows up. For example, in the LVS process is it instructive to change the order of two inputs in the schematic, or change the width of one transistor, or move a bulk connection and see how the error is reported by the LVS tool.

8 The End

You have completed the layout of the 1-bit ripple-carry cell and ensured that it is manufacturable. You have also verified that your circuit schematic matches the netlist extracted from your layout.

It should be noted that the true circuit, represented by the layout, has some electrical properties that are not captured in the circuit schematic or in the simple extracted netlist. Specifically, the physical layout will have some "parasitic" elements, e.g., stray capacitances. To make sure that such parasitic circuit elements do not have a detrimental impact on the function and the performance of the circuit, there are extra design flow steps to extract all the parasitics components from the layout. In the interest of time, this lab series will however not cover these steps.