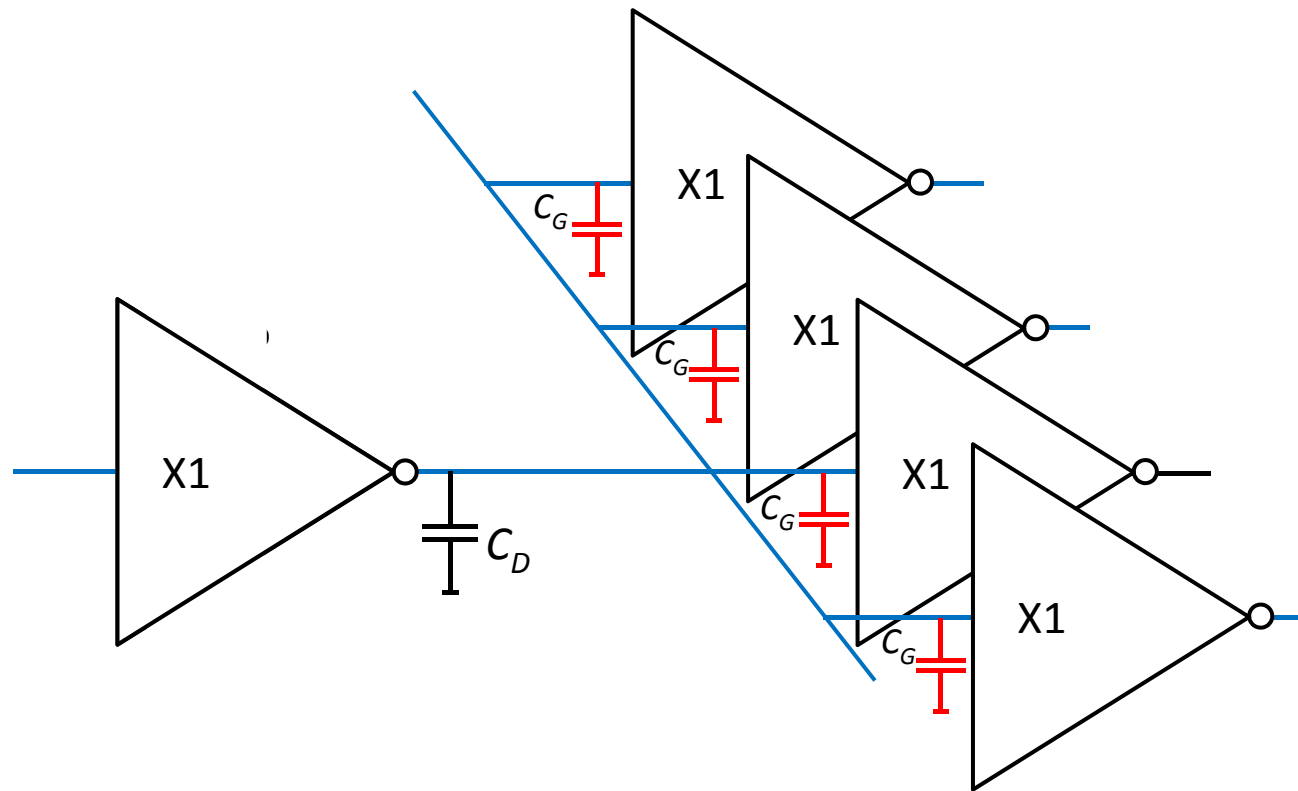# Lecture 4 follow-up
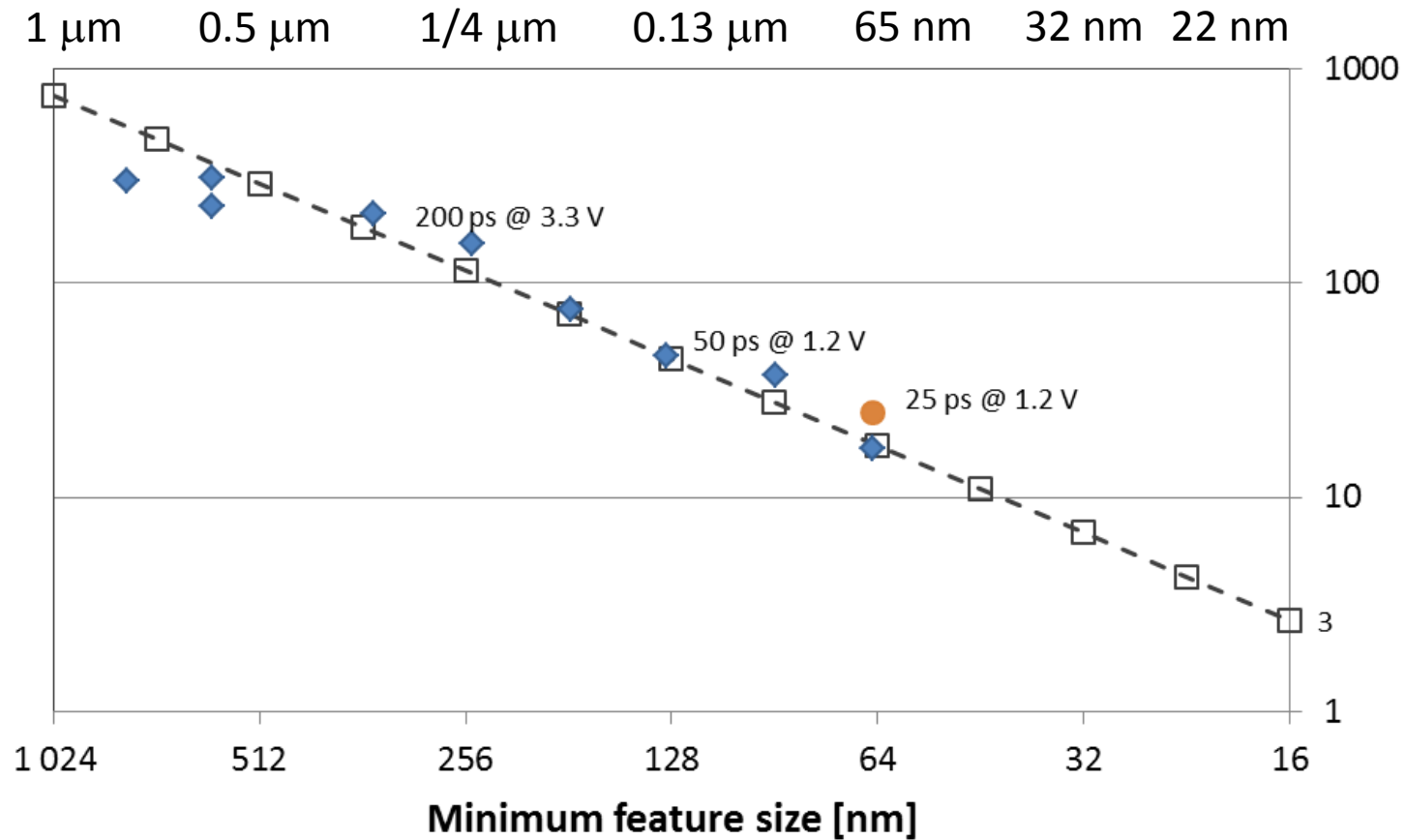# Tapered CMOS Inverter stages

Dynamic properties

Introduction

- In these set of slides some supplementary information and material for self studies is presented.
- The importance of the FO4 delay as 5tau is again high-lighted.
- An attempt to show values for tau vs. technology as measured by its minimum feature size (i.e. minimum channel length) is shown in the trend graph.
- A published comparison of different processor cycle time trends in terms of FO4 delays is shown.
- The tapered buffer is analyzed in detail in terms of path electrical effort H, and stage electrical effort h.
- A stage electrical effort, or fanout, of four is shown to be very close to the optimal solution for minimum delay.
- An H-tree clock distribution network is used to show how branching affects the fanout of a critical timing path. The path fanout, F, becomes the product of the path branching, B, and the path electrical effort, H!
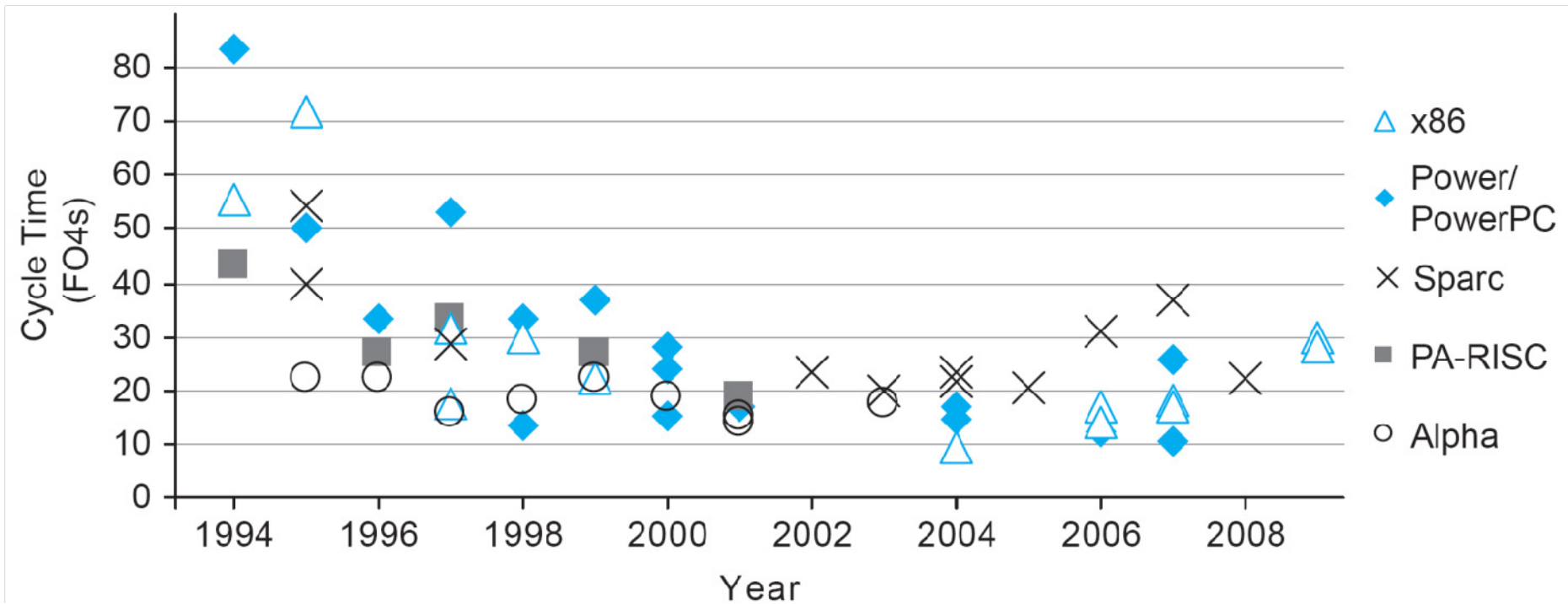- Conclusion $F=BH$ and $h=\sqrt[N]{F}$!

Inverter FO4 delay

The FO4 propagation delay becomes $t_{pd} = 0.7 R_{eff} \left(C_D + 4C_G \right) = \underbrace{0.7 R_{eff} C_G}_{\text{τau}} \left(p + 4 \right) = 5 \text{ ps} \times 5 = 25 \text{ ps}$

FO4 delay trends vs. feature size

Microprocessor cycle time trends

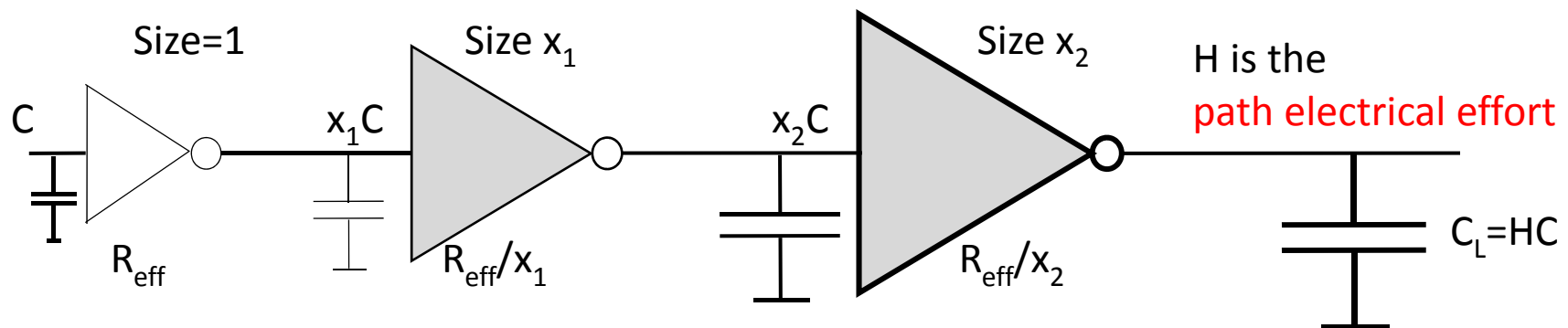*From Weste & Harris.*

The tapered buffer

Please note that H is the path electrical effort while h is the stage electrical effort.

Reference inverter . . .   and two inserted buffer inverters

Size=1   Size x_1 Size x_2

H is the path electrical effort

C x_1C x_2C $C_L=HC$

R_{eff} R_{eff}/x_1 R_{eff}/x_2

With two intermediate buffer inverters we obtain a normalized delay relative to tau:

$d=(p_{inv}+h_1)+(p_{inv}+h_2)+(p_{inv}+h_3)$

where we have defined the stage electrical efforts, or fanouts, h.

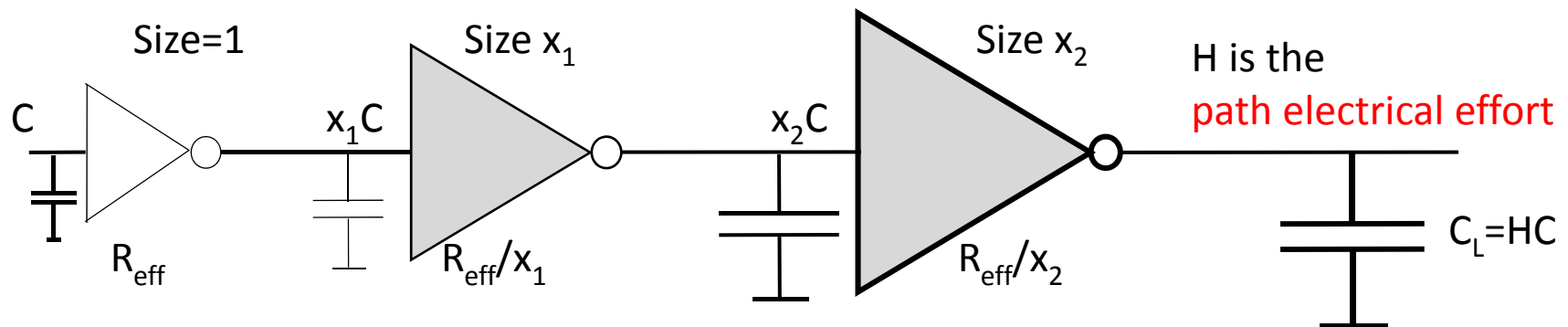Here $h_1=x_1$, $h_2=x_2/x_1$, and $h_3=x_3/x_2$).

Only h_1 and h_2 are independent variables, the third h_3 becomes $h_3=H/h_1h_2$.

TASK: Show that minimum delay is obtained for $h_1=h_2=h_2=h=\sqrt[3]{H}$ >>> $d=3(p_{inv}+\sqrt[3]{H})$

The tapered buffer

Please note that H is the path electrical effort while *h* is the stage electrical effort.

Reference inverter . . .   and two inserted buffer inverters

With two intermediate buffer inverters we obtain a normalized delay relative to tau:

$d = (p_{inv} + h_1) + (p_{inv} + h_2) + (p_{inv} + H/h_1 h_2)$.

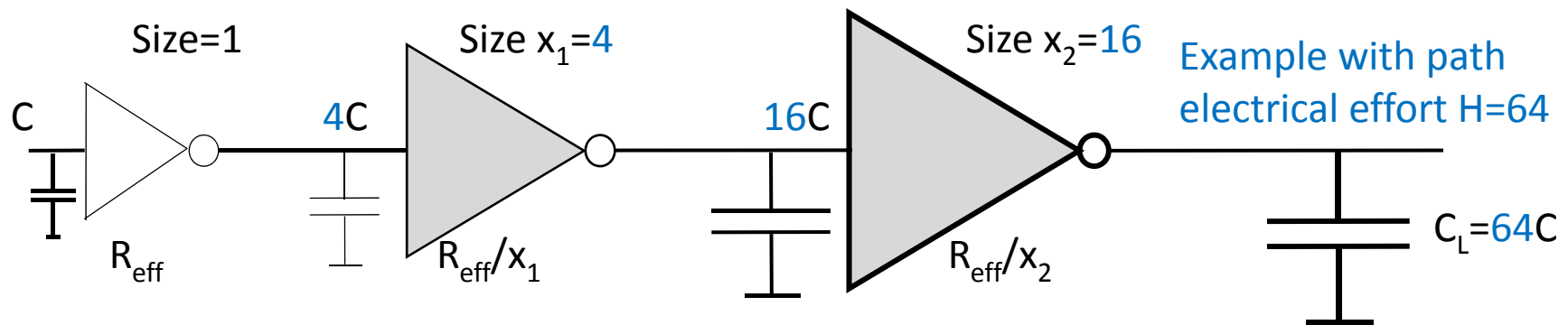Taking partial derivatives wrt h_1 and h_2 we obtain

$$\frac{d}{dh_1} d(h_1, h_2) = 1 - \frac{H}{h_1^2 h_2} = 0, \text{ and } \frac{d}{dh_2} d(h_1, h_2) = 1 - \frac{H}{h_1 h_2^2} = 0$$

$$\text{This yields } h = h_1 = h_2 \text{ and } H = h^3 \rightarrow h = \sqrt[3]{H}$$

The tapered buffer

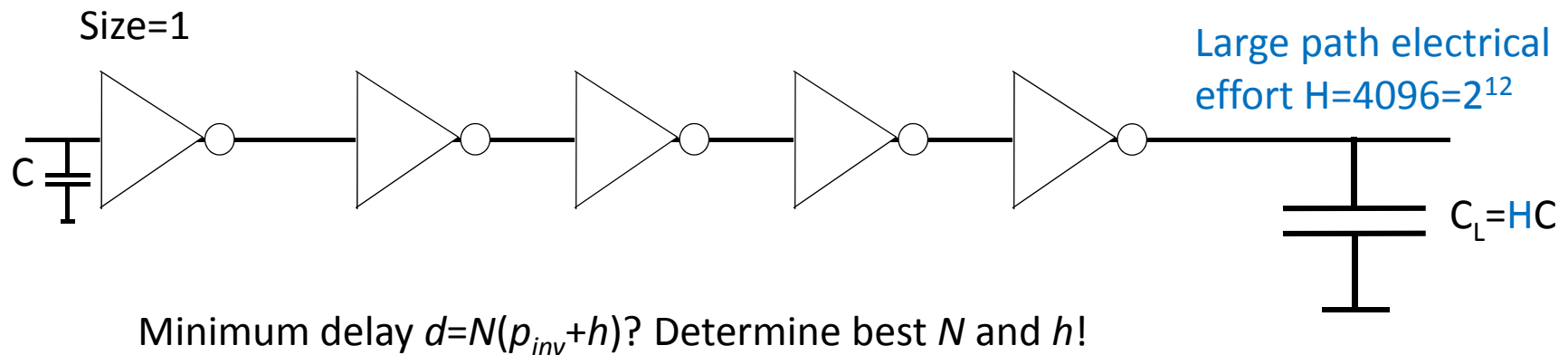Reference inverter . . .   and two inserted buffer inverters

Sharing the load equally between the inverters yields equal stage fanouts $h=\sqrt[3]{64}=4$

The total delay is then equal to 3 FO4 delays, i.e. 15tau=75 ps (assuming p_{inv}=1).

The Tapered Buffer

- What if the path electrical effort, for some reason, is very large, e.g. H=4096.

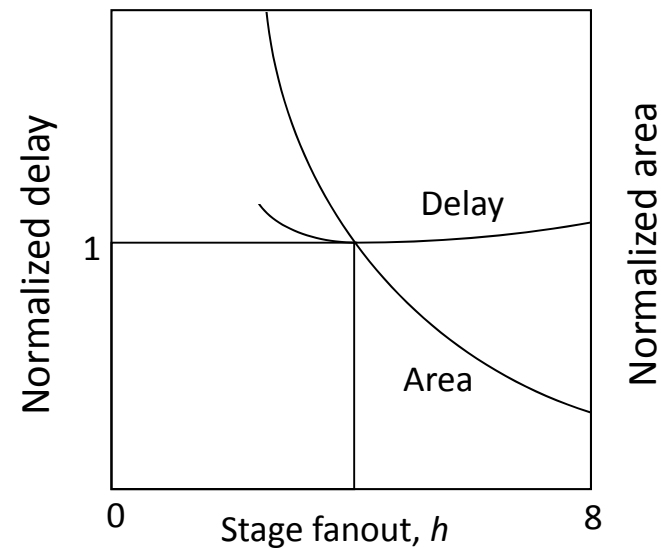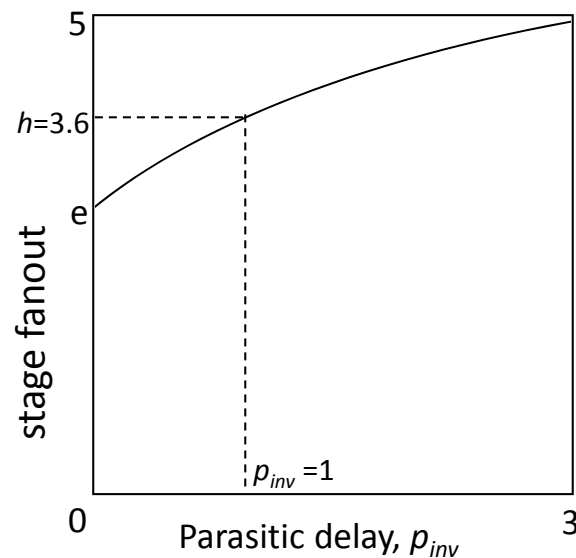- How many inverters, N, are needed to minimize the delay?

Size=1

Large path electrical effort $H=4096=2^{12}$

$C_L=HC$

C

Minimum delay $d=N(p_{inv}+h)$? Determine best N and h!

The Tapered Buffer

- Solving this problem we start by having accepted that minimum delay occurs when stage electrical efforts, *h*, are shared eqaually between the inverter stages.

- Hence propagation delay is given by $d = N(p_{inv} + h)$

- Furthermore, $h = \sqrt[N]{H}$, i.e. $H = h^N$.

- Taking natural logariths we obtain number of inverters $N = \dfrac{\ln H}{\ln h}$

- Rewrite delay equation $d = N(p_{inv} + h) = \dfrac{p_{inv} + h}{\ln h} \ln H$

- Looking for minimum delay by taking derivatives wrt *h*

- We obtain $\ln H \dfrac{\ln h - (p_{inv} + h)/h}{(\ln h)^2} = 0$, i.e. $\ln h = \dfrac{p_{inv} + h}{h}$

- Analytical solution only for $p_{inv}=0$, namely *h*=e=2.72

The Tapered Buffer

- For $p_{inv} \neq 0$ the equation has to be solved numerically

[Hedenstierna & Jeppson 1987]

For typical values of p_{inv} the optimum tapering factor is between 3.6 and 5. Typically a FO4!

Please, note that the propagation delay minimum is rather flat,
while total inverter area on the silicon decreases rapidly when larger stage fanout is used.
Silicon real estate (=cost) can be saved for relatively little loss of speed!
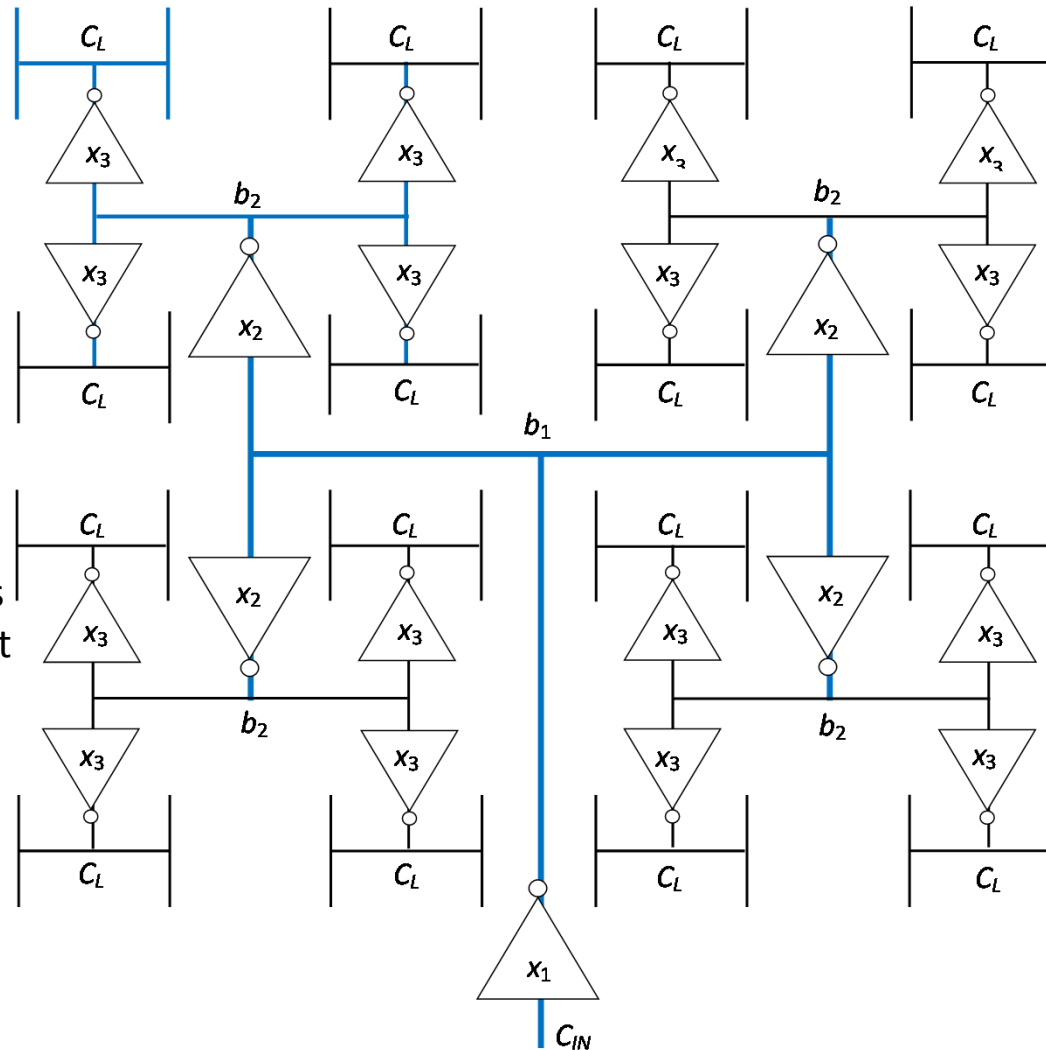
The Tapered Buffer

- So for a path electrical effort H=4096=4^6, minimum delay is obtained for N=6 inverters with a stage fanout of four!!

- Minimum normalized delay d=6(p_{inv}+4)=30, and t_{pd}=150 ps

- What if we choose N=4? That is h=8?

- What would be the propagation delay?

- Normalized delay d=4(p_{inv}+8)=36, and t_{pd}=180 ps.

- At the same time the inverter area would be reduced from

- A=1+4+16+64+256+1024=1365 to A=1+8+64+512=585 units. That is a reduction by more than 55%.

H-tree clock distribution

Problem: To distribute a clock signal across the chip area so that it arrives simultaneously to all chip corners, i.e no clock skew, and with sharp clock edges!
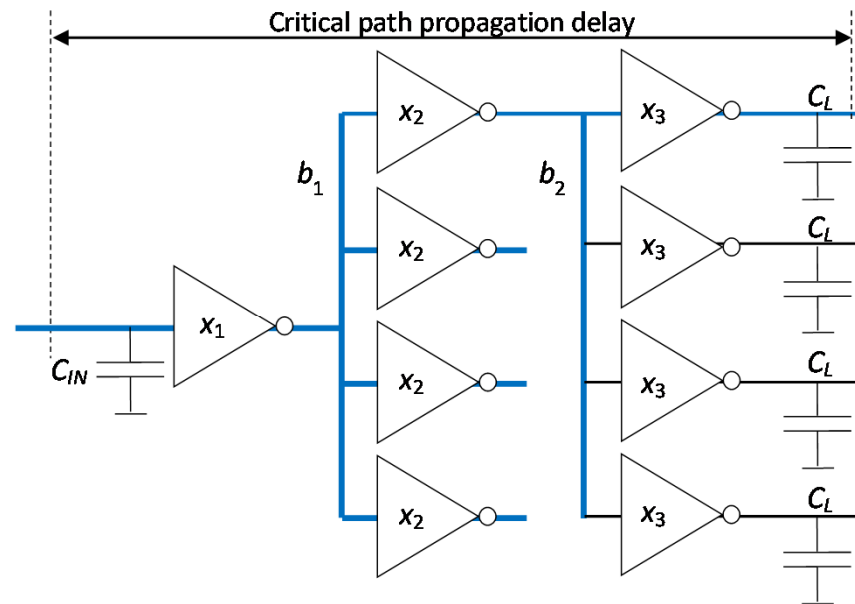
One approach is to use balanced H-trees!

The load capacitances C_L are due to the input capacitances of all clocked register cells.

H-tree clock distribution

- What is the electrical effort of the timing paths considering also the branching?

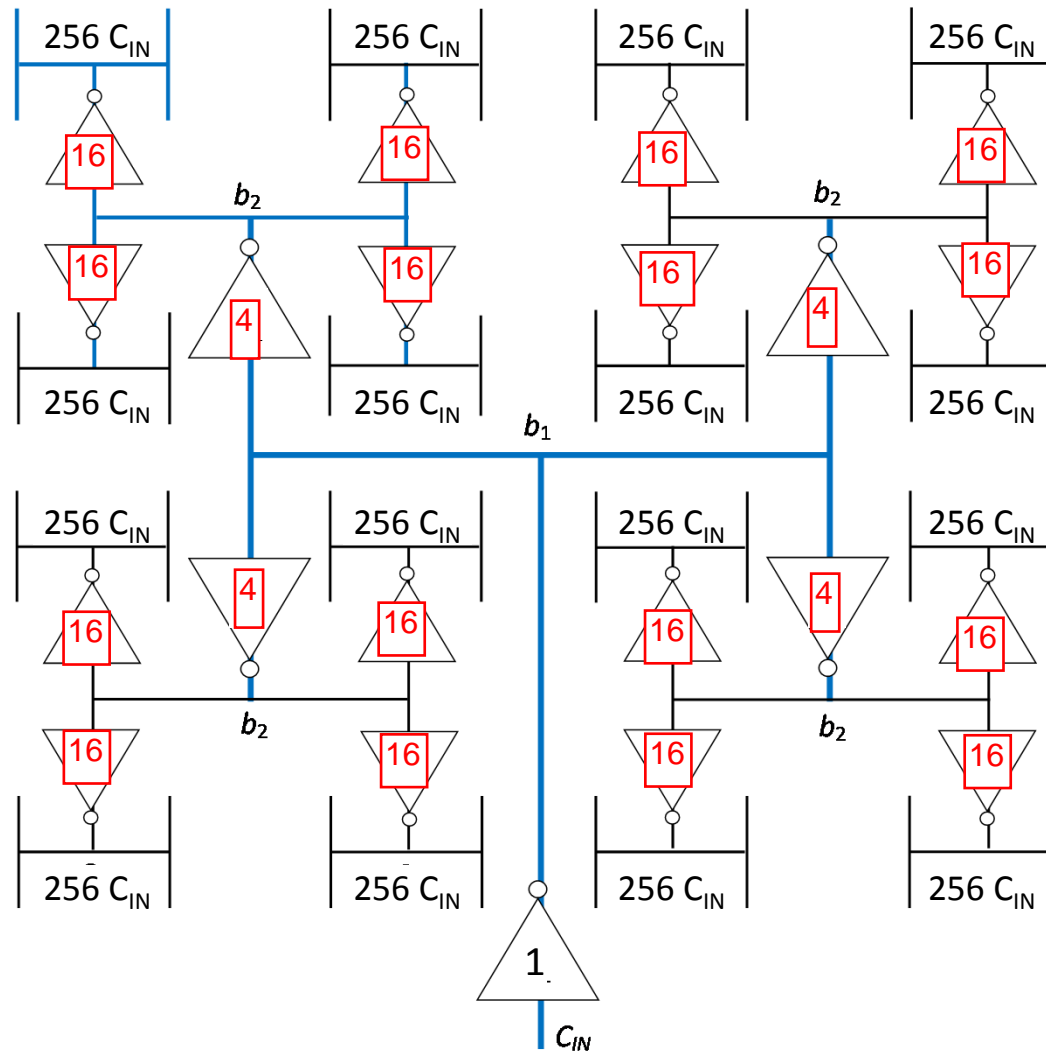- What sizes to choose for the inverters of the H-tree?

H-tree clock distribution

- As before, assume stage fanouts h_1, h_2, h_3.

- Path delay is then given by $d = \left(p_{inv} + h_1 \right) + \left(p_{inv} + h_2 \right) + \left(p_{inv} + h_3 \right)$

- How are stage efforts related considering the branching where the first inverter has a branching $b_1 = 4$ and the second stage a branching $b_2 = 4$?

- We have the following relationships: $h_1 = b_1 \dfrac{x_2}{x_1}, \; h_2 = b_2 \dfrac{x_3}{x_2}, \; h_3 = \dfrac{C_L}{\dfrac{x_3}{x_1} C_{IN}} = \dfrac{x_1}{x_3} H$

- Hence, $h_1 h_2 h_3 = b_1 \dfrac{x_2}{x_1} b_2 \dfrac{x_3}{x_2} \dfrac{x_1}{x_3} H = b_1 b_2 H$

- Now, let us introduce the path branching B = $b_1 b_2$!

- The path fanout is now F=BH, and stage fanout $h = \sqrt[3]{F}$.

- In an example with B=16 and H=256 we obtain F=4096=16^3.

Example solution for $C_L = 256\,C_{IN}$!

H-tree clock distribution

The sizes have been updated by Lena on 2017-10-23