# Wires & wire delay

Lecture 9 on Interconnect

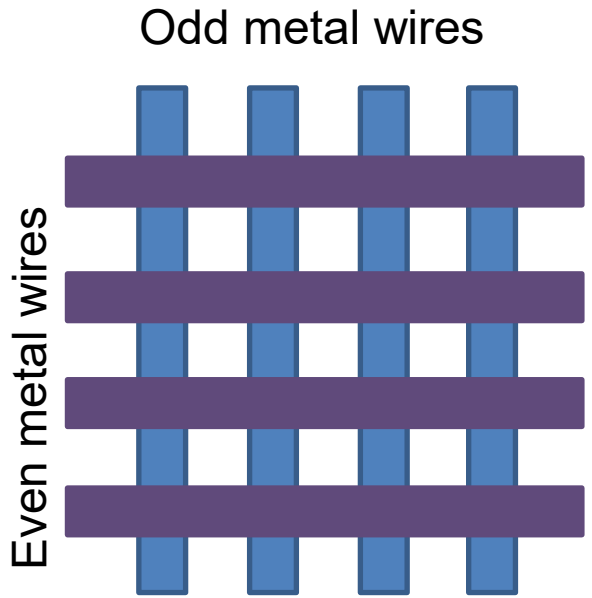
Tuesday September 27, 2017

# Outline

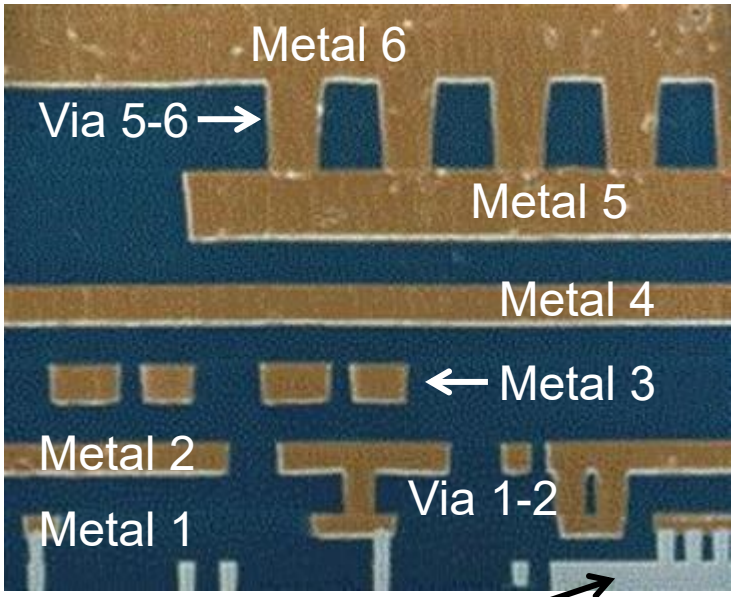
- Introduction
- Interconnect Modeling
  - Wire Resistance [sheet resistance in ohms per square]
  - Wire Capacitance
- Introducing a distributed wire RC $\pi$-model
- Estimating wire delay assuming a dominant RC time constant
- Inserting repeaters to keep wire lengths short
- Elmore delay model – a generalized model
- Handling wire branches
- Conclusions

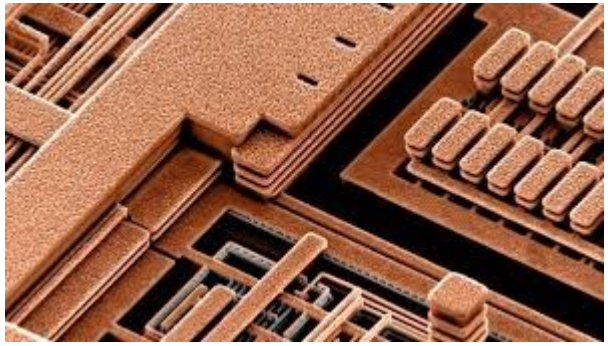
# Introduction

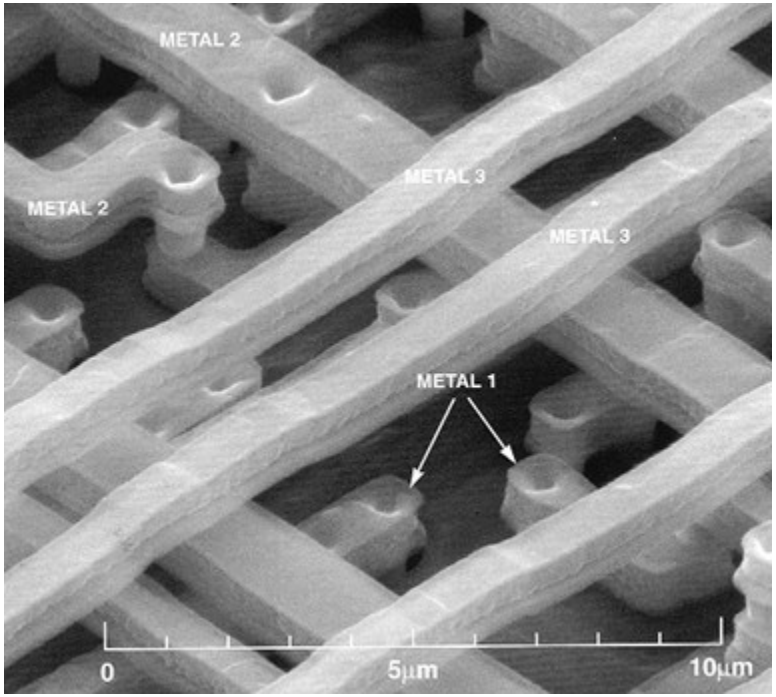
- Chips are mostly made of wires called *interconnect*
  - Transistors are little things under the wires
  - Many layers of wires
- Wires are as important as transistors
  - Speed
  - Power
  - Noise
- Alternating layers run orthogonally



# Modern interconnect



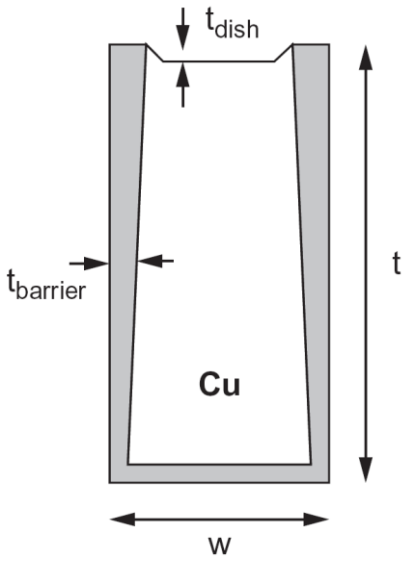





# Choice of metals

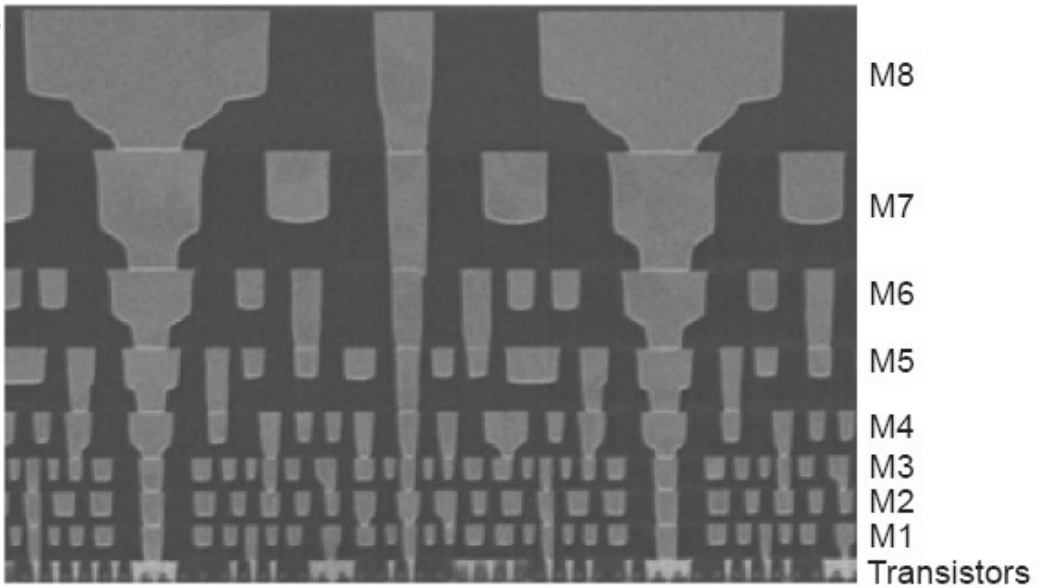
- Until 180 nm generation, most wires were aluminum
- Contemporary processes normally use copper
  - Cu atoms diffuse into silicon and damage FETs
  - Must be surrounded by a diffusion barrier

| Metal | Bulk resistivity (μΩ·cm) |
|---|---|
| Silver (Ag) | 1.6 |
| Copper (Cu) | 1.7 |
| Gold (Au) | 2.2 |
| Aluminum (Al) | 2.8 |
| Tungsten (W) | 5.3 |
| Titanium (Ti) | 43.0 |



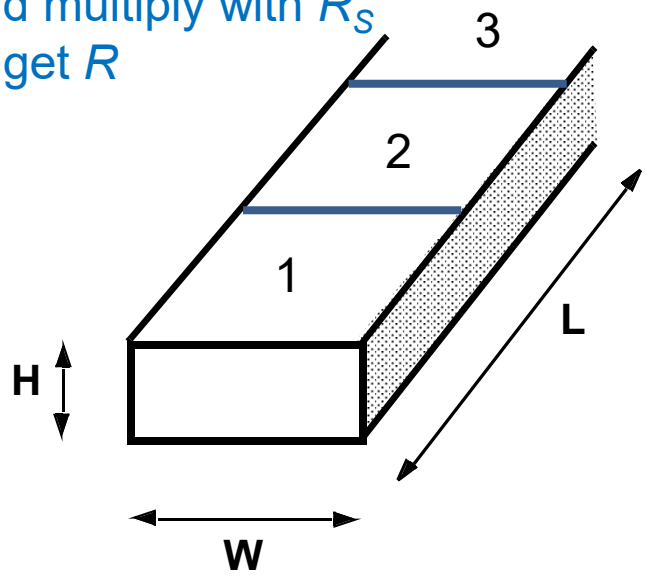
# Layer stack

- AMS 0.35 μm process has 3 metal layers
  - M1 for within-cell routing
  - M2/M3 for vertical/horizontal routing between cells
- Modern processes use 6-10+ metal layers
  - M1: thin, narrow (< 1.5*minimum feature size)
    - High density wiring in cells
  - Mid layers: thick, wide
    - Global interconnect
  - Top layers: THICK, WIDE
    - For $V_{DD}$, GND, clk



# Sheet resistance

Just count number of squares along wire and multiply with $R_S$ to get $R$




$$R = \rho \frac{L}{H W}$$

When W=L the resistance is equal to $R_0$, the sheet resistance (i.e. the resistance of a square wire)

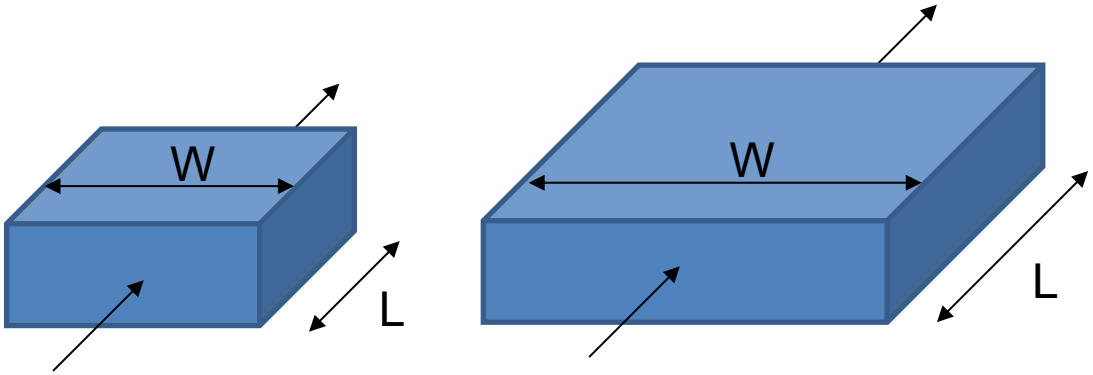
Sheet Resistance

$R_0 = \rho / H$

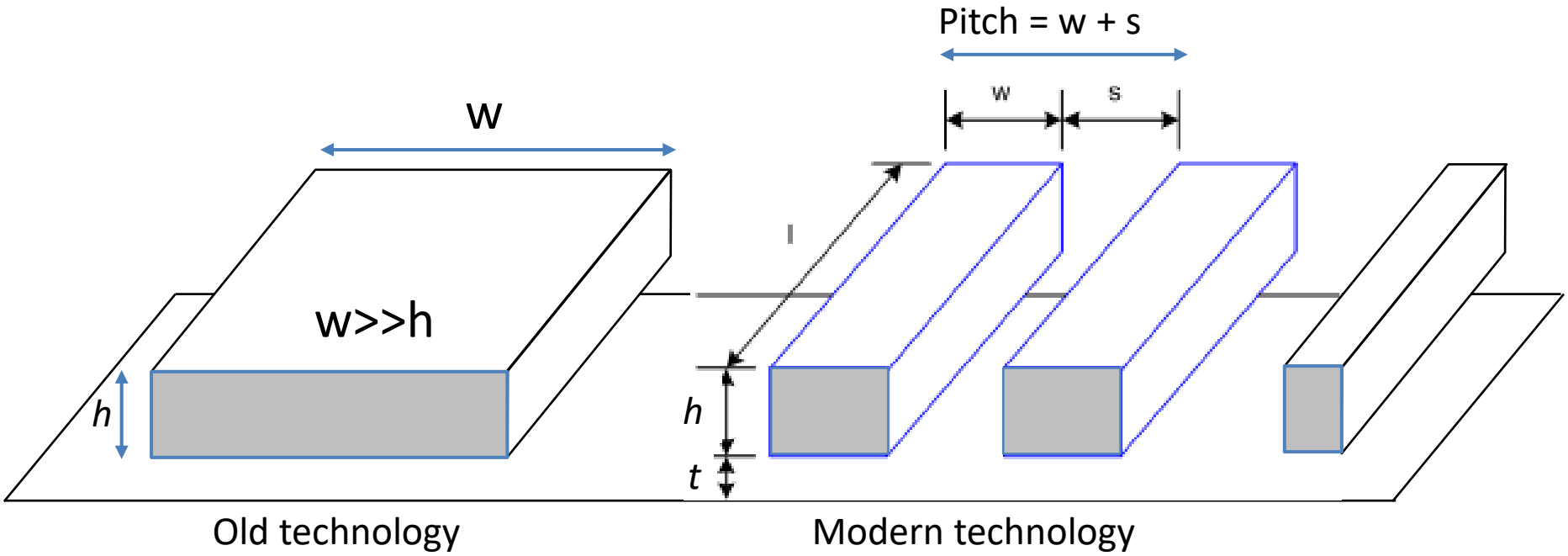
Some books use $R_S$ instead of $R_0$

$R_1 \equiv R_2$

All wires in a layer, or sheet, have the same height H, therefore we use "sheet resistance" in $\Omega/\square$ (ohms per square)



# Wire geometry




Today: pack in many skinny wires!
For long skinny wires resistance cannot be neglected since cross sectional area shrinks with feature size, wire length stays the same or increases. Hence: we need a wire RC model

# Example

- Compute the sheet resistance of a 0.22 μm thick Cu wire in a 65 nm process.
  The resistivity of thin film Cu is 22 nΩ·m.

- Find the total resistance if the wire is 0.125 μm wide and 1 mm long.

# Example

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$$R_S = \frac{22\times10^{-9}\ \Omega\cdot\mathrm{m}}{0.22\times10^{-6}\ \mathrm{m}} = 0.10\ \Omega/\square$$

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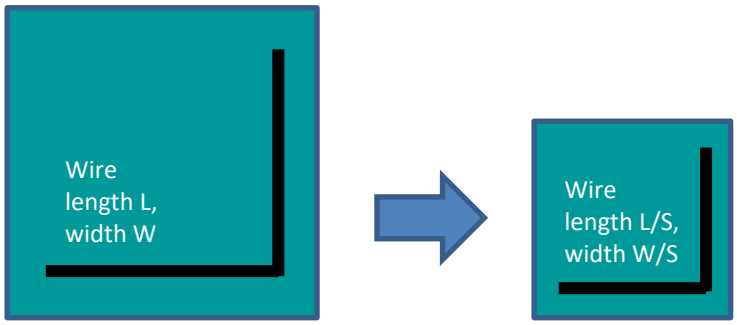
- Find the total resistance if the wire is 0.125 μm wide and 1 mm long.

$$R = 0.10\times\frac{1000\ \mu m}{0.125\ \mu m} = 800\ \Omega$$

# Wire delay scaling – Local wires




- For local wire crossing the same amount of circuitry
  - Resistance stays roughly constant
    - Length decreases by same amount as width,
    - height stays large and/or change material to copper
  - Capacitance decreases by scaling factor
    - Cap/unit length stays constant, length decreases

stays constant

$$R = \frac{\rho}{h}\frac{L/S}{W/S}$$

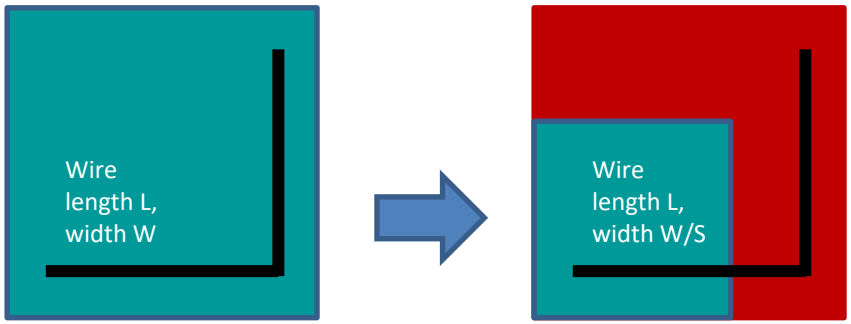
$$C = \left(WC_{ox}\right)L/S$$

stays constant

- Conclusion: Local wire delay tracks improvement in gate delay since both *RC*~1/*S*.

From Mark Horowitz at Design Automation Conference 2000

# Wire delay scaling – Global wires




- For global wire crossing the whole chip
  - Resistance grows linearly (with scaling factor)
  - Capacitance stays fixed
- Conclusion: Global wire delay increases relative to gate delay since wire *RC*~*S* and gate *RC*~1/*S*.

stays constant

$$R = \frac{\rho}{h}\frac{L}{W/S} \sim$$

$$C = \left(WC_{ox}\right)L$$

stays constant

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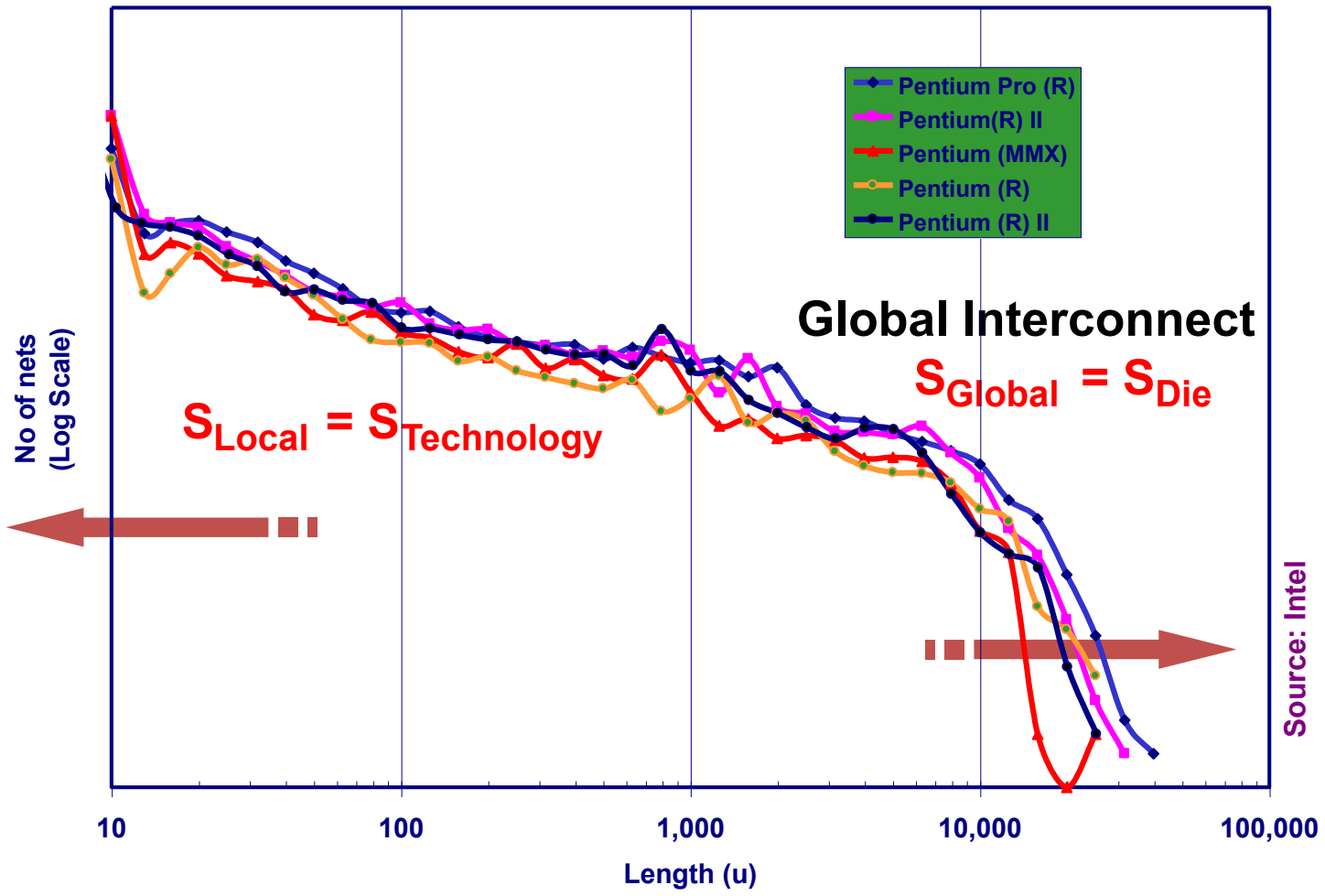
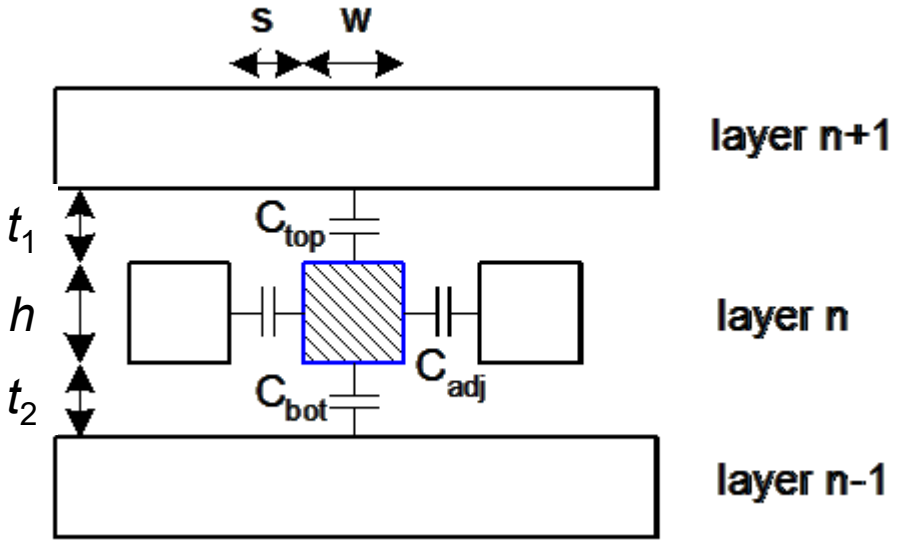
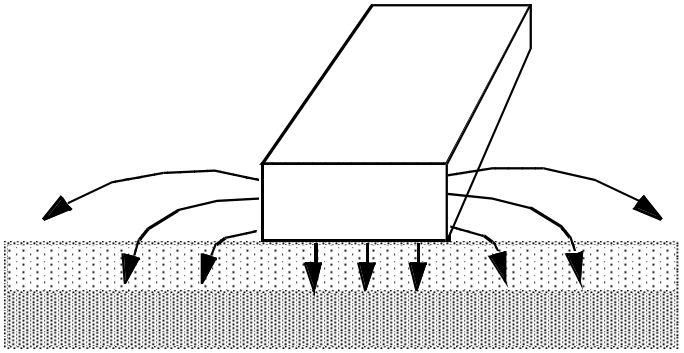
# Modern Interconnect



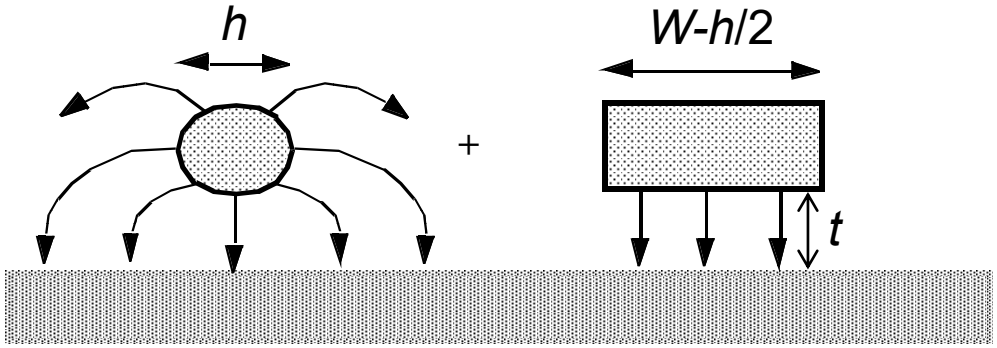
# Wire capacitance




Bottom plate and fringe capacitance



(a)




(b)

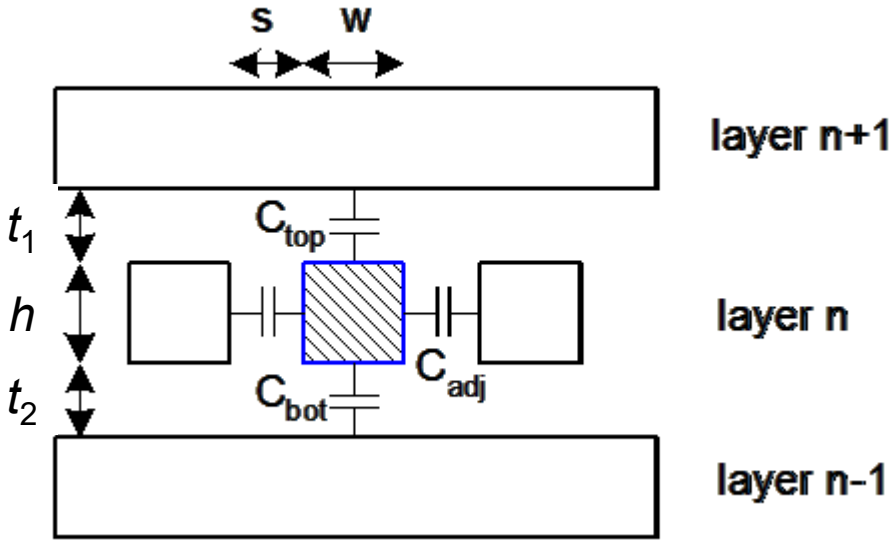
Wire has capacitance *c* per unit length

- to neighbors
- to layers above and below

Parallel plate capacitance equation

- $C = WL\varepsilon/t$
- $\varepsilon_{ox}=\kappa\varepsilon_0$, $\kappa\approx4$ for $SiO_2$, low-kappa $\kappa<3$

# Wire capacitance

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Parallel plate capacitance equation

- $C = WL\varepsilon/t$
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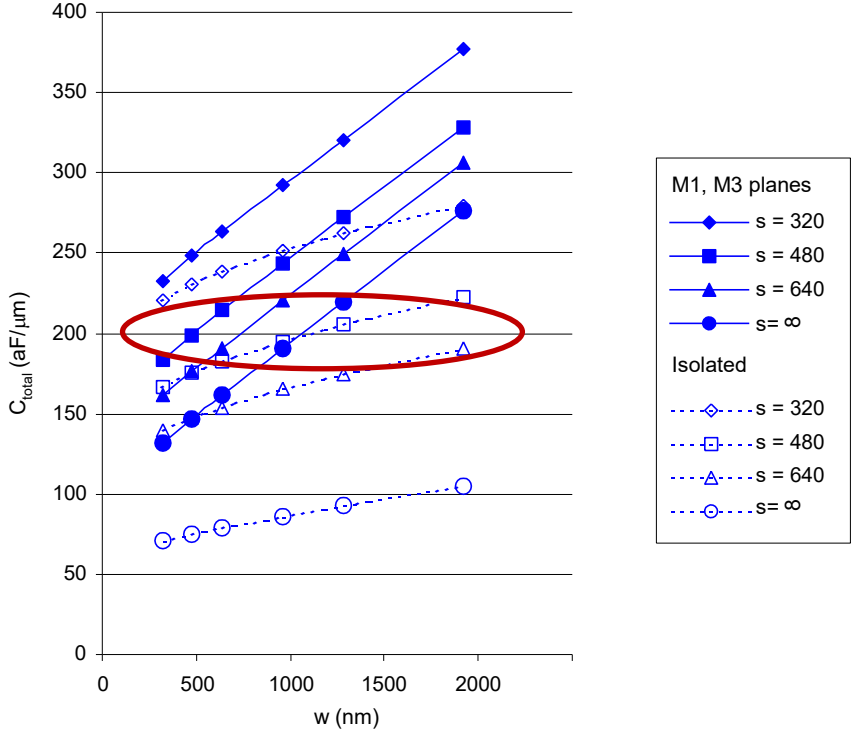
Typical wires have ~0.2 fF/μm, i.e. 200 fF/mm. Compare with 1.2 fF/μm MOSFET gate capacitance



# Wire RC delay

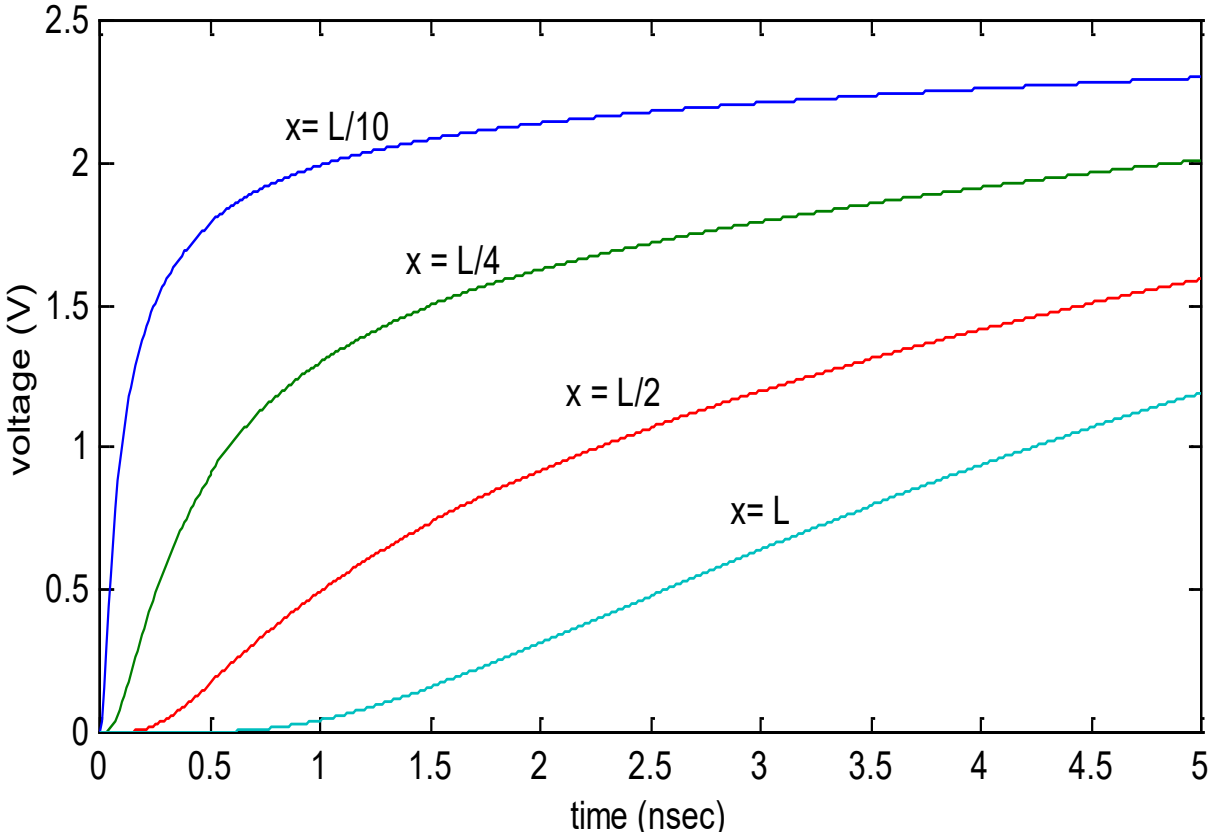
In any given technology

- wire RC increases as $L^2$ with wire length $L$
- $r$ is wire resistance per unit length
- $c$ is wire resistance per unit length

$$R = \frac{R_S L}{W} = rL \qquad C = \left(WC_{ox}\right)L = cL$$

$$RC = rcL^2$$

# Step-response voltage along the wire as a function of time



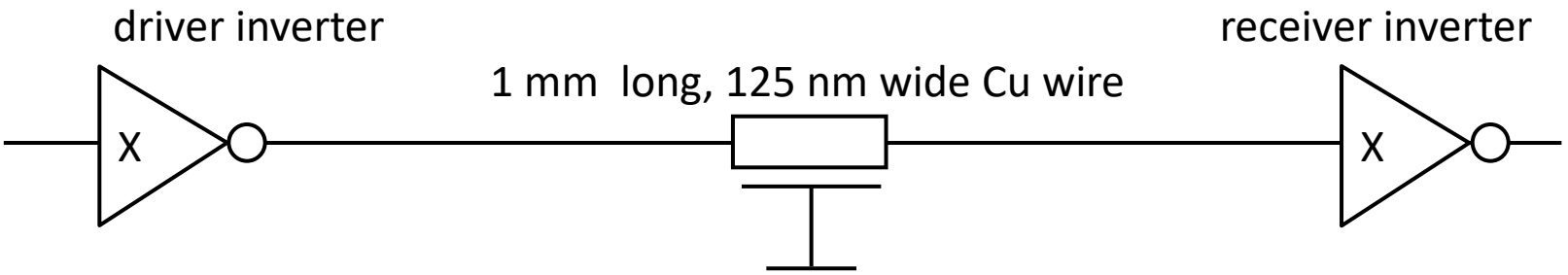
# Wire delay example

Estimate the delay of an inverter driving an identical inverter at the end of the 1 mm wire! $W_P=2W_N$.

Assume wire cap $c$= 200 fF/mm, $r$=800 Ω/mm from previous examples

Without wire, electrical effort is $h$=1

Delay becomes 5 ps*($p_{inv}$+$h$)=5*2 = 10 ps



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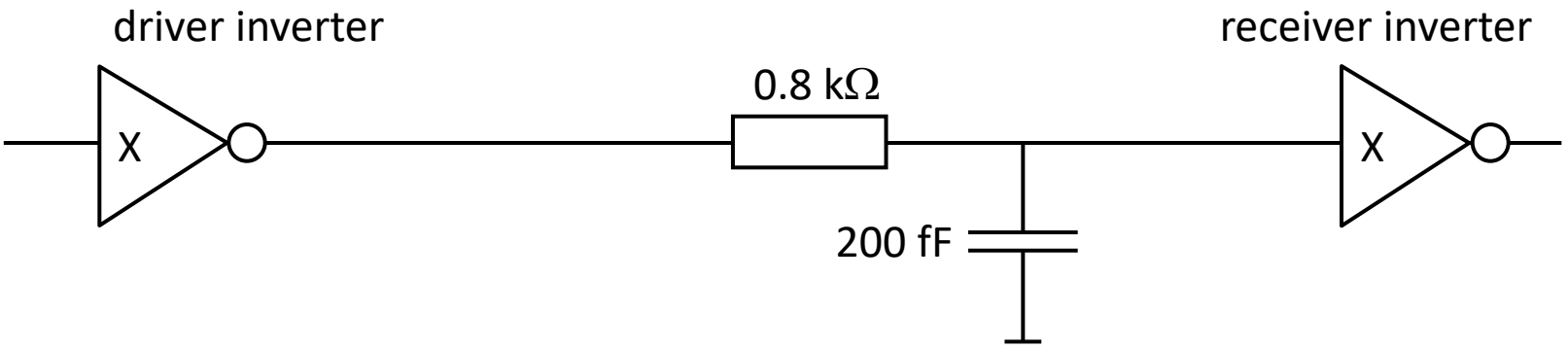


Wire RC product is $R_WC_W$=160 ps. To be compared with inverter $RC$=7.2 ps

Wire effort is $W_E$=160/7.2=22

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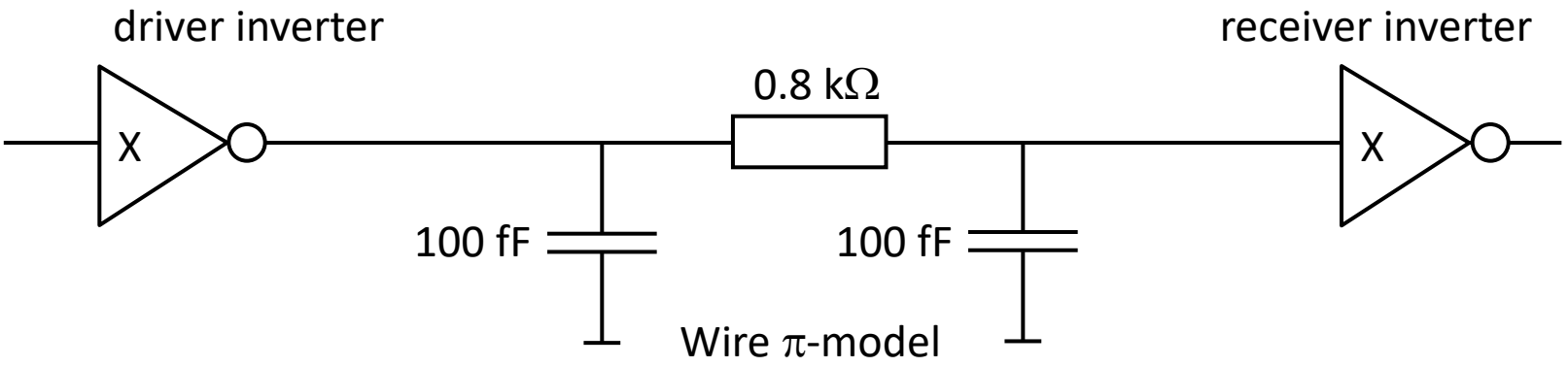


Wire capacitance is distributed and must at least be divided into 2 halves

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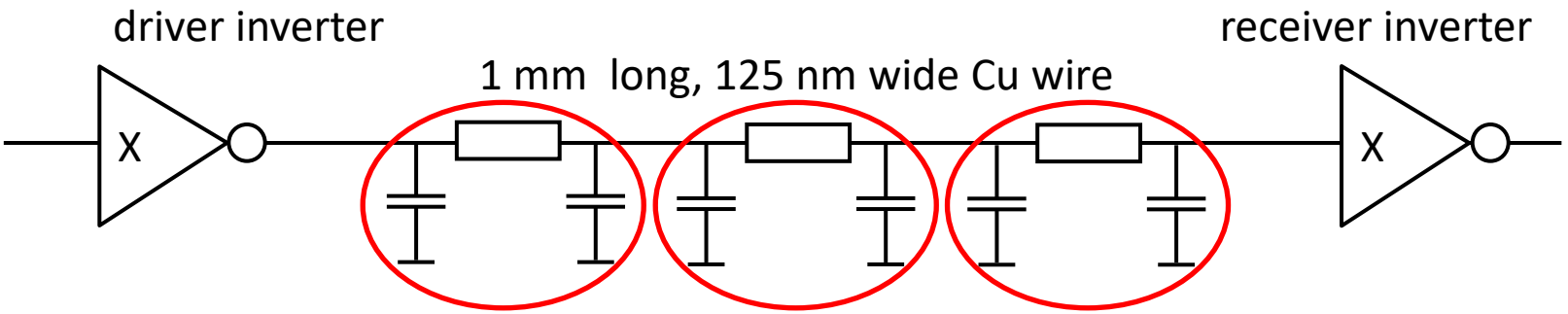


Wires are distributed systems

Approximate with lumped element models

In Spice simulations a 3-segment π-model is accurate to 3%

# Wire delay example

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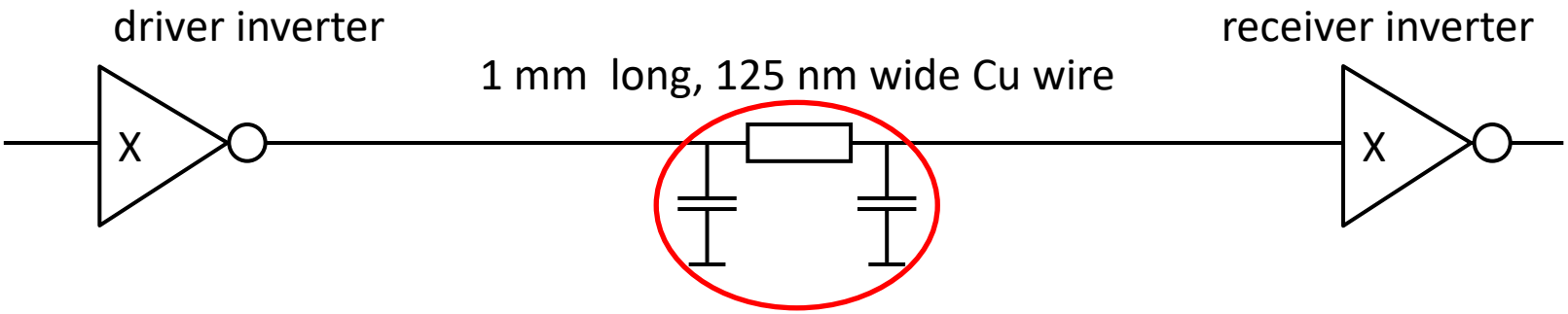


Wires are distributed systems
For analytical solution:
use single segment π-model

# Wire effort

- This year I decided to introduce a new concept
- The wire effort, similar to logical effort
- The ratio between RC products
- In our example the wire RC product is $R_W C_W$=160 ps compared to inverter $RC$=7.2 ps ($\tau$/0.7)
- Wire effort in our example is $W_E = \frac{R_W C_W}{RC} = \frac{160}{7.2} = 22.2$
- Why introduce this new concept?
- Because minimum normalized wire delay is $T_E = 4\sqrt{\frac{R_W C_W}{RC}} = 18.9$
- And the critical wire length is $L_{crit} = \frac{2L}{\sqrt{W_E}} = 0.42 \text{ mm}$

# Wire delay example

Estimate the delay of an inverter driving an identical inverter at the end of the 1 mm wire! $W_P=2W_N$.

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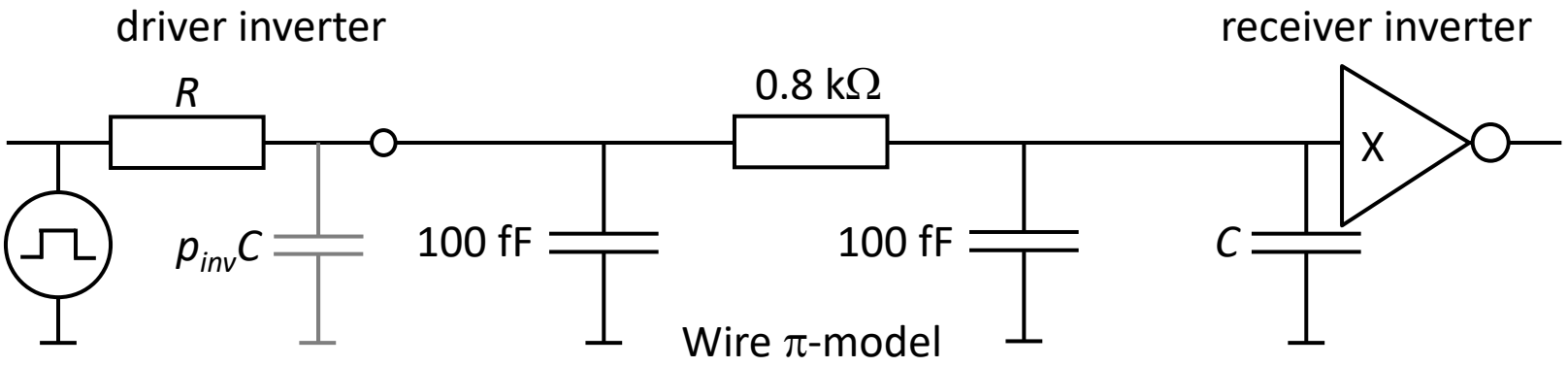



Introduce electrical inverter models

What is the delay of this two-stage RC circuit?

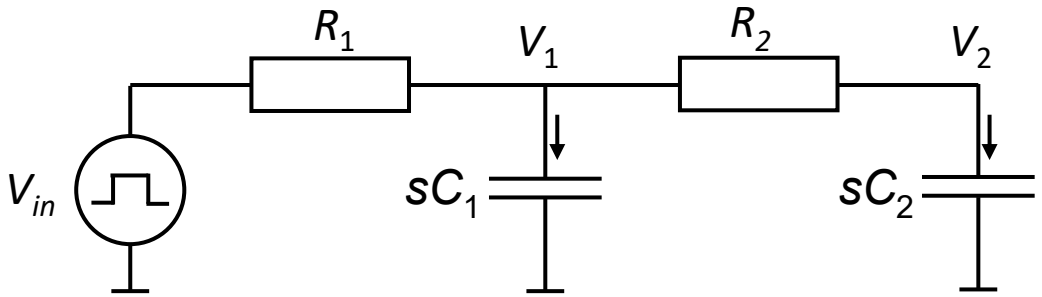
Can be found analytically from second-order differential equation!

# Wire delay example

Estimate the delay of an inverter driving an identical inverter at the end of the 1 mm wire! $W_P=2W_N$.

Assume wire cap $c$= 200 fF/mm, $r$=800 Ω/mm from previous examples

- For a moment, let us simplify the two-stage RC circuit!
- Get transfer function!




This transfer function contains a second-order equation with two solutions $s_1$ and $s_2$.

$$H(s)=\frac{1}{s^2R_1R_2C_1C_2+s\left(R_1\left(C_1+C_2\right)+R_2C_2\right)+1}$$

$$s^2R_1R_2C_1C_2+s\left(R_1\left(C_1+C_2\right)+R_2C_2\right)+1=0$$

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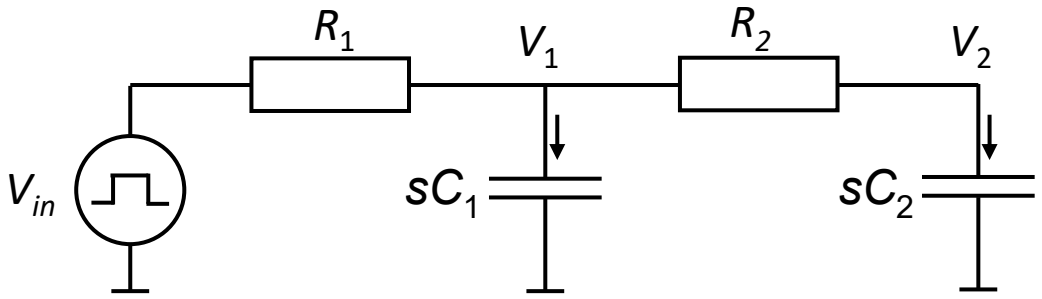


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This transfer function contains a second-order equation with two solutions $s_1$ and $s_2$.
Usually, $s_2$>>$s_1$.
Which indicates a dominating time constant $\tau_1=1/s_1$.
For a rising input step voltage, we get an exponentially decreasing output voltage

$$V_2(t)=V_{DD}e^{-t/\tau_1}$$

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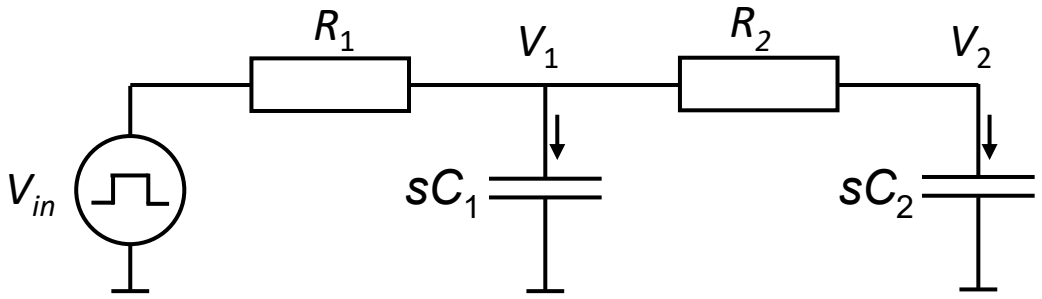


Neglect $s^2$ term in the transfer function and we immediately get $\tau_1 = R_1(C_1 + C_2) + R_2C_2$

$$s^2 R_1R_2C_1C_2 + s\left(R_1(C_1 + C_2) + R_2C_2\right) + 1 = 0$$

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$$V_2(t) = V_{DD}e^{-t/\tau_1}$$

# Approximative solution

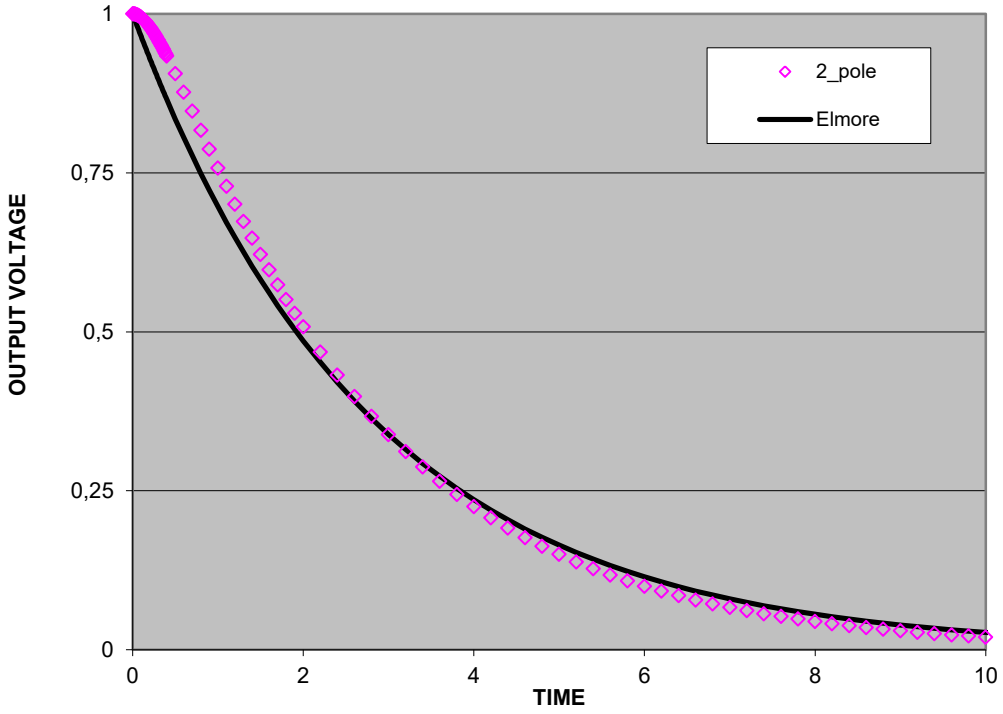
## with dominating time constant

One example:

$R_1=0.8R_2$, $C_1=1.2C_2$

$t_1=2.45$, $t_2=0.31$

Compare exponential two-pole solution with exponential decay assuming a dominant time constant $t_1=2.76$

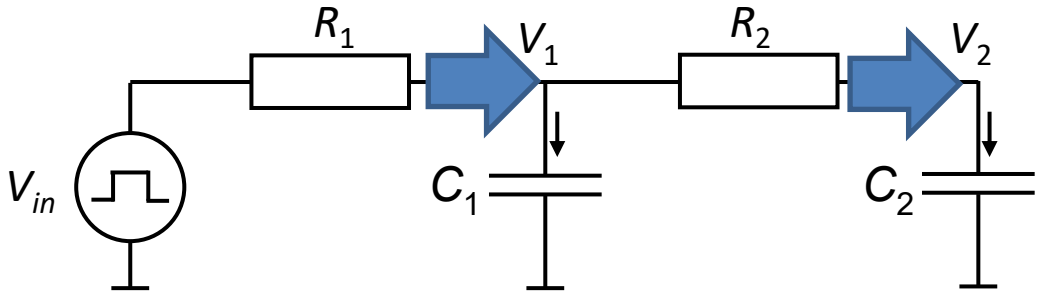


# Wire delay example

Estimate the delay of an inverter driving an identical inverter at the end of the 1 mm wire! $W_P=2W_N$.

Assume wire cap *c*= 200 fF/mm, *r*=800 Ω/mm from previous examples

- Now, let us return to the simplified two-stage RC circuit
- How to remember how to get the dominant time constant?




Each resistance is multiplied by its downstream capacitance!

$$\tau_1 = R_1\left(C_1 + C_2\right) + R_2 C_2$$

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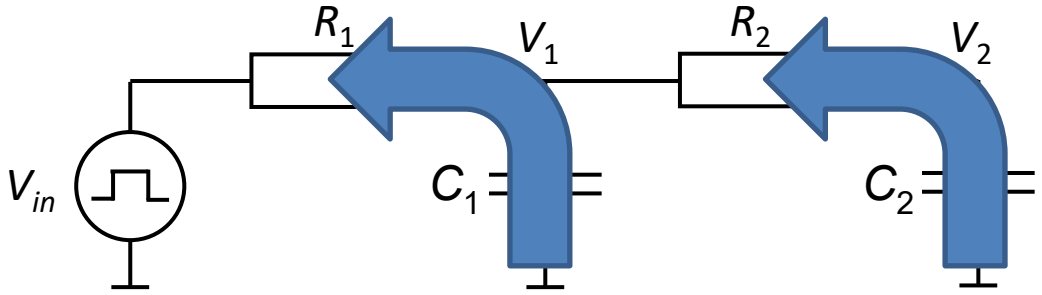


Or: Each capacitance is multiplied by its upstream capacitance!

$$\tau_1 = R_1 C_1 + (R_1 + R_2) C_2$$

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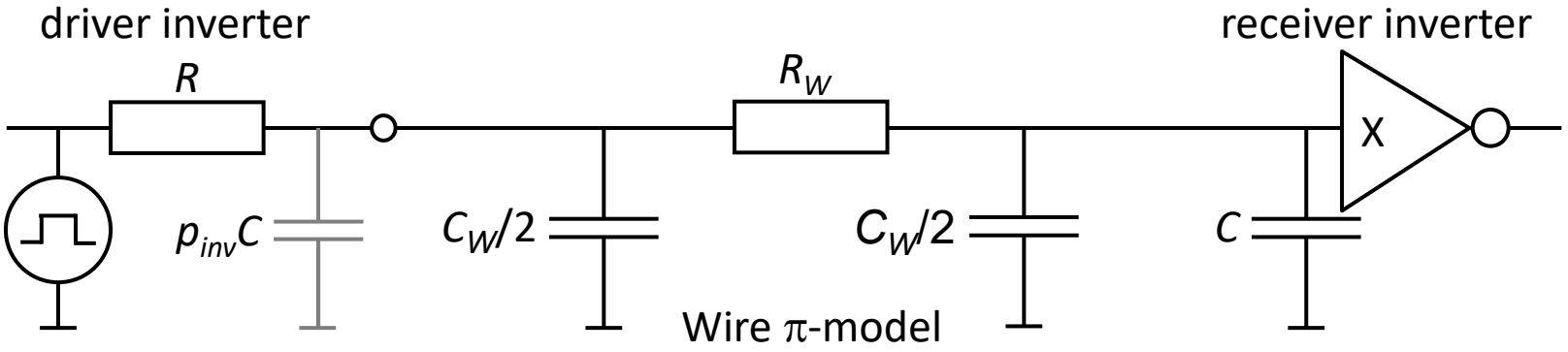
Without wire, electrical effort is *h*=1. Delay becomes 5 ps*($p_{inv}$+1)=5*2 = 10 ps




Now, let us apply the dominant time constant model to our example.

$$\tau_1 = R\left(p_{inv}C + C + C_W\right) + R_W\left(C + \frac{C_W}{2}\right) = RC\left(p_{inv}+1\right) + RC_W + R_WC + \frac{R_WC_W}{2}$$

# Wire delay example

Estimate the delay of an inverter driving an identical inverter at the end of the 1 mm wire! $W_P=2W_N$.

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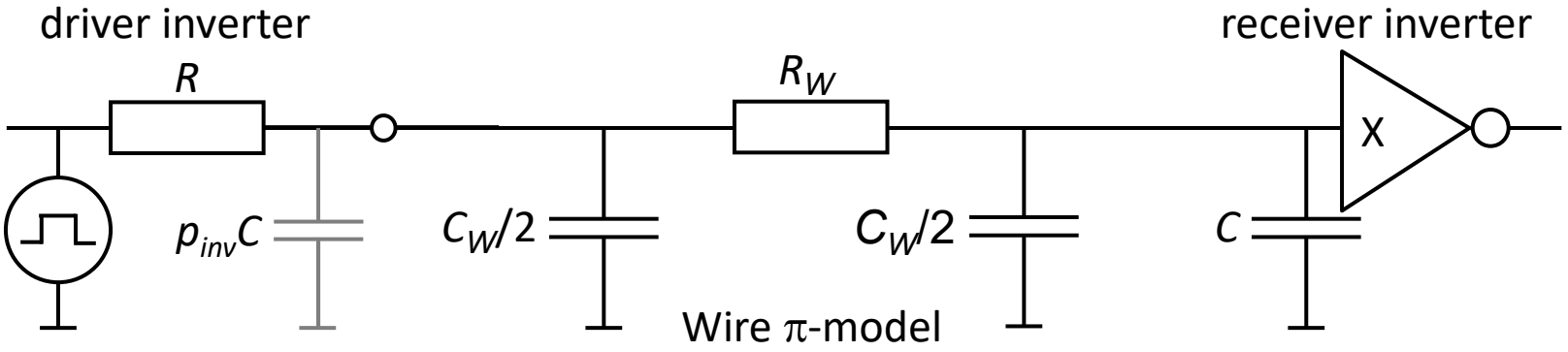


Once time constant is known, delay can be normalized wrt ideal FO1 delay, i.e. to tau!

$$t_{pd} = 0.7RC\left( p_{inv} + 1 + \frac{R_W C_W}{RC}\frac{R}{R_W} + \frac{R_W}{R} + \frac{R_W C_W}{2RC} \right)$$

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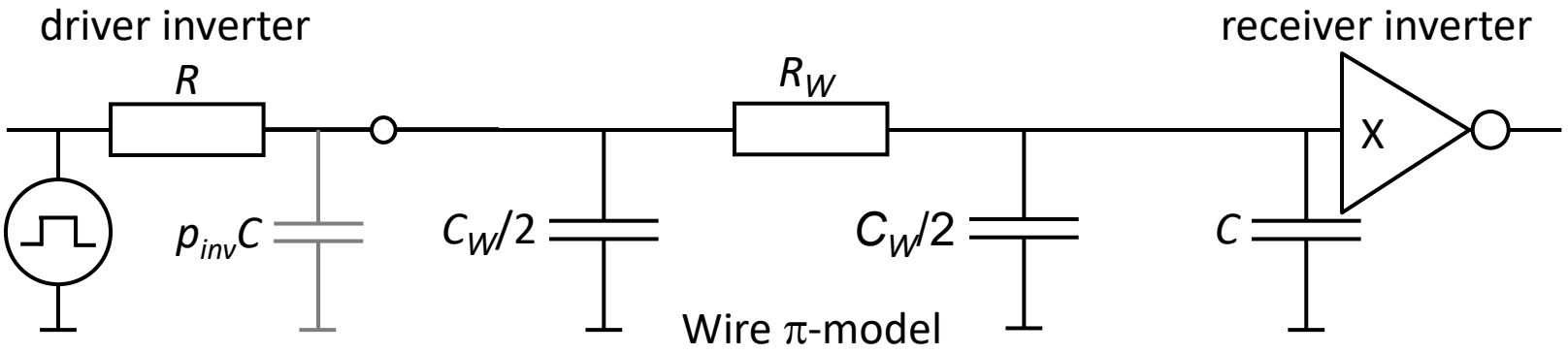


In terms of the wire effort $W_E=R_WC_W/RC$?

$$t_{pd} = 0.7RC\left( p_{inv} + 1 + W_E \frac{R}{R_W} + \frac{R_W}{R} + \frac{W_E}{2} \right)$$

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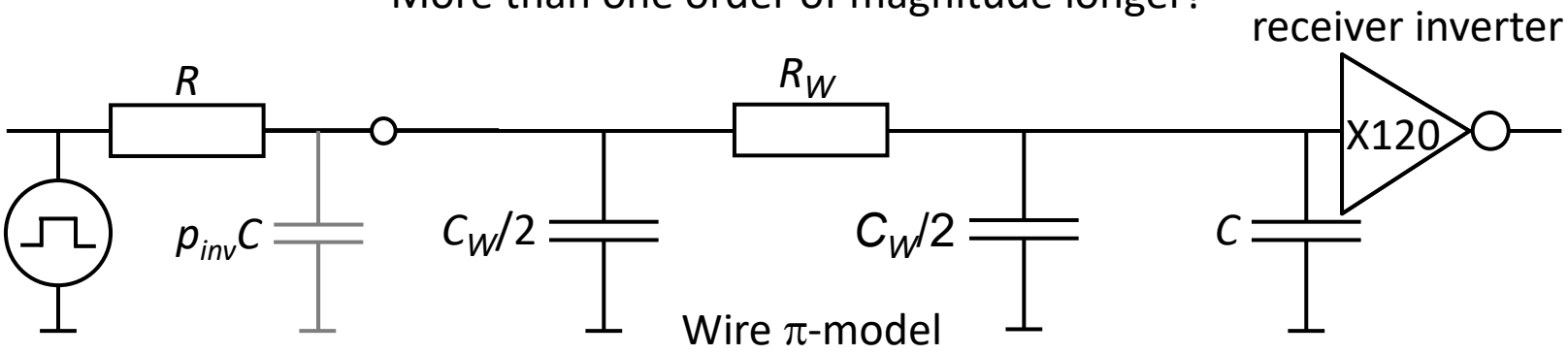
Without wire, electrical effort is $h$=1. Delay becomes 5 ps*($p_{inv}$+1)=5*2 = 10 ps
With wire, normalized delay becomes $d=2+2\sqrt{W_E}+W_E/2=22.5$ instead of 2!
More than one order of magnitude longer!




How should driver resistance be chosen wrt $R_W$ for minimum delay? Let derivative wrt $R$ be zero!

$$\frac{\partial d}{\partial R}=\frac{W_E}{R_W}-\frac{R_W}{R^2}=0 \rightarrow R=\frac{R_W}{\sqrt{W_E}};\ R_W=0.8\ \text{k}\Omega,\ W_E=22.2 \rightarrow R=170\ \Omega$$

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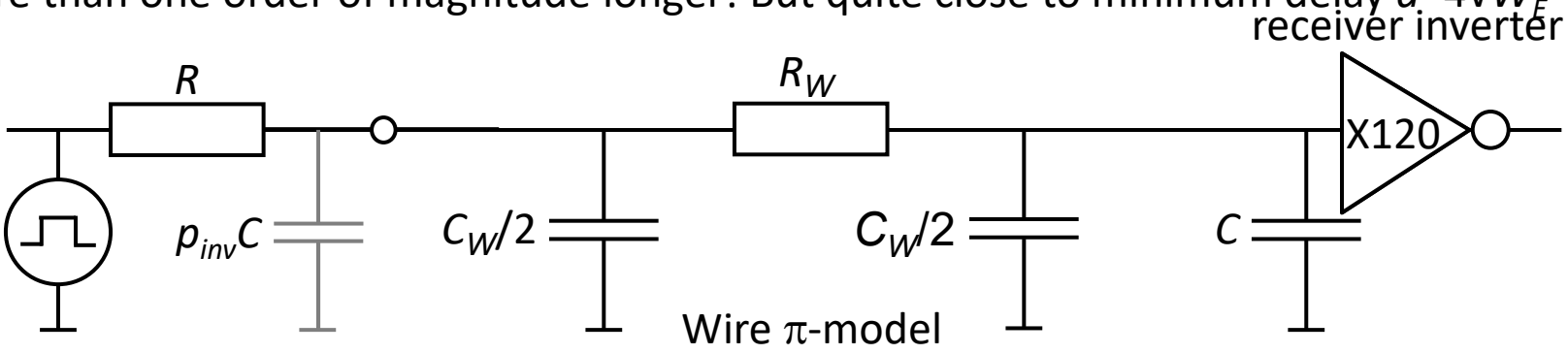
More than one order of magnitude longer! But quite close to minimum delay $d=4\sqrt{W_E}=18.9$

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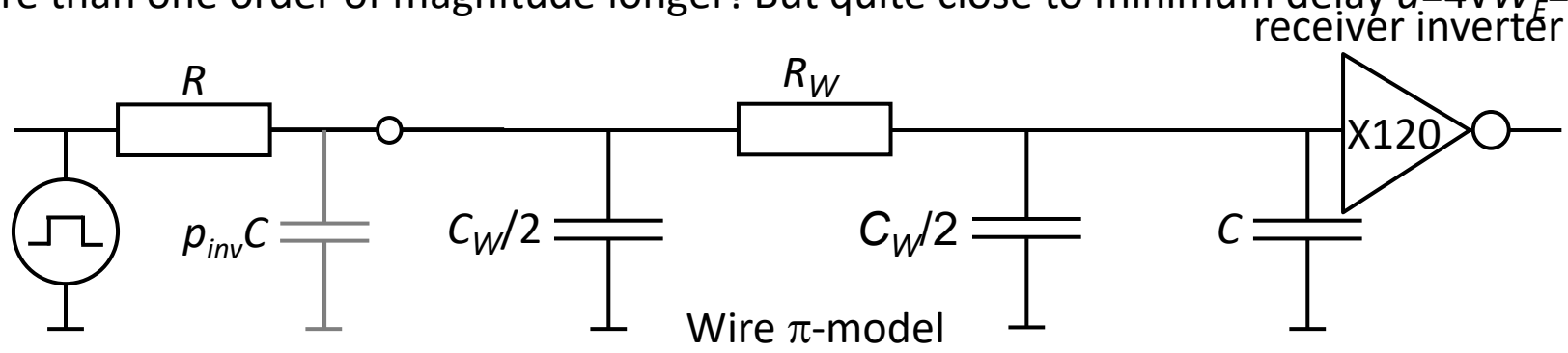
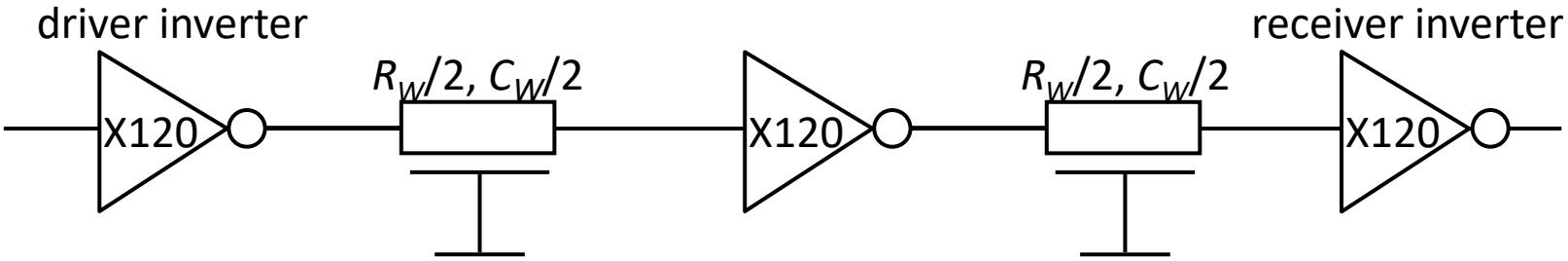



The wire effort is proportional to wire length squared!

$$W_E = \frac{rcL^2}{RC} \sim L^2$$ Therefore, keep wires short!

# Keeping wires short using repeaters

Divide wire into 2 segments driven by repeaters.
A repeater is just an identical inverter called repeater!
To estimate the propagation delay, just add the two segment delays!




$$d = 2\left( p_{inv} + 1 + \frac{W_E}{2}\frac{R}{R_W} + \frac{R_W}{2R} + \frac{W_E}{8} \right)$$

Eq. from slide 30

$$d = 2\left( p_{inv} + 1 + \frac{\sqrt{W_E}}{2} + \frac{\sqrt{W_E}}{2} + \frac{W_E}{8} \right) = 2\left(2 + 2.35 + 2.35 + 2.8\right) = 19$$

Quite close to minimum delay $d = 4\sqrt{W_E} = 18.8$

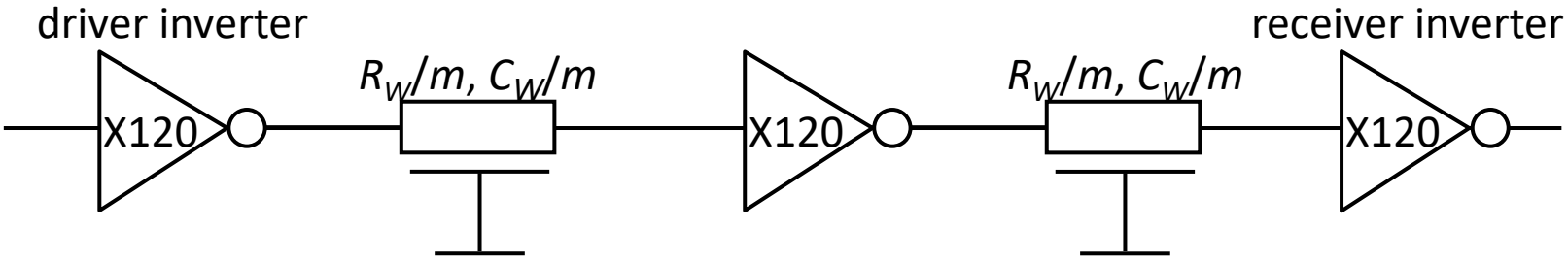
# Keeping wires short using repeaters

The general case: finding the optimal number of segments

Divide wire into *m* segments driven by repeaters.

A repeater is just an identical inverter called repeater!

To estimate the propagation delay, just add the segment delays!




$$d = m\left( p_{inv} + 1 + \frac{W_E}{m}\frac{R}{R_W} + \frac{1}{m}\frac{R_W}{R} + \frac{W_E}{2m^2} \right)$$

Eq. from slide 30

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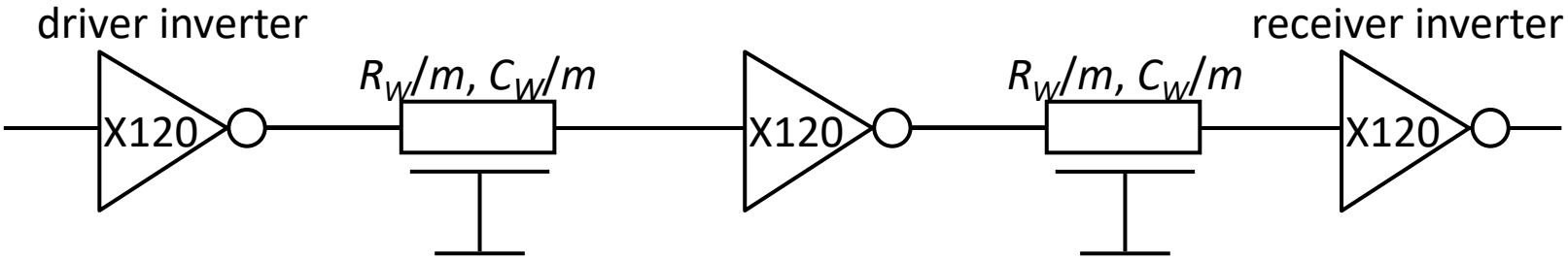



$$d = m\left( p_{inv} + 1 + \frac{W_E}{m}\frac{R}{R_W} + \frac{1}{m}\frac{R_W}{R} + \frac{W_E}{2m^2} \right)$$

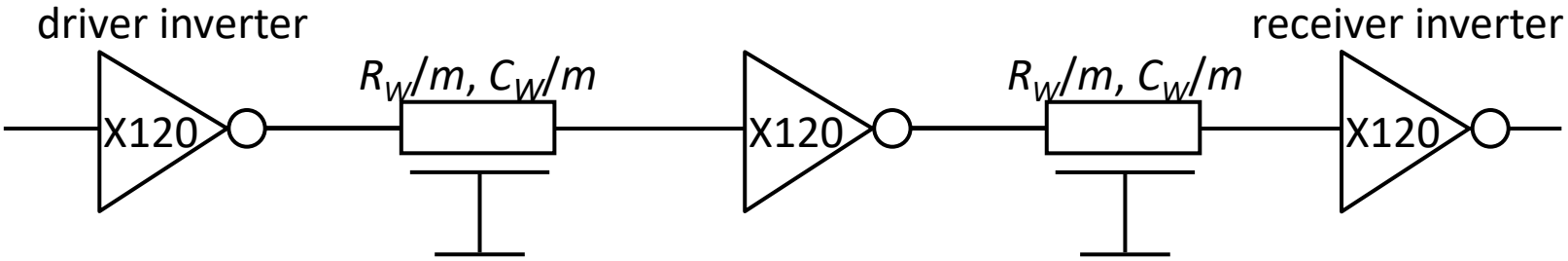
Eq. from slide 30

Minimum delay for ∂*d*/ ∂*m*=0, i.e. for $m = \frac{1}{2}\sqrt{W_E} = 2.35$ which means that the minimum normalized delay is $d=4\sqrt{W_E}$, and for $W_E$=22.5 we have $d_{min}\approx 18.9$ assuming $p_{inv}$=1.

# Keeping wires short using repeaters

We had $d$=22.4 without repeaters, so obviously there was not much to gain by sectioning wires 1 mm long into segments. Then, for what wire length does it start to pay off?

Well, the critical wire length is $L_{crit} = \frac{L}{m} = 2\sqrt{\frac{RC}{rc}}$




$$d = m\left( p_{inv} + 1 + \frac{W_E}{m}\frac{R}{R_W} + \frac{1}{m}\frac{R_W}{R} + \frac{W_E}{2m^2} \right) \qquad L_{crit} = 2\sqrt{\frac{RC}{rc}} = 2\sqrt{\frac{7.2}{160}} = 0.4 \text{ mm}$$

Minimum delay for $\partial d/\partial m$=0, i.e. for $m = \frac{1}{2}\sqrt{W_E} = 2.35$ which means that the minimum normalized delay is $d$=4√$W_E$, and for $W_E$=22.5 we have $d_{min}$≈18.9 assuming $p_{inv}$=1.

# Keeping wires short using repeaters

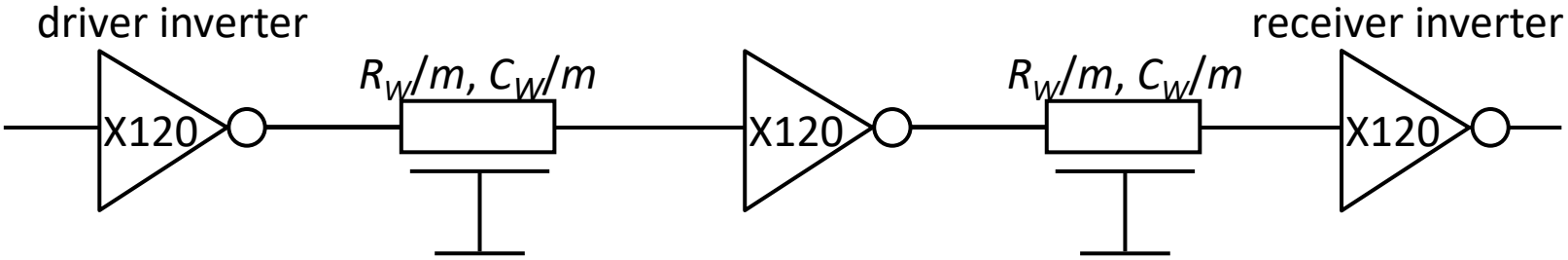
For what wire length does it start to pay off inserting repeaters?

Let´s have a look at a 10 mm wire.

Still $L_{crit}$=0.4 mm for this technology!

What if we divide the wire into 20 segments, each 0.5 mm long?

What would be our speed gain? Wire effort is now 100x larger!

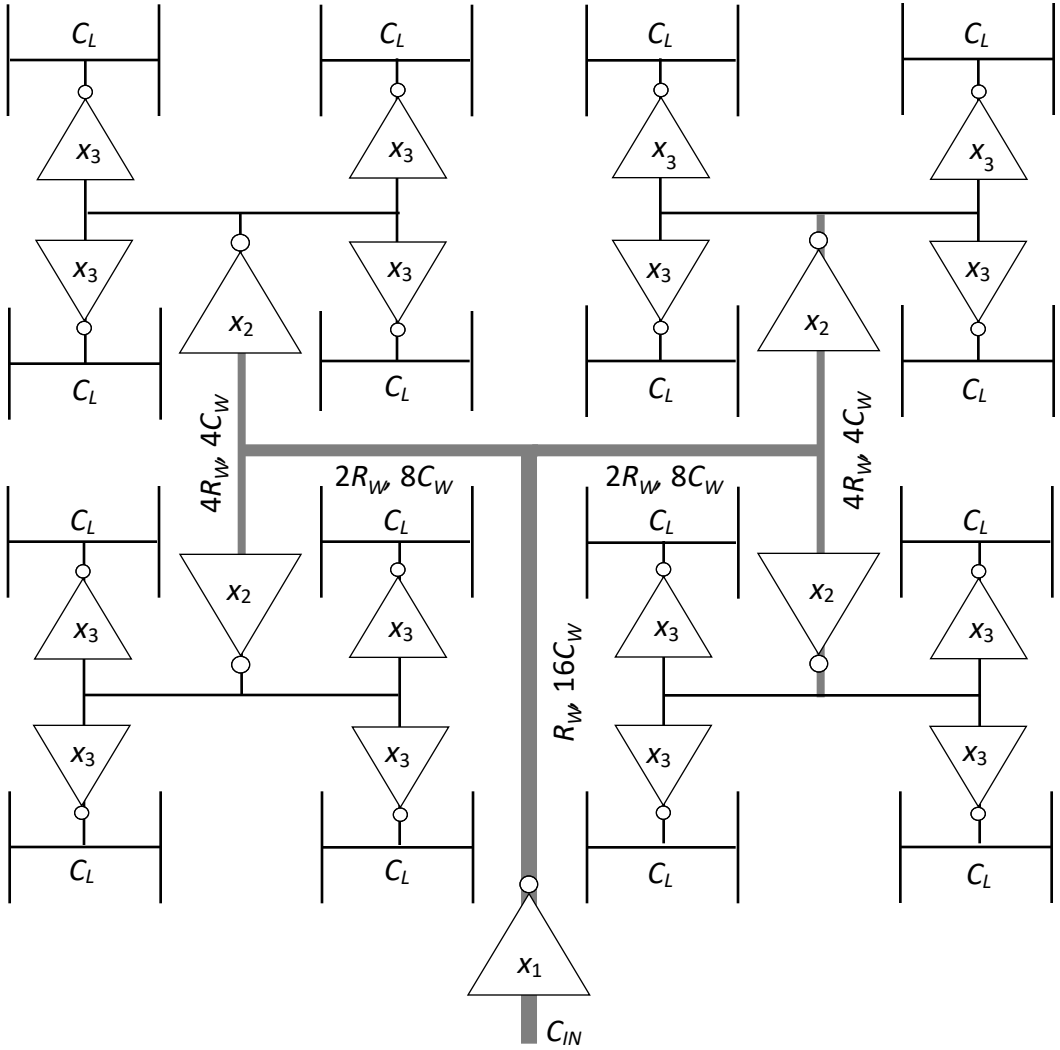



Without repeaters: $d = p_{inv} + 1 + 2\sqrt{W_E} + \frac{W_E}{2} = 2 + 2 \times 47 + \frac{2222}{2} = 1200$

With 20 repeaters: $d = 20\left( p_{inv} + 1 + \frac{2\sqrt{W_E}}{20} + \frac{W_E}{2 \times 20^2} \right) \approx 40 + 2 \times 47 + 56 = 190$

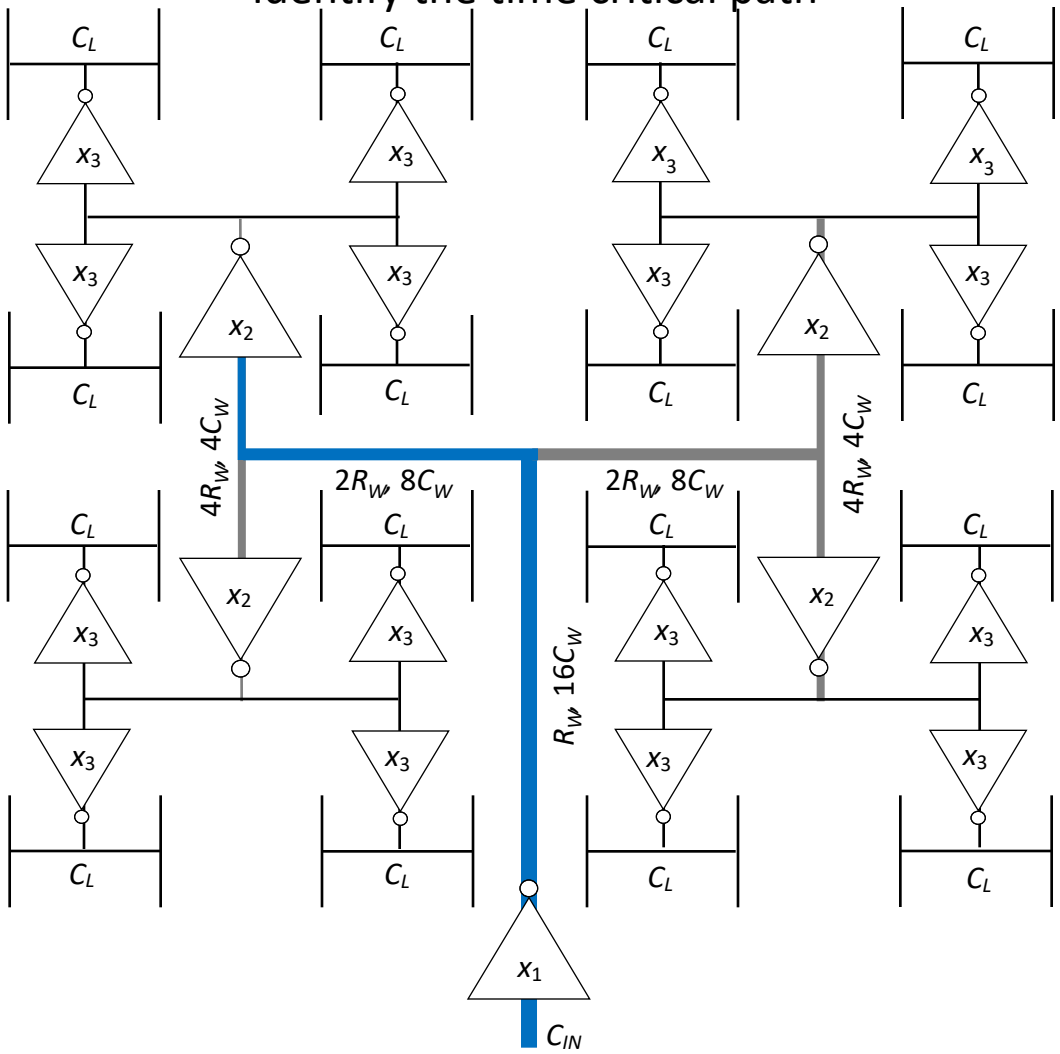
Minimum normalized delay is $d=4\sqrt{W_E}$=188.6. Quite close!

# H-tree clock distribution



# H-tree clock distribution

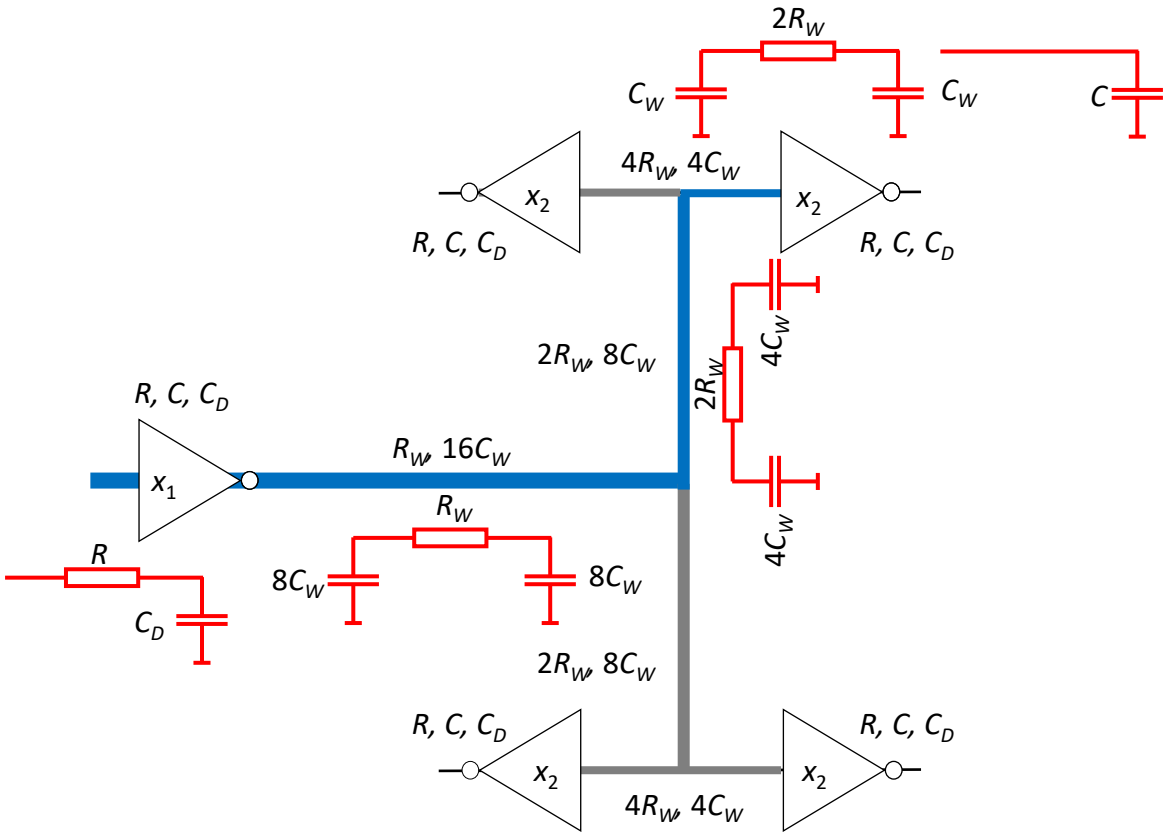
Identify the time critical path



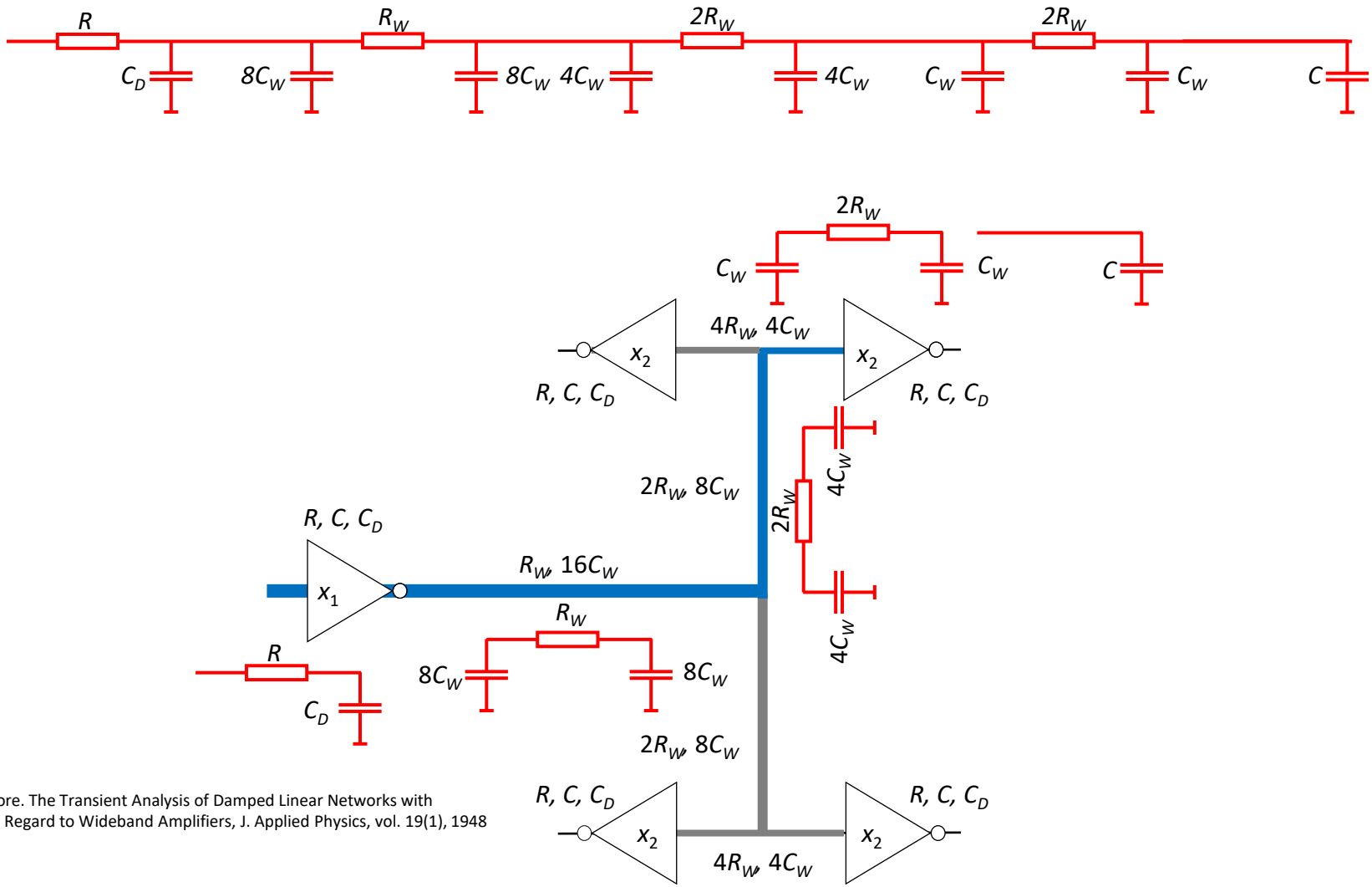
# Analyzing the time critical path

Identify the time critical path

Find the equivalent RC circuit describing the wire and its segments along the time critical path neglecting branches!

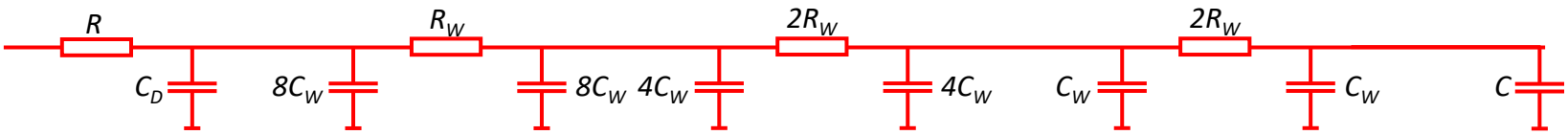


# Analyzing the time critical path

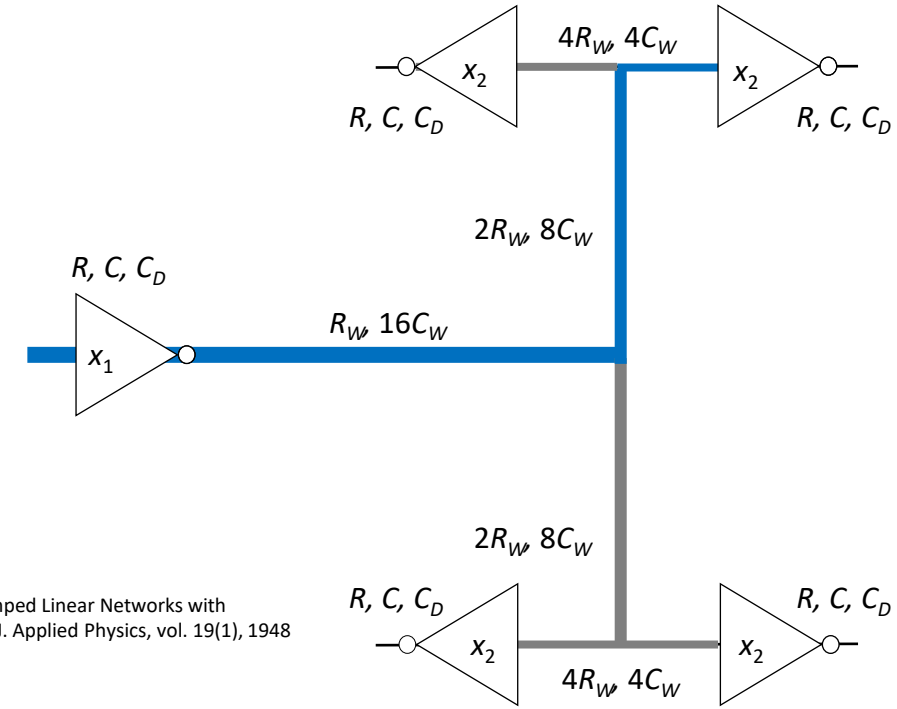



W.C. Elmore. The Transient Analysis of Damped Linear Networks with Particular Regard to Wideband Amplifiers, J. Applied Physics, vol. 19(1), 1948

# Analyzing the time critical path




This is a four-stage RC ladder, and its four time constants cannot be found analytically. However, William C. Elmore analyzed the transfer functions of *n*-stage RC-ladders and found that the sum of the time constants could be easily found as for *n*=2.

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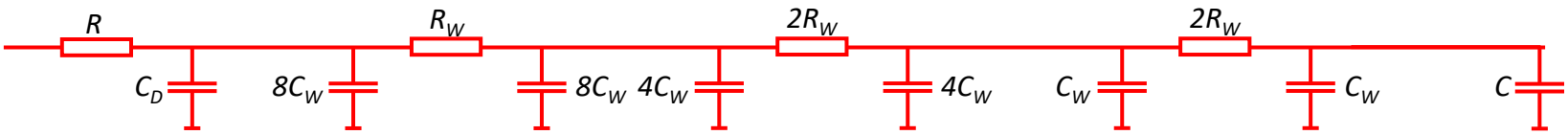
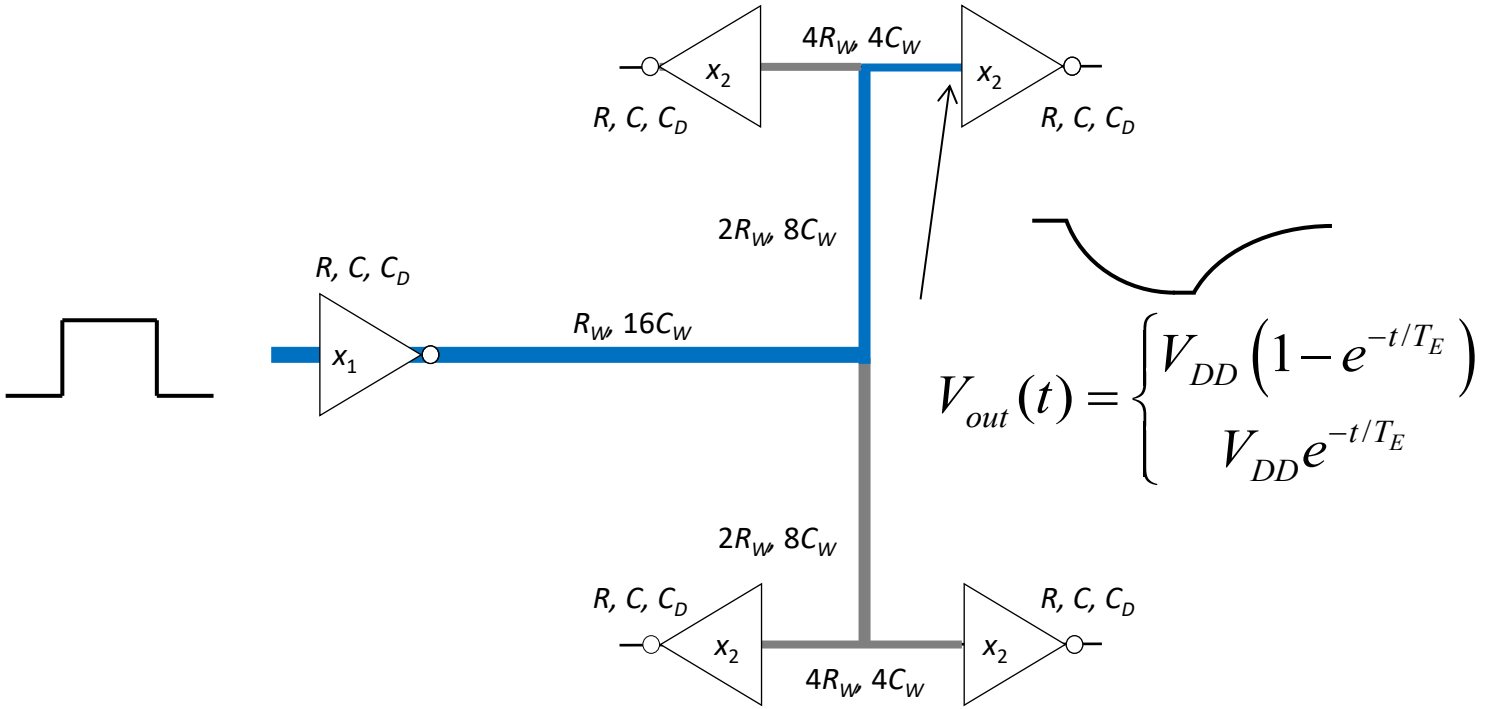
# Main path Elmore time constant

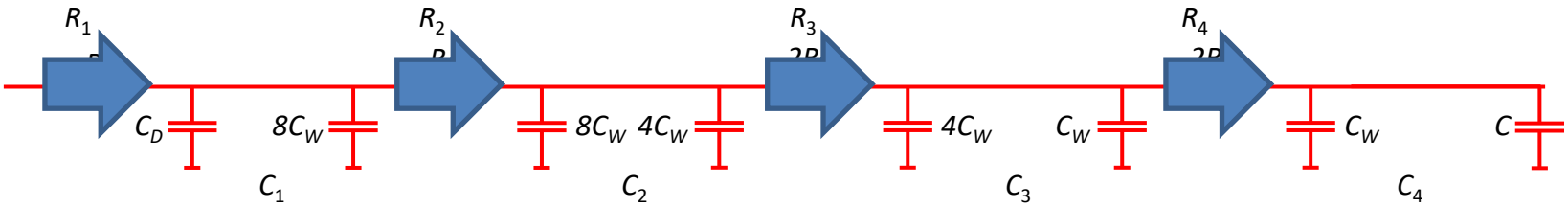



Knowing the sum of the time constants, and assuming the existence a dominant time constant, the exponential growth/decay of the output voltage can be easily found



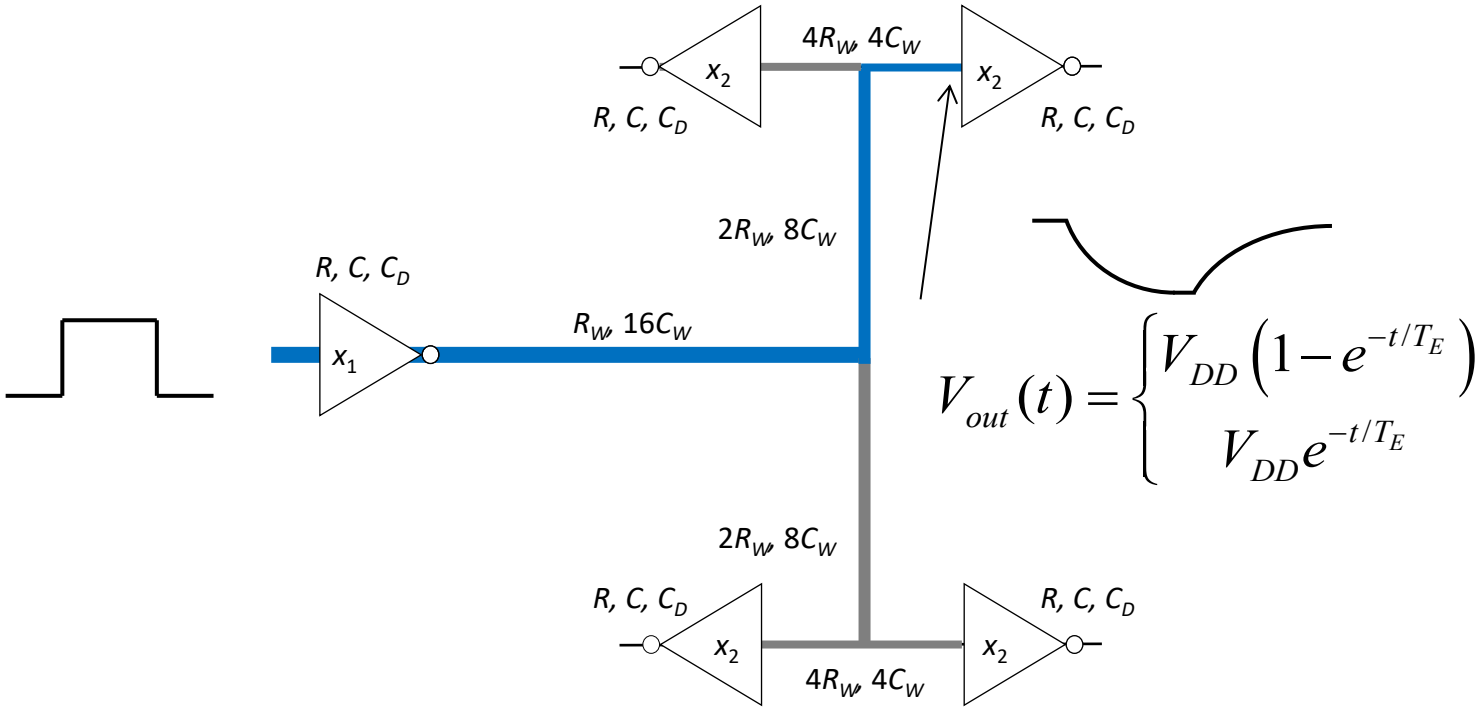

$$V_{out}(t) = \begin{cases} V_{DD}\left(1 - e^{-t/T_E}\right) \\ V_{DD}e^{-t/T_E} \end{cases}$$

# Main path Elmore time constant




The Elmore time constant $T_E$ is found by multiplying each $R$ with its downstream $C$

$$T_E = R_1\left(C_1 + C_2 + C_3 + C_4\right) + R_2\left(C_2 + C_3 + C_4\right) + R_3\left(C_3 + C_4\right) + R_4 C_4$$



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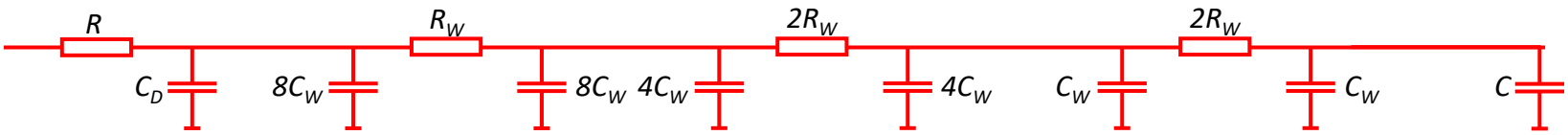


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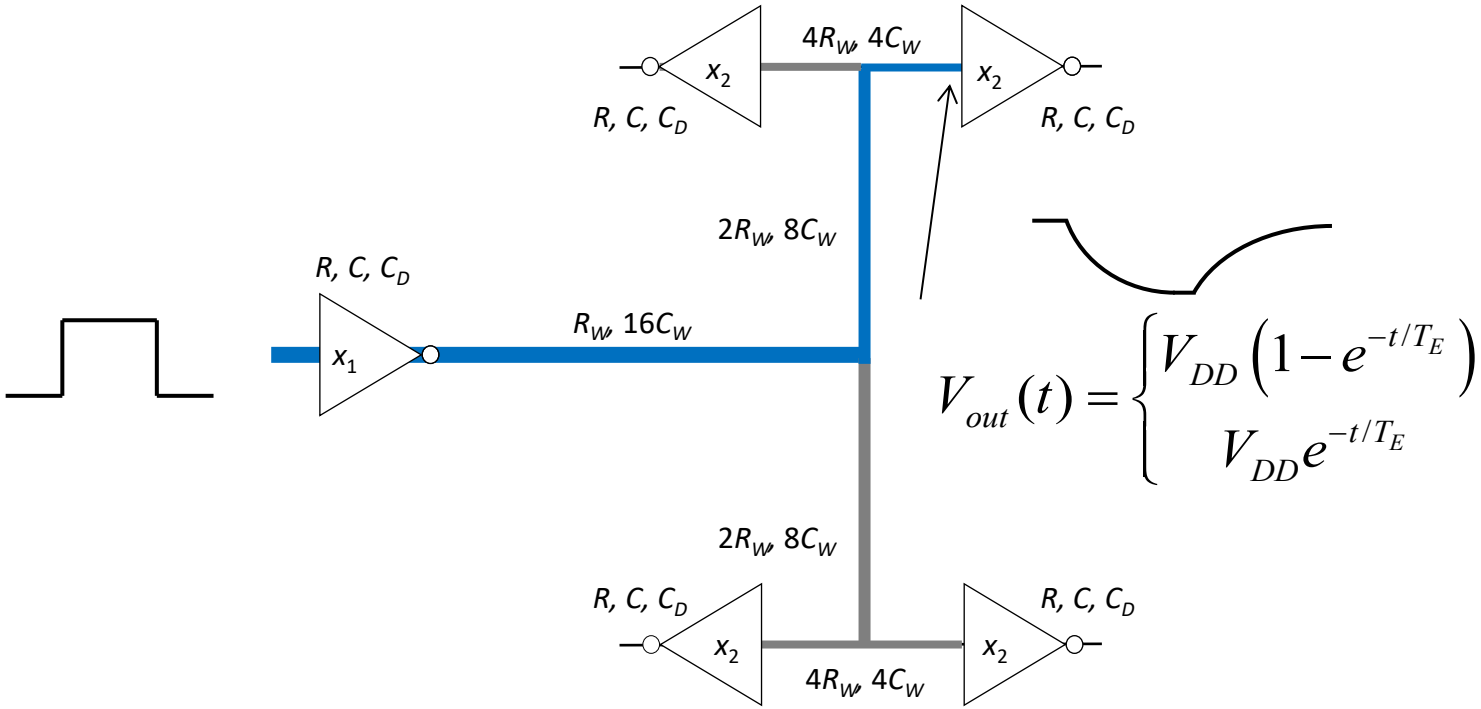
$$T_E = R\left(C_D + 26C_W + C\right) + 18R_W C_W + 2R_W 6C_W + 2R_W C_W + 5R_W C$$



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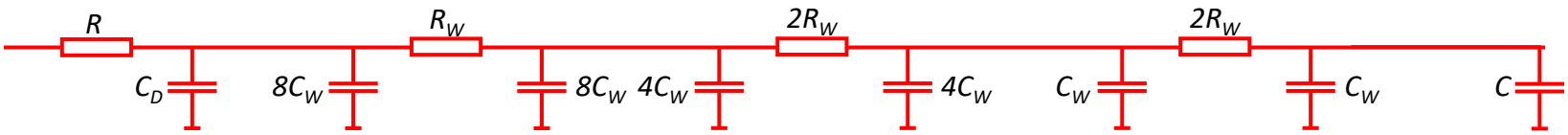
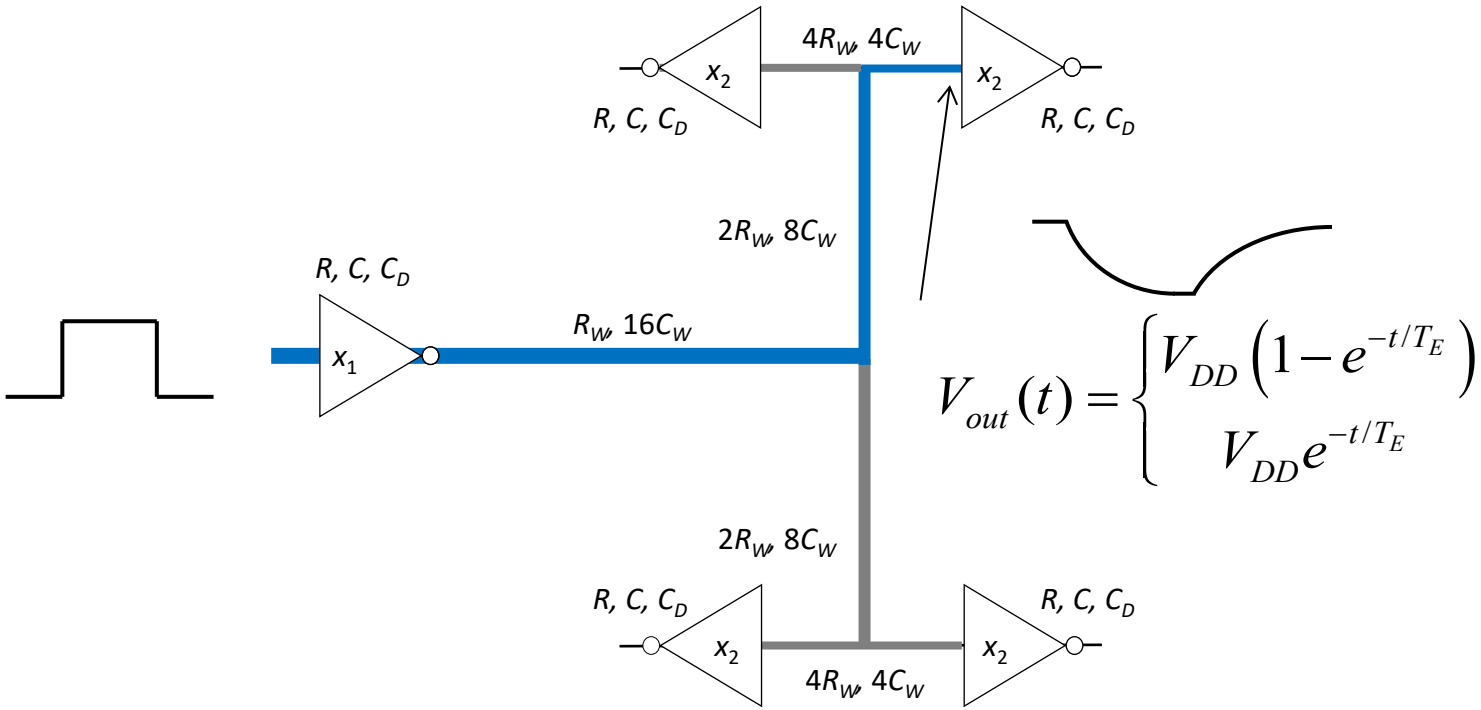
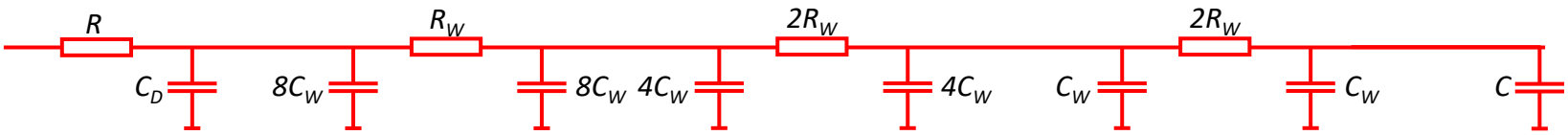



The Elmore time constant $T_E$ is found by multiplying each $R$ with its downstream $C$

Simplify: $$T_E = R(C_D + C) + 26RC_W + 5R_W C + 32R_W C_W$$

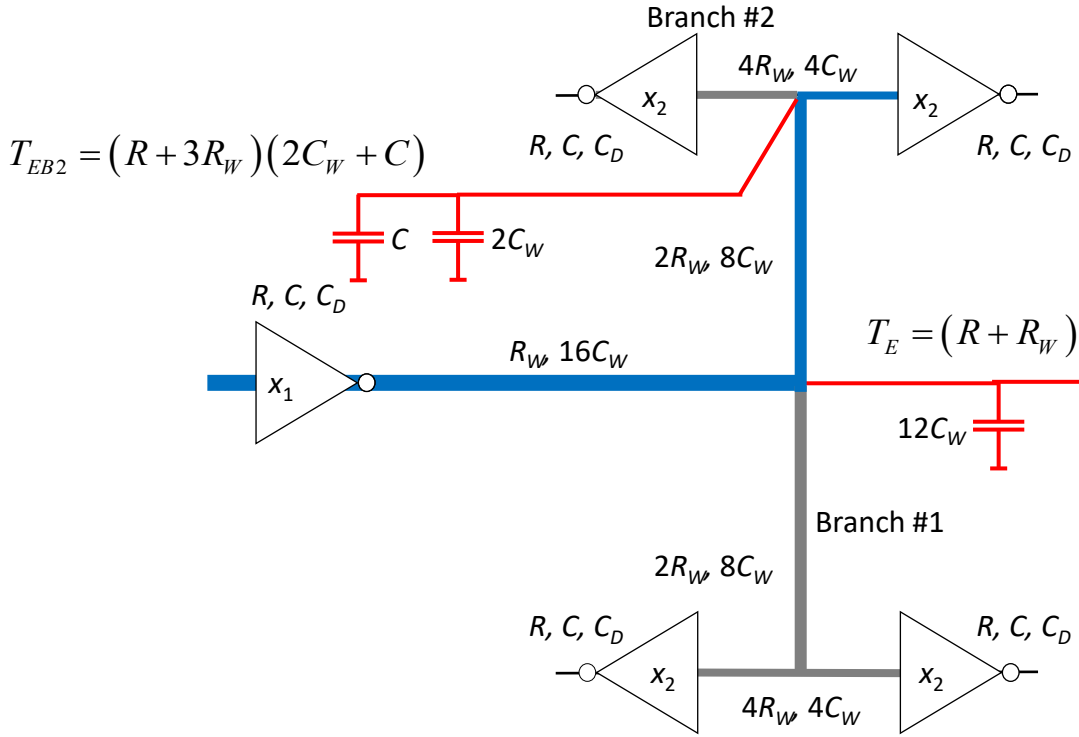


# How about influence of branches?



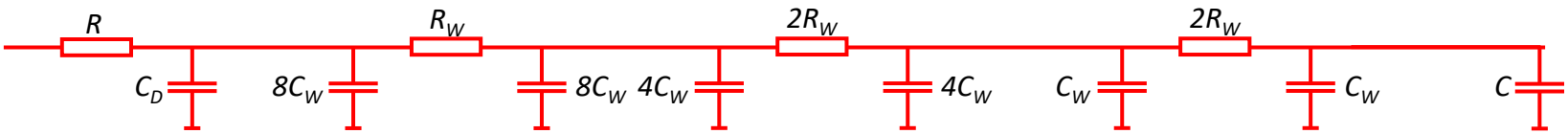

The Elmore time constant $T_E$ is found by multiplying each $R$ with its downstream $C$

Simplify: $T_E = R(C_D + C) + 26RC_W + 5R_WC + 32R_WC_W$



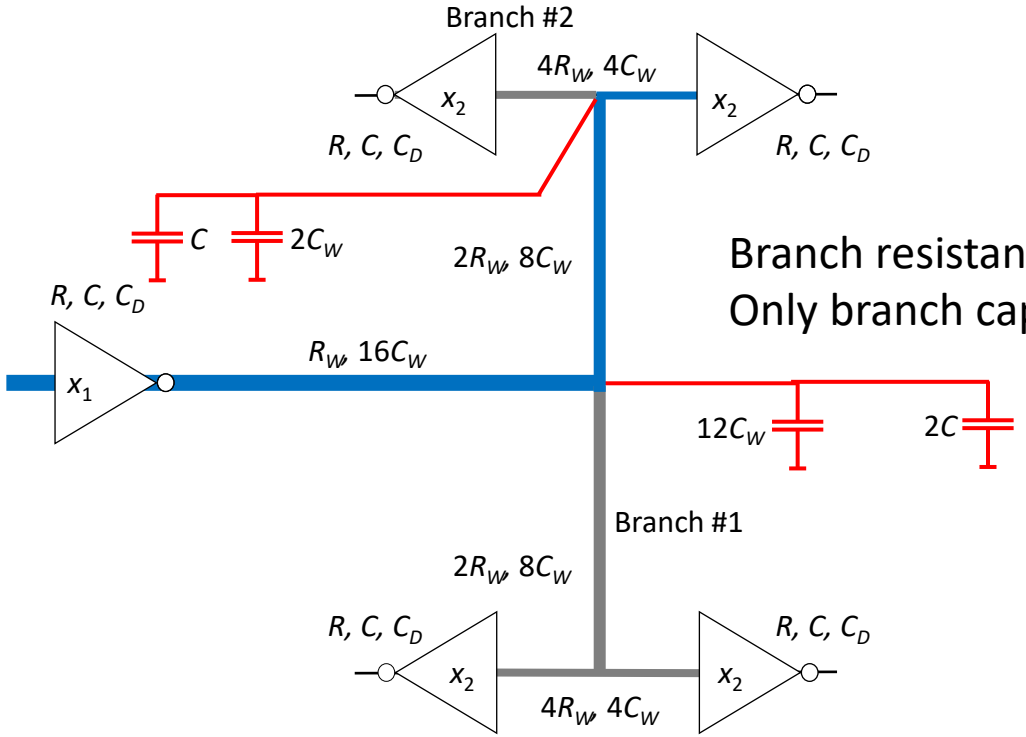

How about the branches, what is their influence on the Elmore time constant?

# Adding the influence of branches




$$T_E = R\left(C_D + C\right) + 26RC_W + 5R_WC + 32R_WC_W$$ w/o branches

$$T_E = R\left(C_D + 4C\right) + 40RC_W + 10R_WC + 40R_WC_W$$ w branches




Branch resistances are neglected!
Only branch capacitances matter!

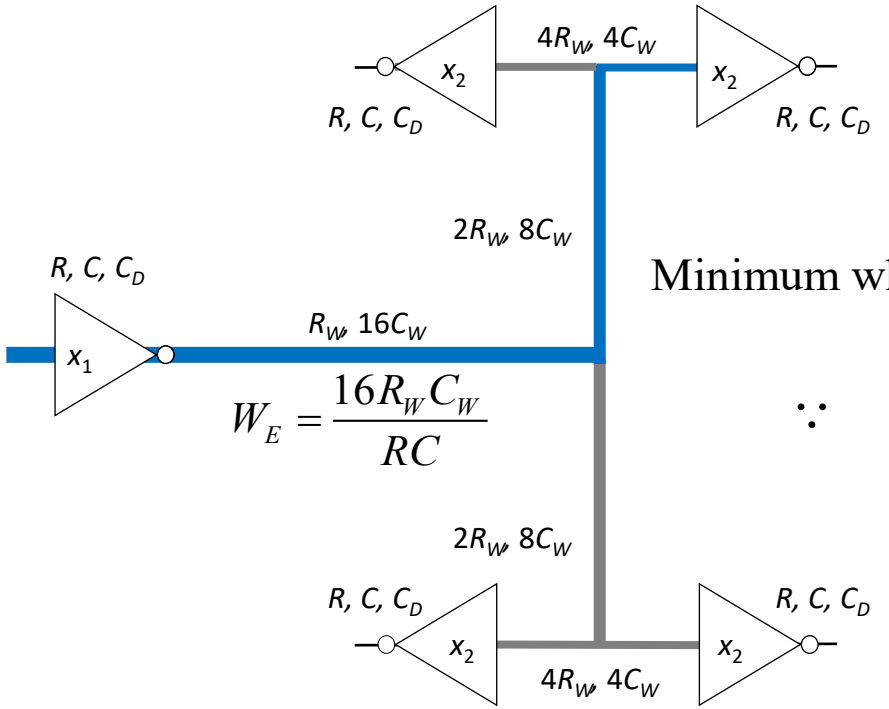
# H-tree clock distribution

How to size driver inverter to minimize the time constant, and hence the wire delay?

Rewrite Elmore time constant:

$$T_E = RC\left( p_{inv} + 4 + 40\frac{R_W C_W}{RC}\frac{R}{R_W} + 10\frac{R_W}{R} + 40\frac{R_W C_W}{RC} \right) =$$

$$= RC\left( p_{inv} + 4 + \frac{10}{4}W_E\frac{R}{R_W} + 10\frac{R_W}{R} + \frac{10}{4}W_E \right) \text{ using } W_E = \frac{16R_W C_W}{RC}$$




Minimum when $\frac{\partial T_E}{\partial R} = \frac{10}{4}\frac{W_E}{R_W} - 10\frac{R_W}{R^2} = 0$

$\because$ or $R = \frac{2R_W}{\sqrt{W_E}}$

$W_E = \frac{16R_W C_W}{RC}$

# Conclusion

- Introduction to interconnect
- Defining the sheet resistance [in ohms per square, $\Omega/\square$]
- Discussing the importance of interconnect
- Introduced a distributed wire RC model, the $\pi$-model
- Discussed the relevance of a delay model assuming the existence of a dominant time constant
- Minimizing wire delay by repeater insertion
- The Elmore model – a generalized delay model
- How to handle the influence on delay of branches
- Questions and answer session