MCC092
Postlab lab 3 &
prelab lab 4
and a few other things

2017-09-28

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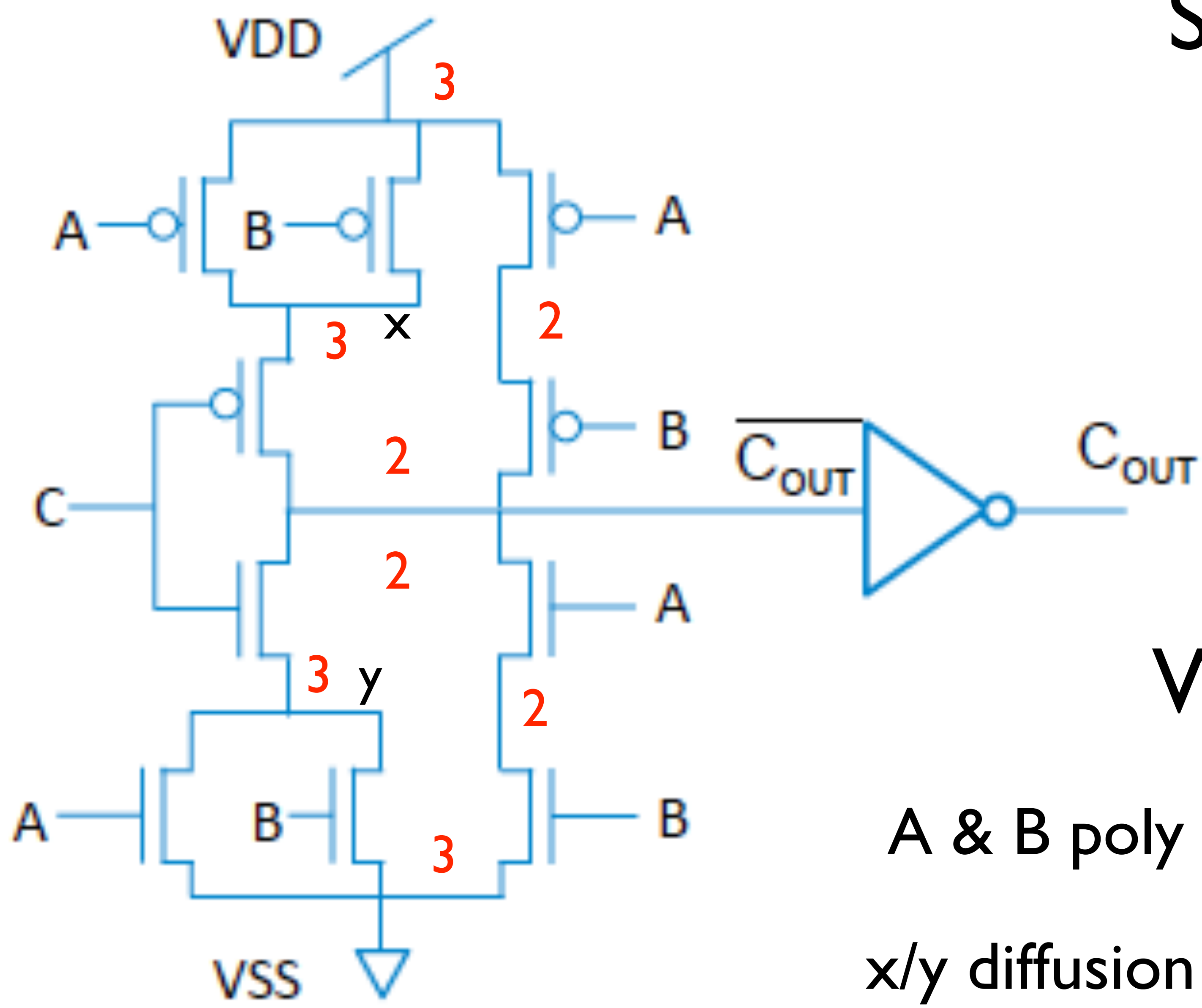
Lab 3

- Do your design on paper first.
- Euler analysis is good - but there may be multiple solutions.
- Stick diagrams help.
  - If you must revise your solution do that on paper first!

Improvements

- Add the info that is on the web in the memo, since many missed it.
- Even more clearly point out that you have to use ESC to deselect a tool.

Euler path



Same topology in n-net and p-net.

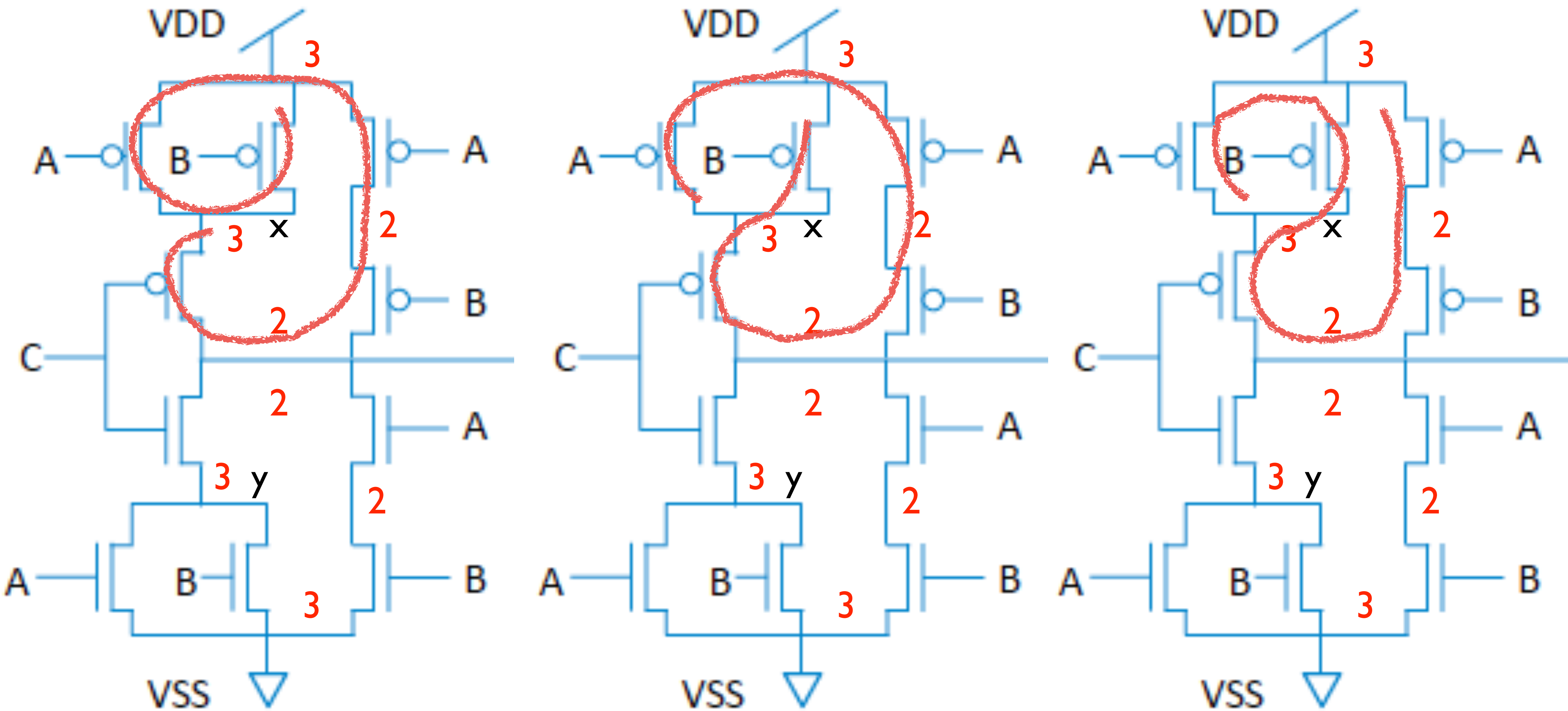
Odd order nodes: Start/end in x/y and V_{DD}/V_{SS}

Which one too choose?

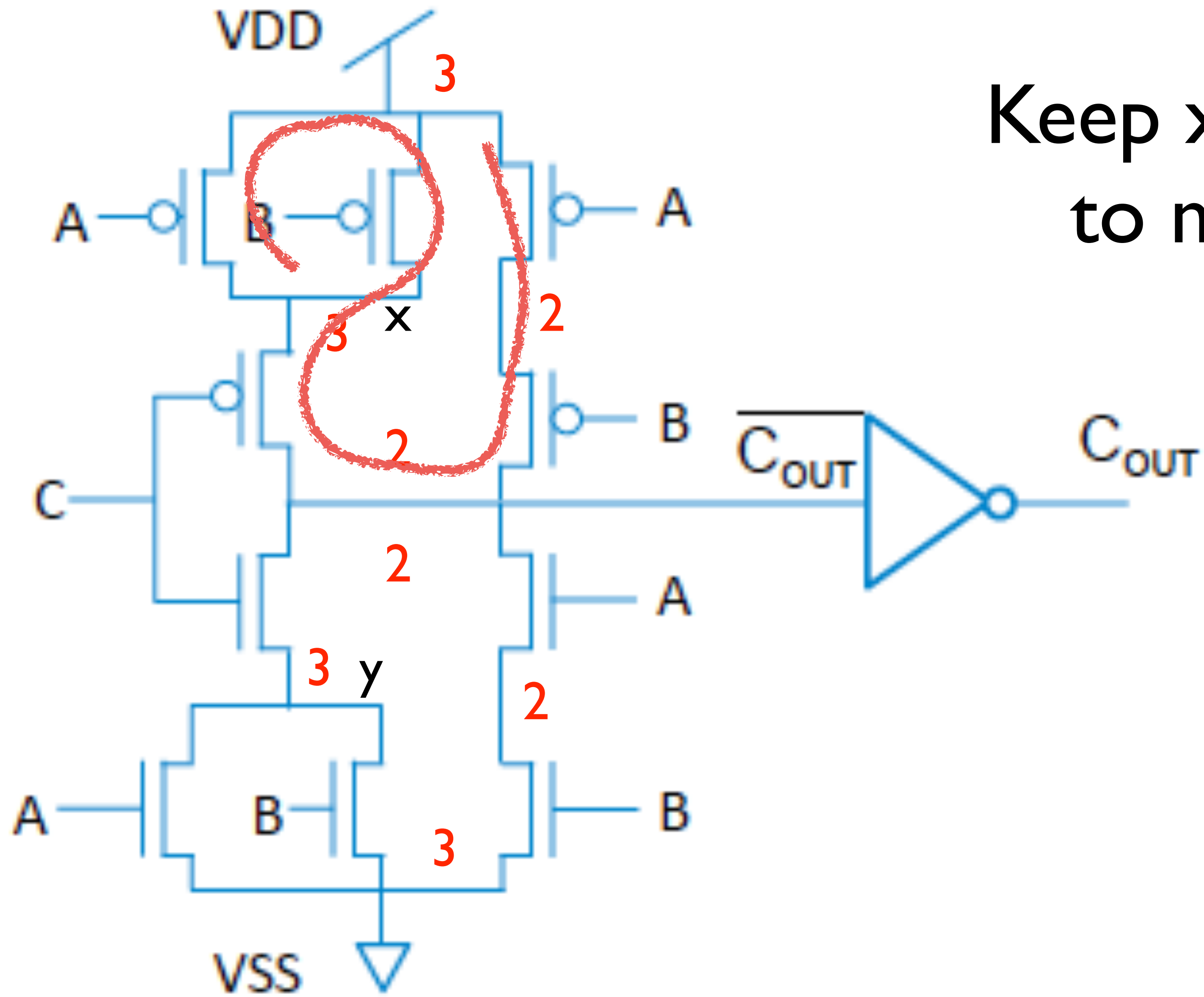
A & B poly lines must be connected

x/y diffusion areas must be connected with metal-1 wire since their node order is > 2

Three Euler paths



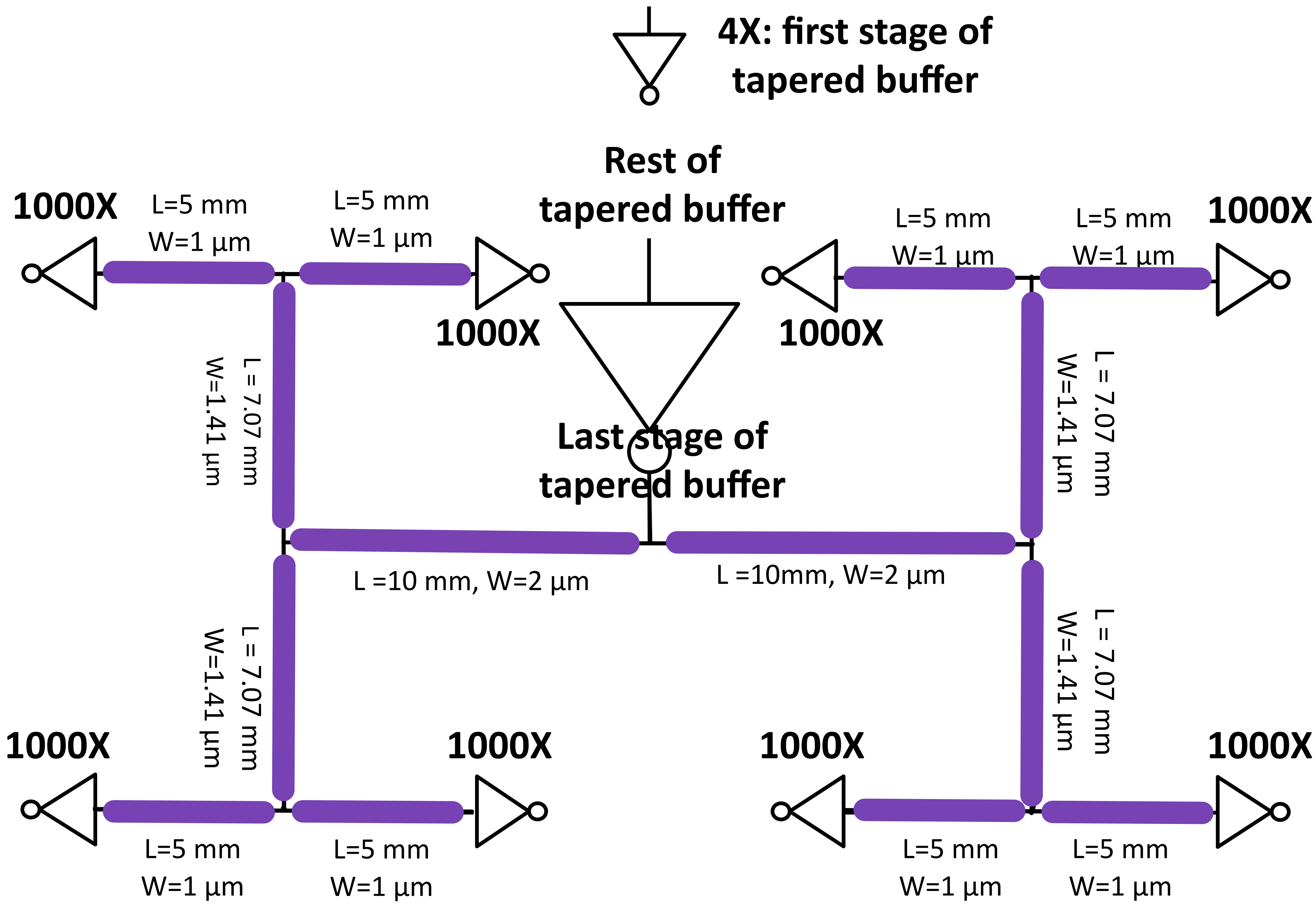
Best Euler path



Best solution(s):
Keep x/y diffusion areas close to minimize wire lengths

Thus best solution(s):
A B C B A
A B C A B

Prelab 4



4X: first stage of
tapered buffer
Rest of
tapered buffer
Last stage of
tapered buffer
1000X
L=5 mm
W=1 μm
L=5 mm
W=1 μm
1000X
1000X
L=5 mm
W=1 μm
L=5 mm
W=1 μm
1000X
1000X
L = 7.07 mm
W=1.41 μm
L = 7.07 mm
W=1.41 μm
L =10 mm, W=2 μm
L =10mm, W=2 μm
L = 7.07 mm
W=1.41 μm
L = 7.07 mm
W=1.41 μm
1000X
1000X
1000X
1000X
L=5 mm
W=1 μm
L=5 mm
W=1 μm
L=5 mm
W=1 μm
L=5 mm
W=1 μm

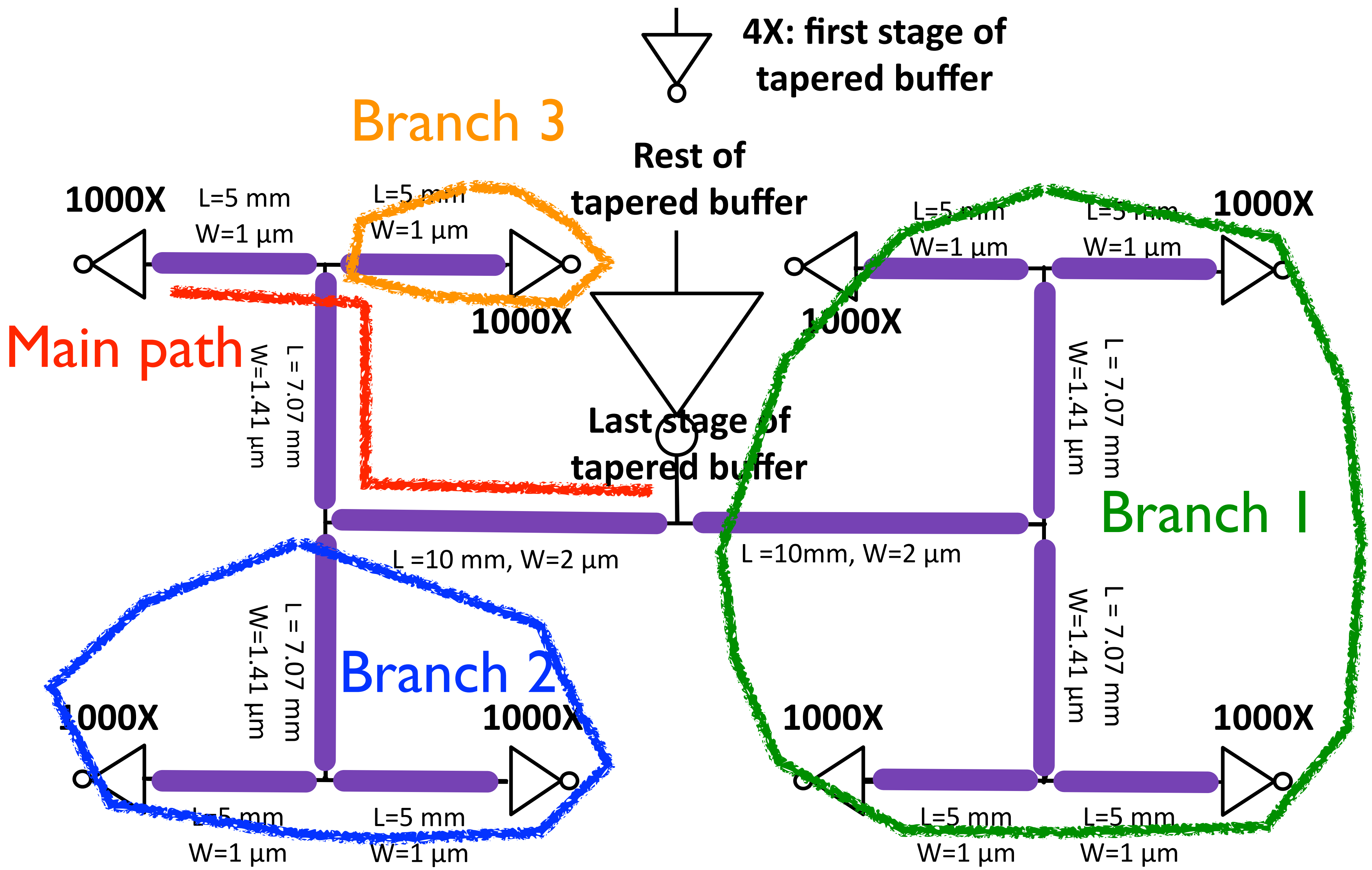
Prelab 4, calculations part 1

- Each wire segment = one pi link
- First, R_{SH}=0, that is whole tree is one big capacitance
- Design a tapered buffer to drive this huge capacitance

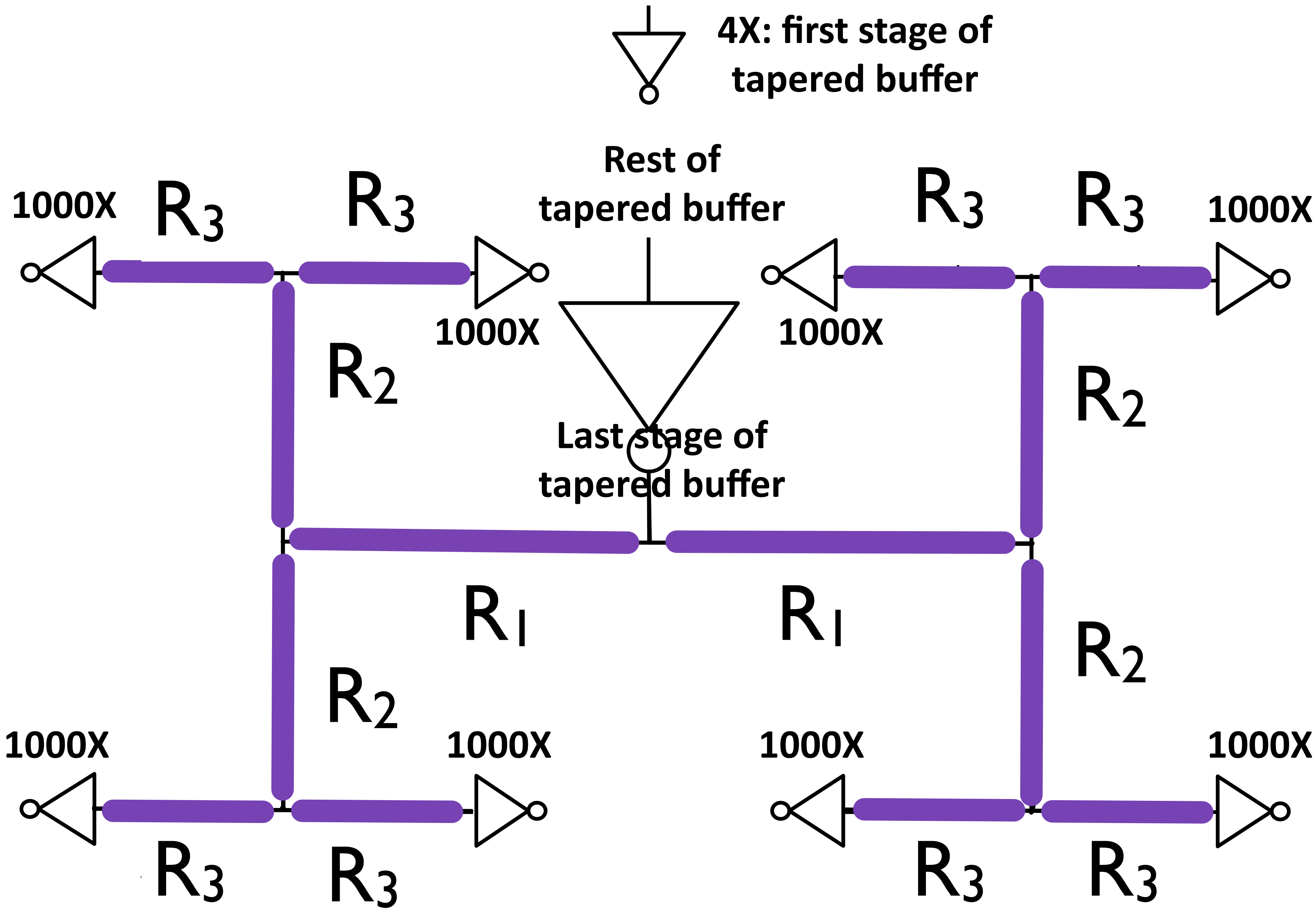
Prelab 4, calculations part 2

- Assume $R_{SH} \neq 0$
- Calculate delay to leaves using Elmore model
- Collapsed tree helps!

H-tree branching

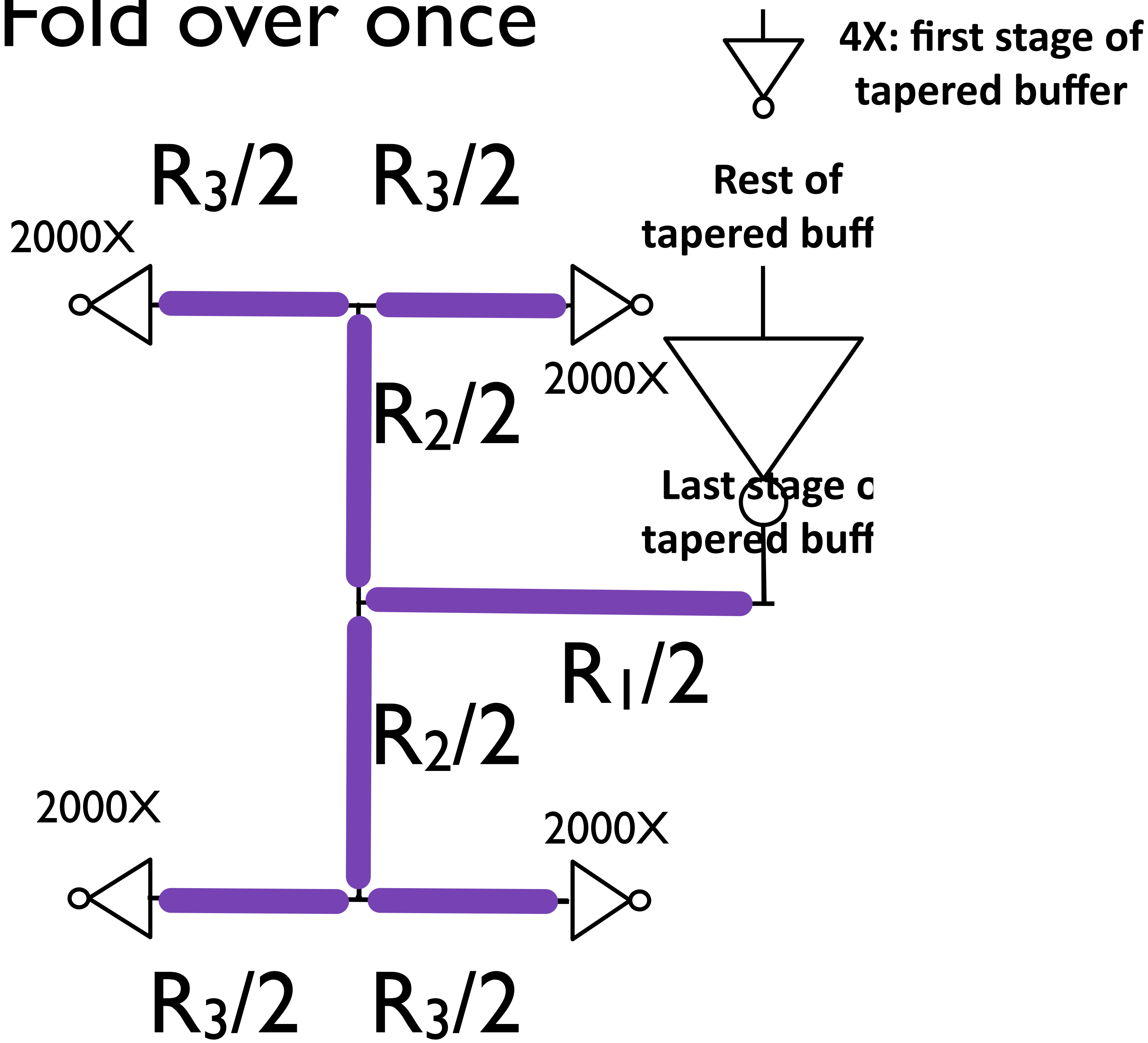


H-tree collapsing



H-tree collapsing

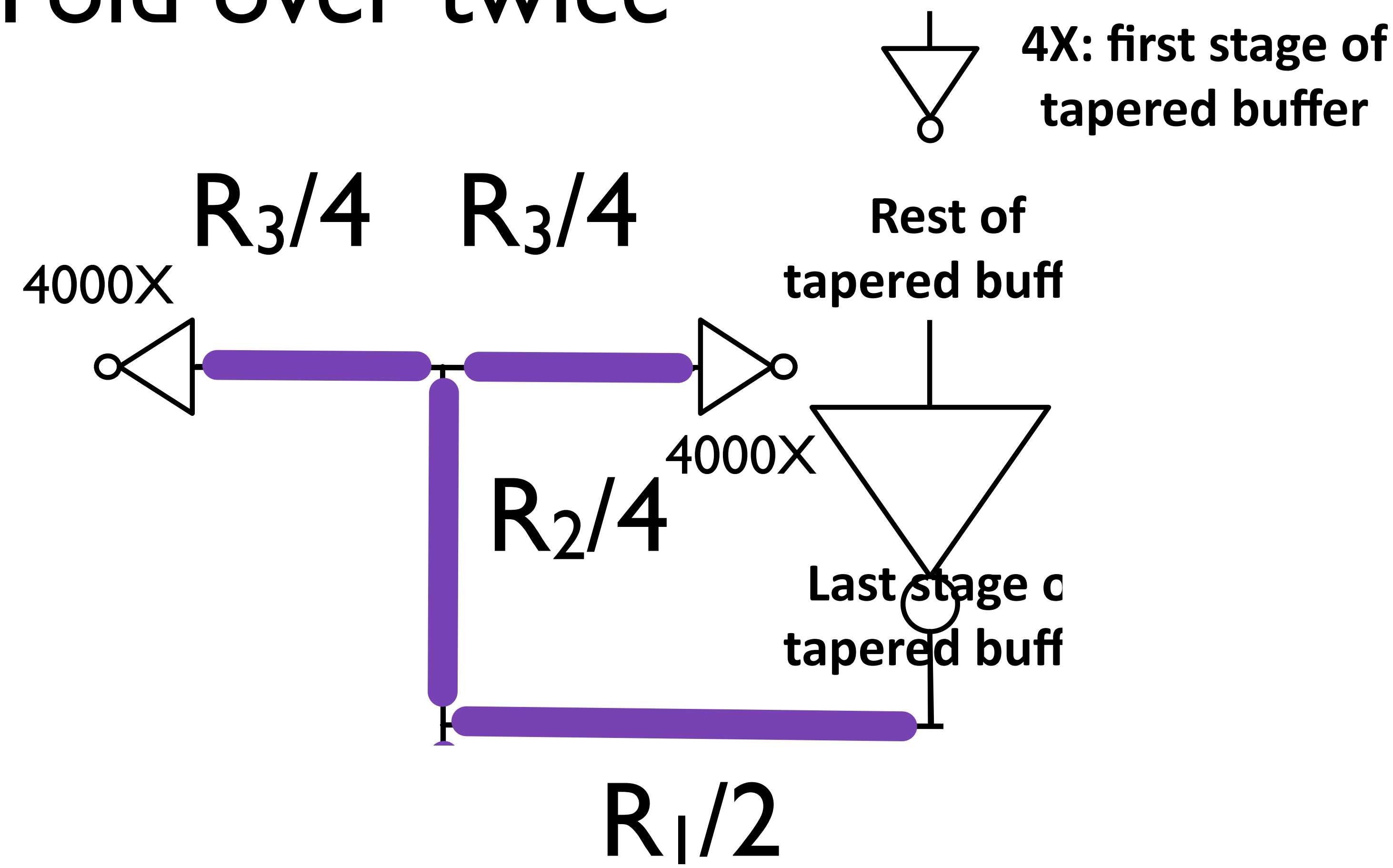
Fold over once



And wire capacitances are added

H-tree collapsing

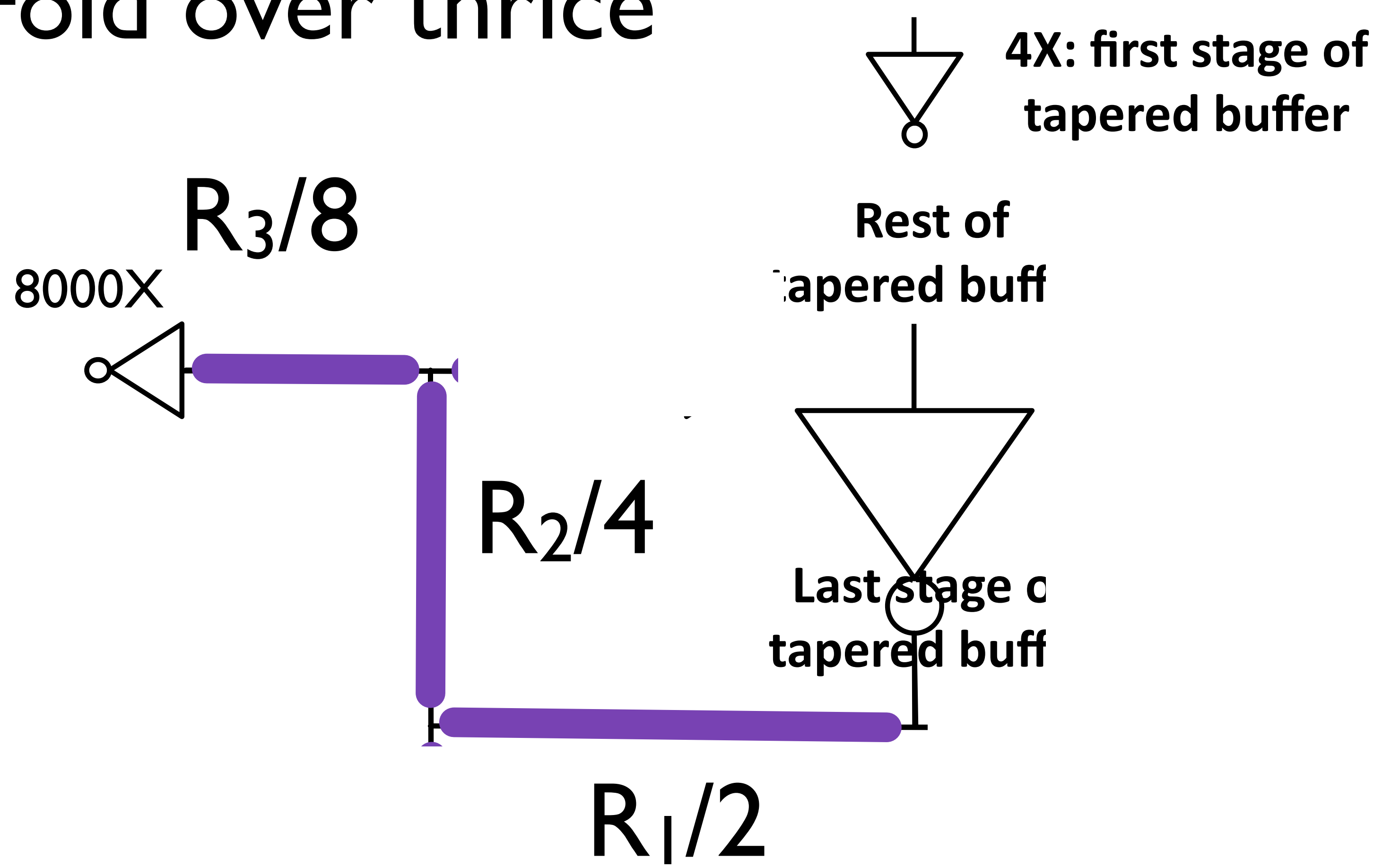
Fold over twice



And wire capacitances are added again

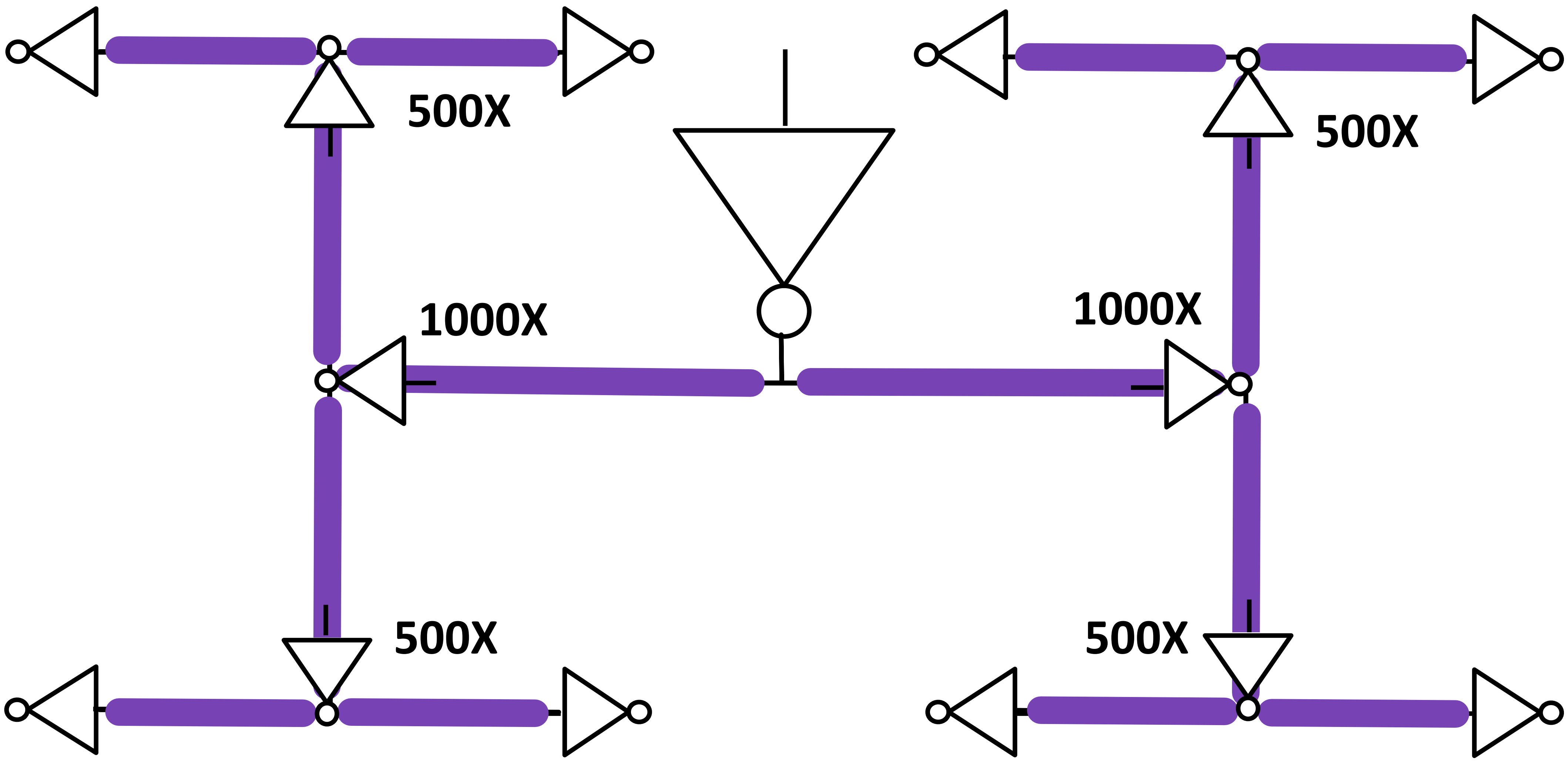
H-tree collapsing

Fold over thrice



And wire
capacitances
are added again

Prelab 4, calculations part 3



Prelab 4

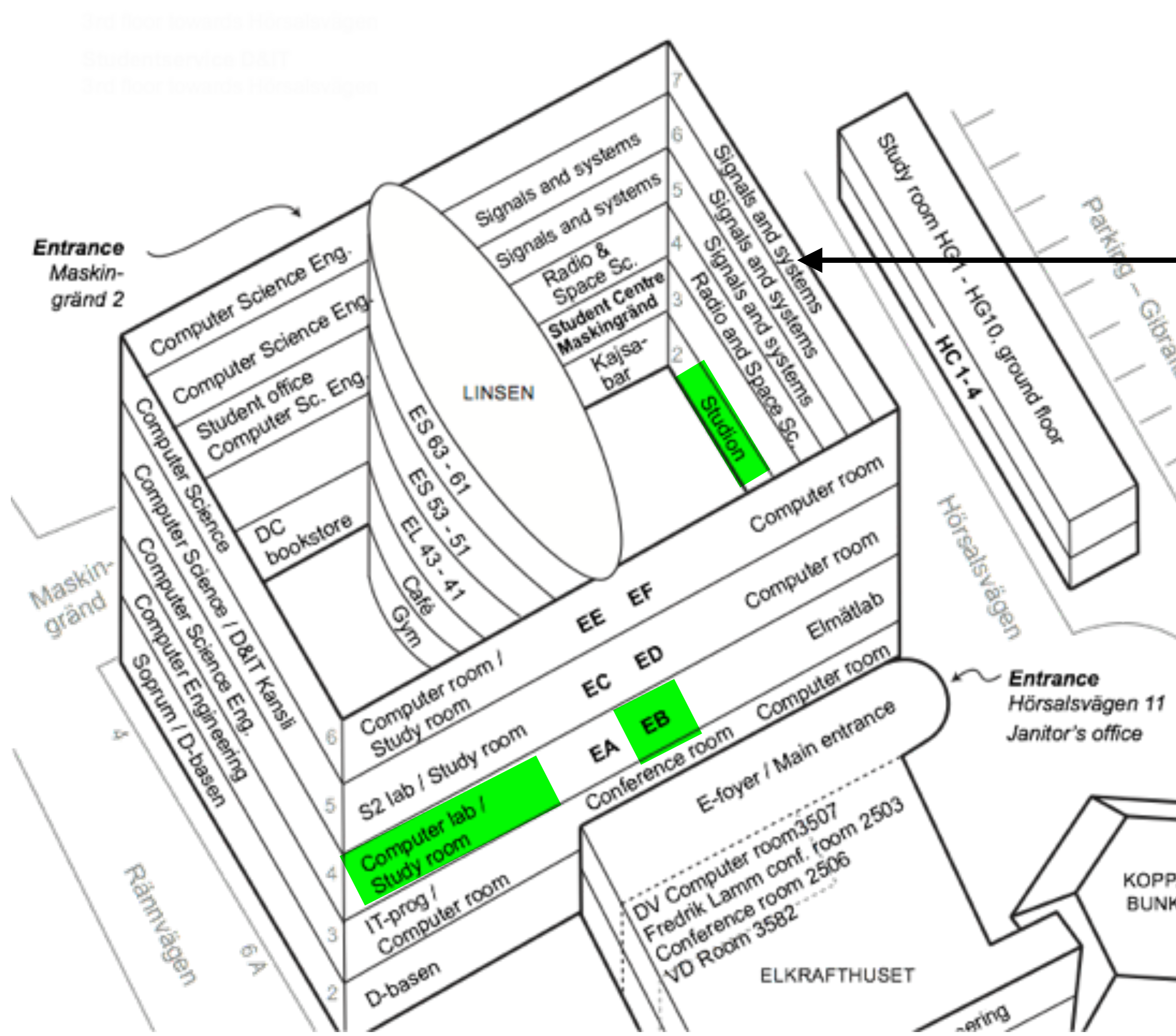
- We will use Spectre with command-line input.
- Write the Spectre input file properly!
- Otherwise you have to spend valuable lab time doing that!
- Consultation time after class and tomorrow: Sept 29: 9-10 (Note! I may be a little late).

Lab make-up session

- Monday Oct. 9 8.00-11.45.

Adder lecture/exercises

- Tuesday October 3 13.15-15.00 in E-studion.
- Tuesday October 10 13.15-15.00 in E-studion.

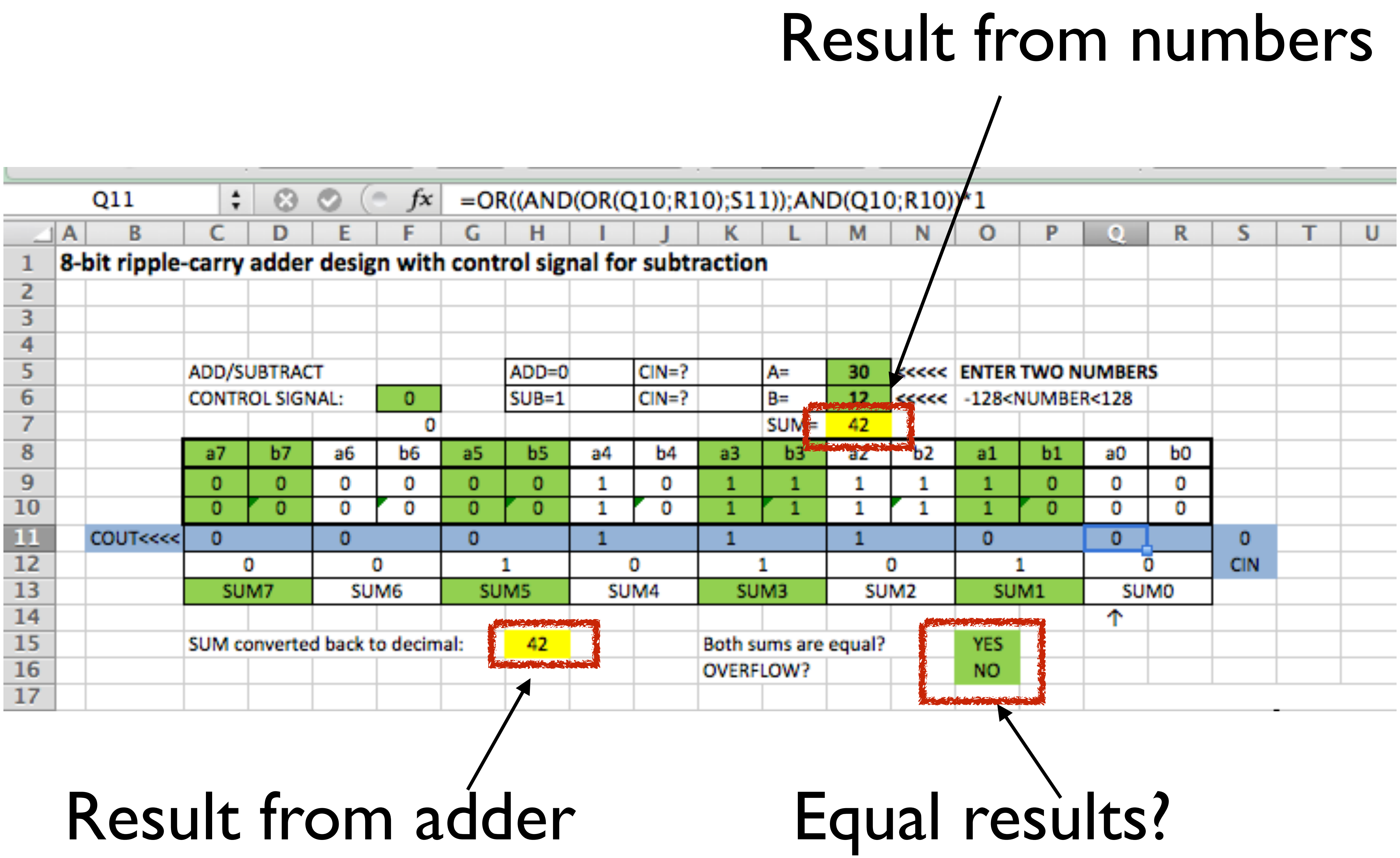


Entry is from Hörsalsvägen

Adder lecture/exercise preparation

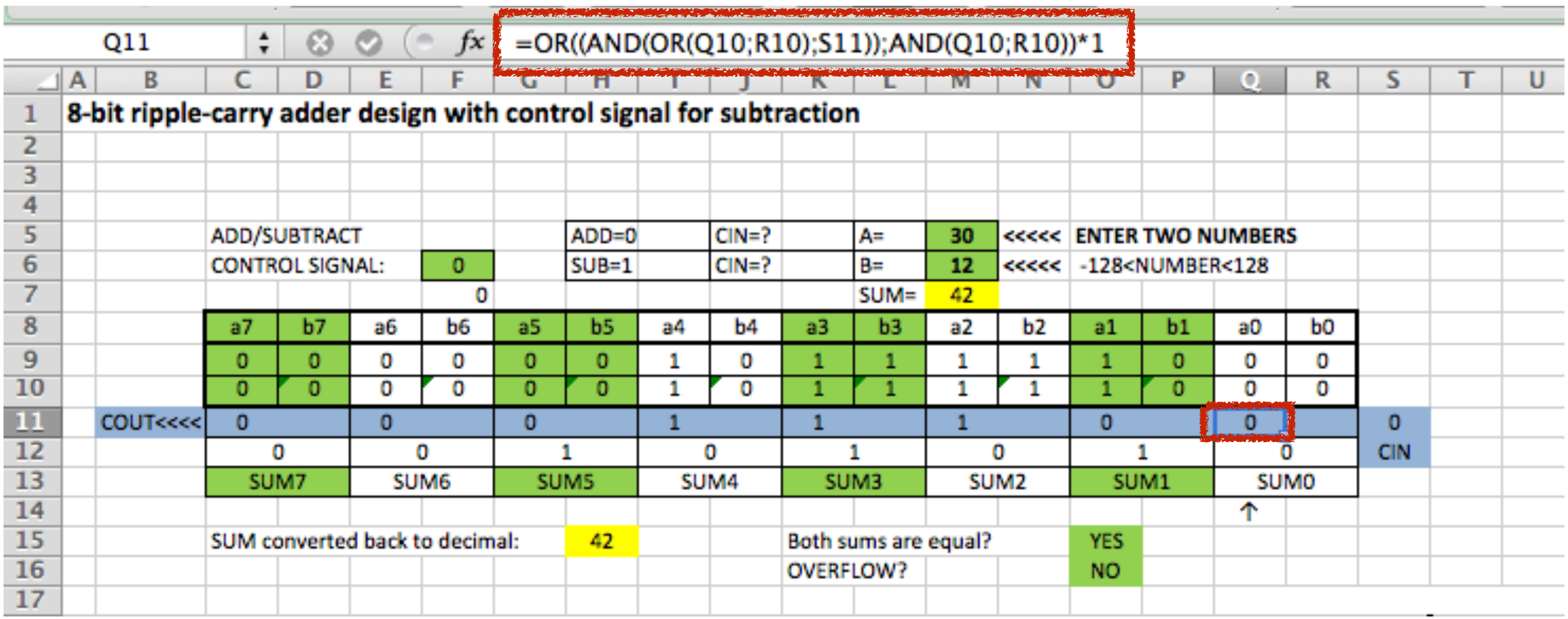
- If you do not have access to the book download **chapter 11** of W&H from cmosvlsi.com. Use“Look inside” to the left.
- Read sections 11.2.1, 11.2.2 (for Oct. 3 up to 11.2.2.8 for Oct. 10 the rest of 11.2.2) Skip any optional parts.
- Find excel (either on Chalmers PC:s or download it on your own computer - see later slides).
- Download example file: Excel_examples 2017.xslx and open in Excel. Three examples:
    1. 8-bit zero-detect circuit as ILA
    2. 8-bit comparator circuit as ILA
    3. 8 bit ripple-carry adder with negation

Ripple-carry adder



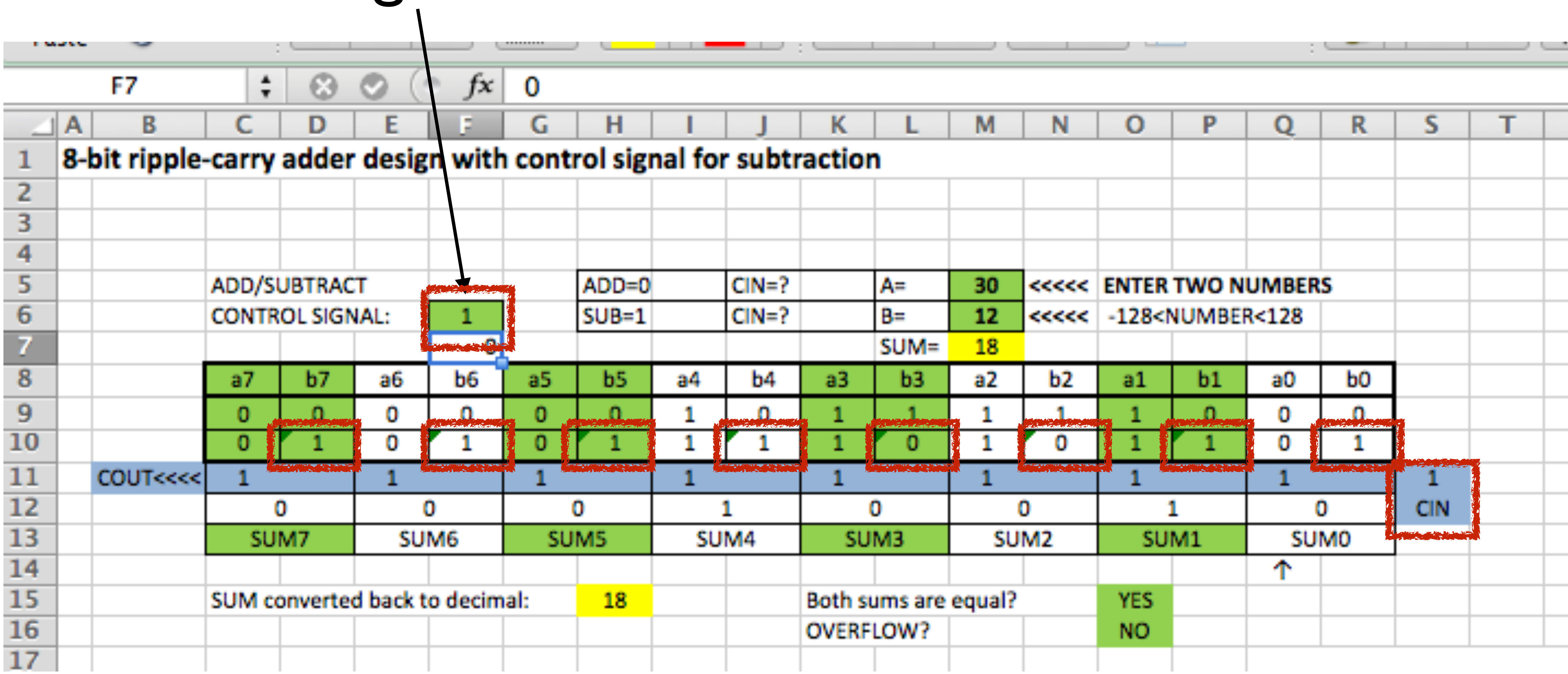
Addition

Expression for C_{out0}



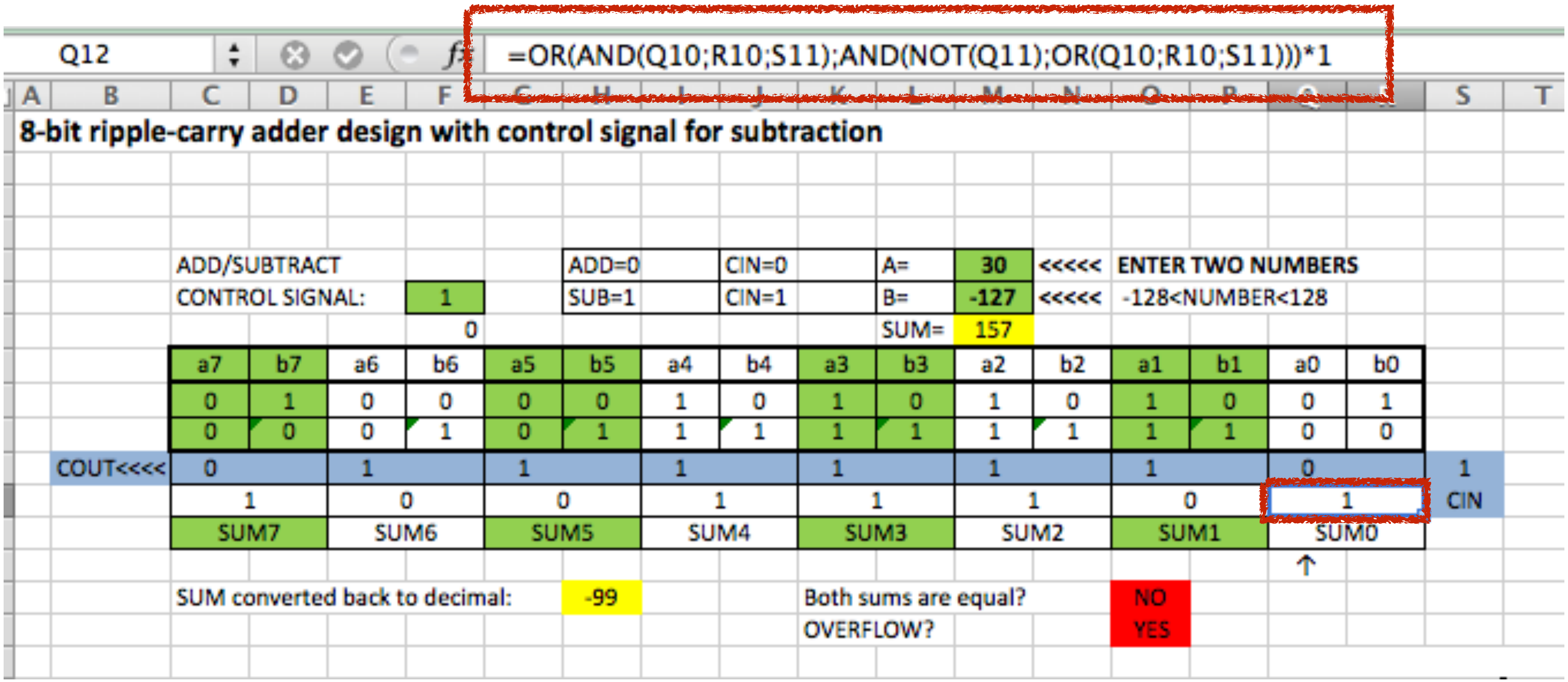
Subtraction

Control signal



Overflow

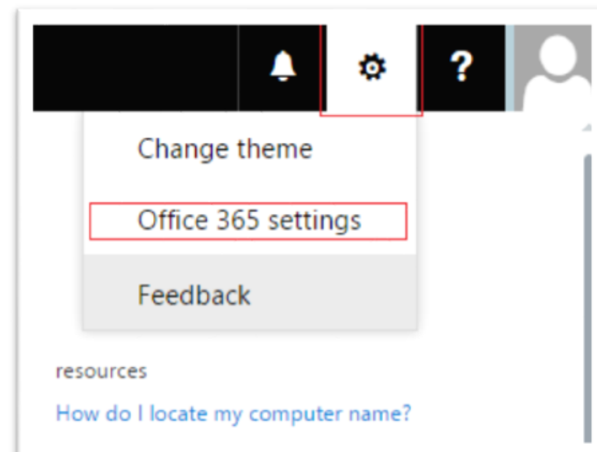
Expression for SUM_0



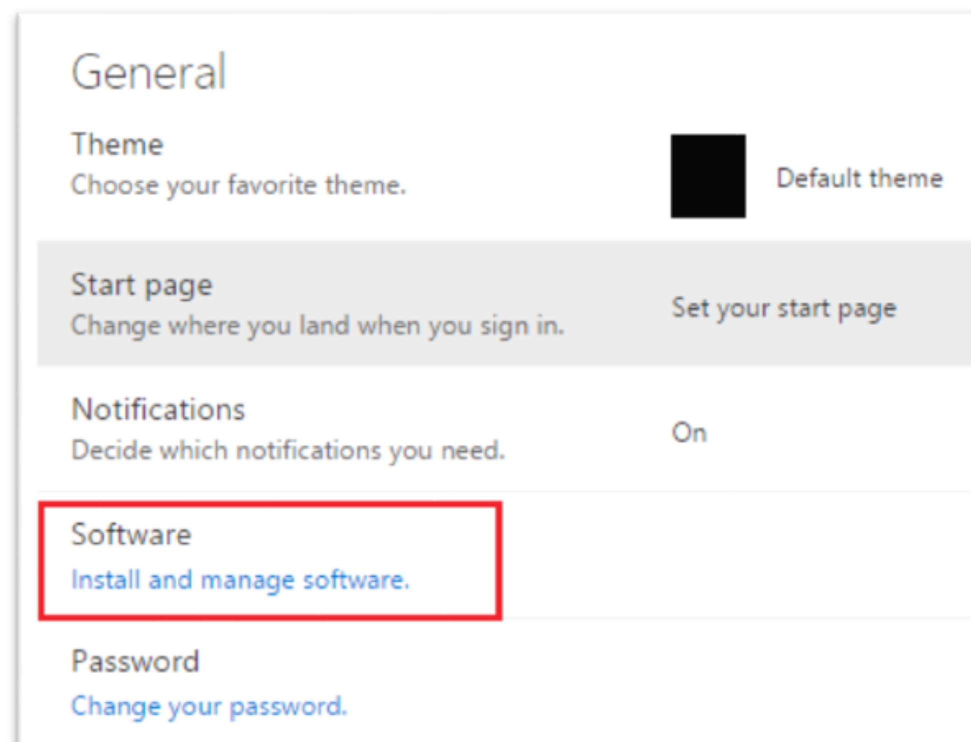
How to download Office 365 on your own PC (1)

1. Go to: https://outlook.com/net.chalmers.se

2. Click on the cogwheel, select "Office 365 settings"



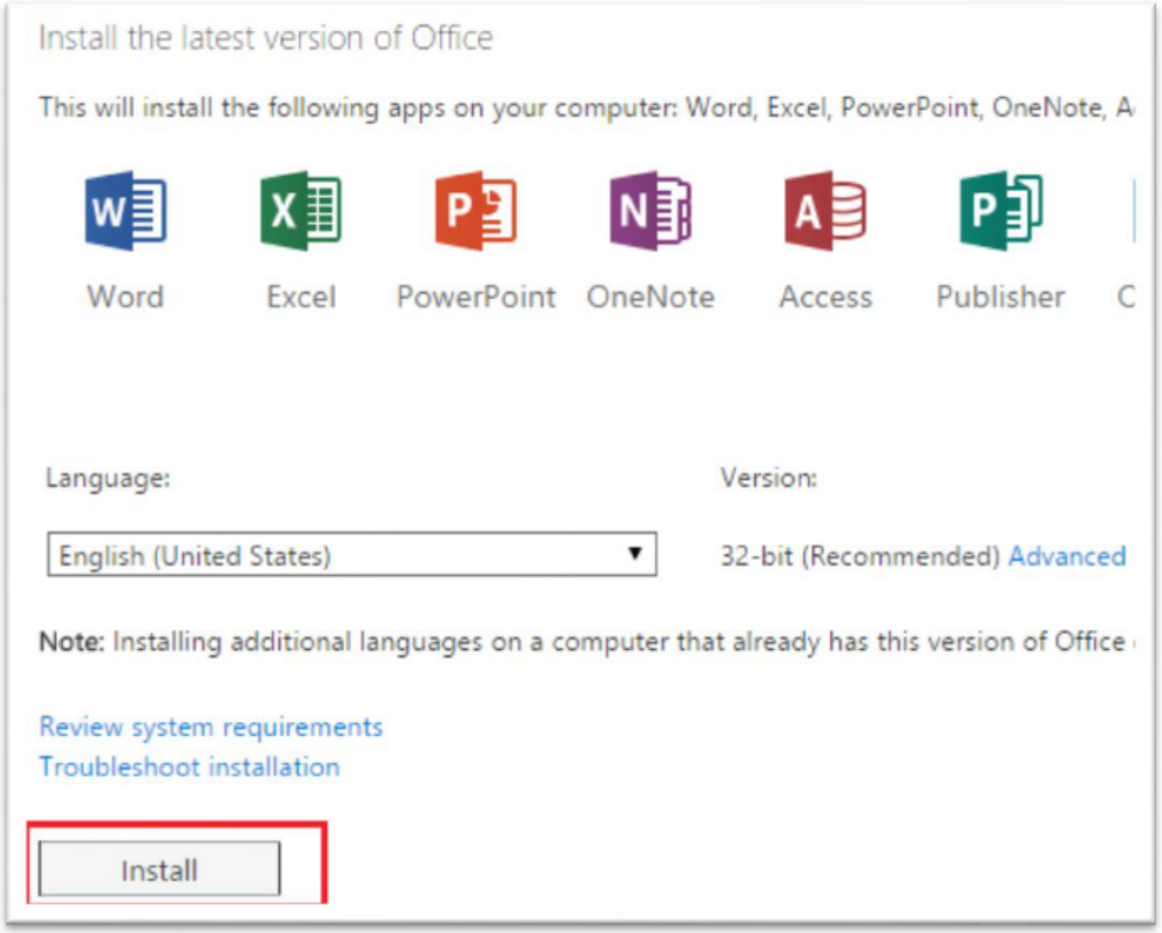
3. Under "Software" click on "Install and manage software"



How to download Office 365 on your own PC (2)

4. Download the installation program:

5. When you are asked to activate the license log in with CID@net.chalmers.se



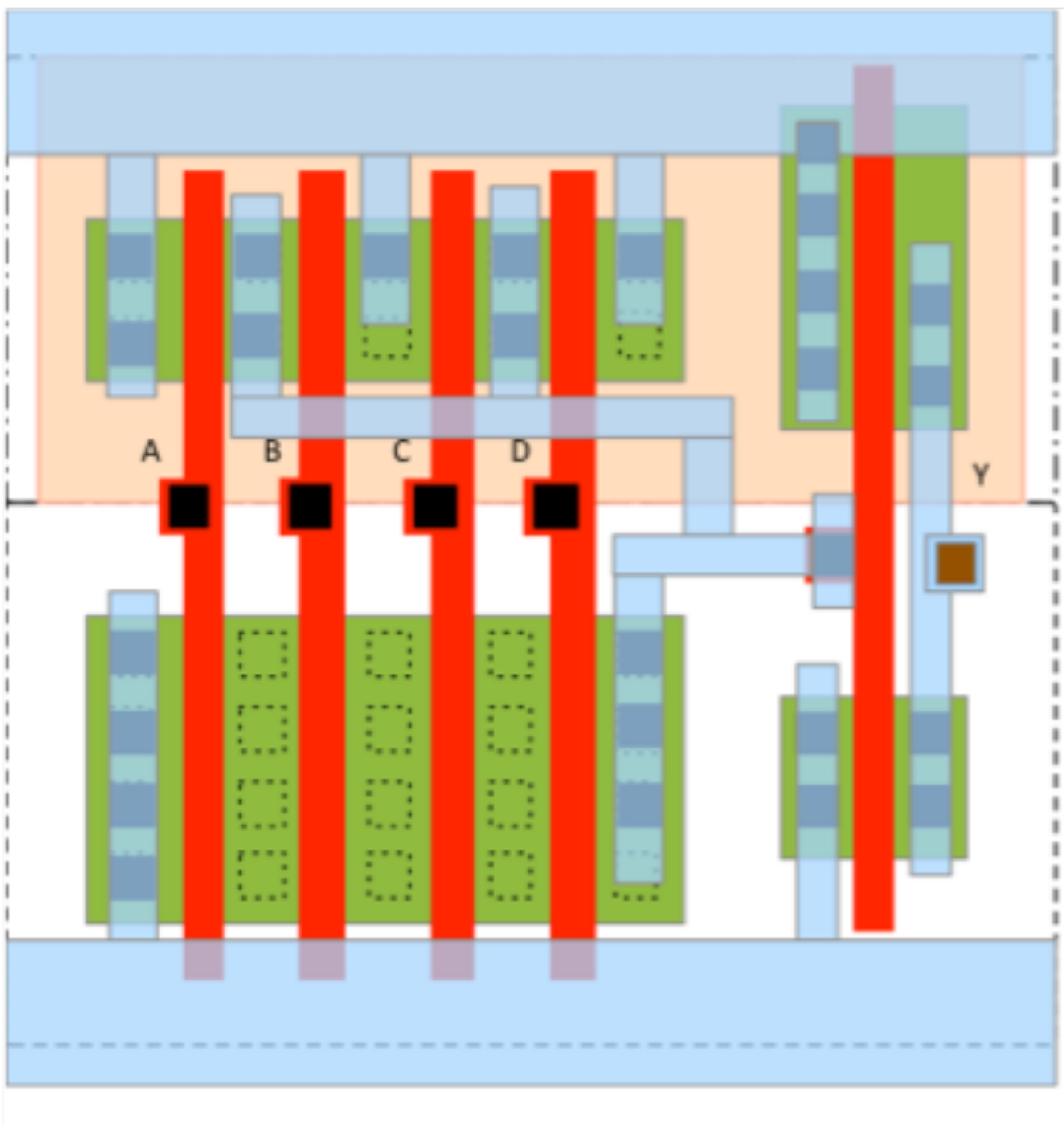
Note! Only one installation per CID is allowed

Question related to quiz: g and p for sequence of gates

- Our linear model for normalized delay:
  - $d = g \times h + p$
- p is constant part
- g part depends linearly on load capacitance:
  - $g \times h = g \times C_L/C_{in}$

Exercise 8.2
solutions from last week

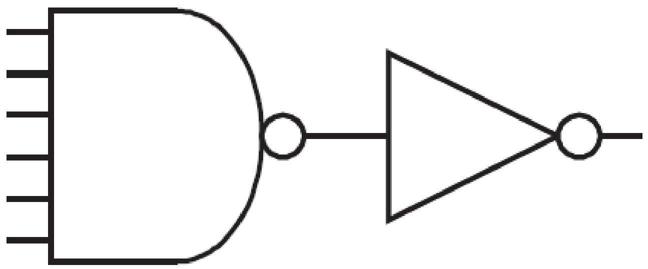
a)



b)

$g_{NAND4} = 2$
from layout:
$p_{NAND4} = 8/3$

Problem 8.2 c)



$g_{NAND4} = 2$ $g_{INV} = 1$

$p_{NAND4} = 8/3$ $p_{INV} = 1$

Transistor sizes from layout:

$C_{NAND4} = C+2C$

$C_{inv} = 2C + C$

$\Rightarrow C_{inv} = C_{NAND4}$

$h_{NAND4} = 1$

$h_{inv} = C_L/C_{inv} = C_L/C_{NAND4}$

$d = 2 \times 1 + 8/3 + 1 \times C_L/C_{inv} + 1$

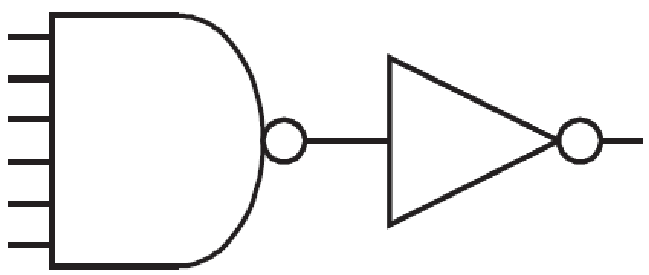
$d = 5\ 2/3 + C_L/C_{inv}$

$d = 5\ 2/3 + C_L/C_{NAND}$

thus, $p_{AND4} = 5\ 2/3$

$g_{AND4} = 1$

What if we size inverter up by 2?



$g_{NAND4} = 2$ $g_{INV} = 1$

$p_{NAND4} = 8/3$ $p_{INV} = 1$

New gate sizes:

$C_{NAND4} = 3C$

$C_{inv} = 6C$

$\Rightarrow C_{inv} = 2C_{NAND4}$

$h_{NAND4} = 2$

$h_{inv} = C_L/C_{inv} = C_L/2C_{NAND4}$

Note (afterwards): the ratio C_{inv}/C_{NAND4} can also be expressed with X ratio: X4/X2 =2 etc.

$$d = 2 \times 2 + 8/3 + 1 \times C_L/C_{inv} + 1$$

$$d = 7\ 2/3 + C_L/C_{inv}$$

$$d = 7\ 2/3 + C_L/2C_{NAND}$$

thus, $p_{AND4} = 7\ 2/3$

$g_{AND4} = 1/2$