

Lecture 11b

Metastability

2018-10-16

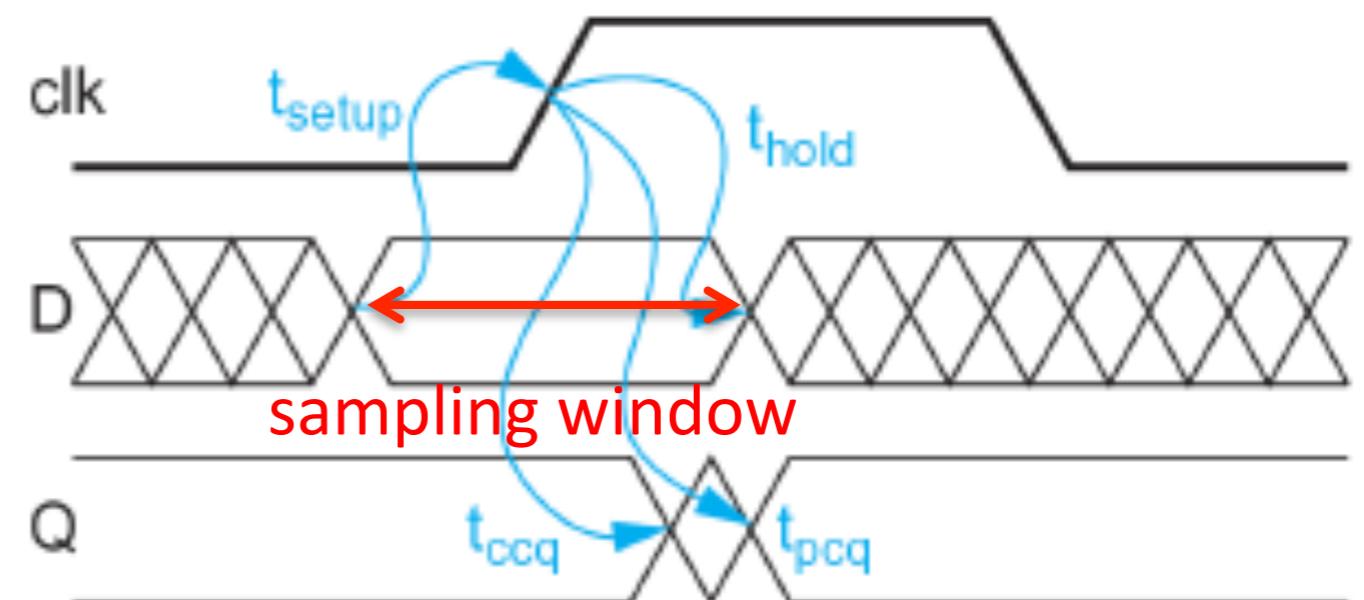
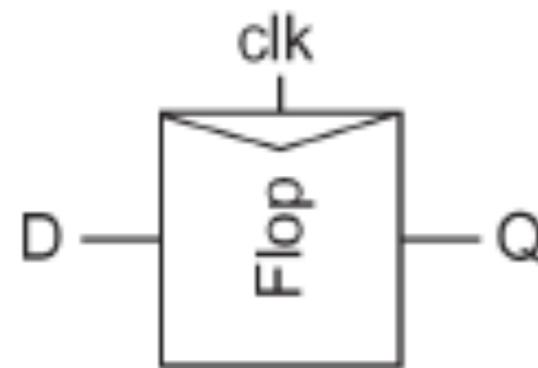
Why care?

- Digital abstraction:
 - All signals in a system must have a valid digital representation
- Consequence: Must reliably synchronize external events

Real world problem!

- Inputs from real world are usually not synchronous with system clock.
- Inputs from other synchronous systems are based on another system clock usually not synchronous with your system clock.
- They can switch during the **sampling window**.

The sampling window



What happens then?

- Received data may be neither 1 nor 0
- Or, data may be correct eventually but we do not know **when** it is correct.

The metastability equation

$$MTBF = \frac{e^{\frac{S}{\tau}}}{T_W f_c f_D}$$

MTBF is the figure of merit for synchronisation

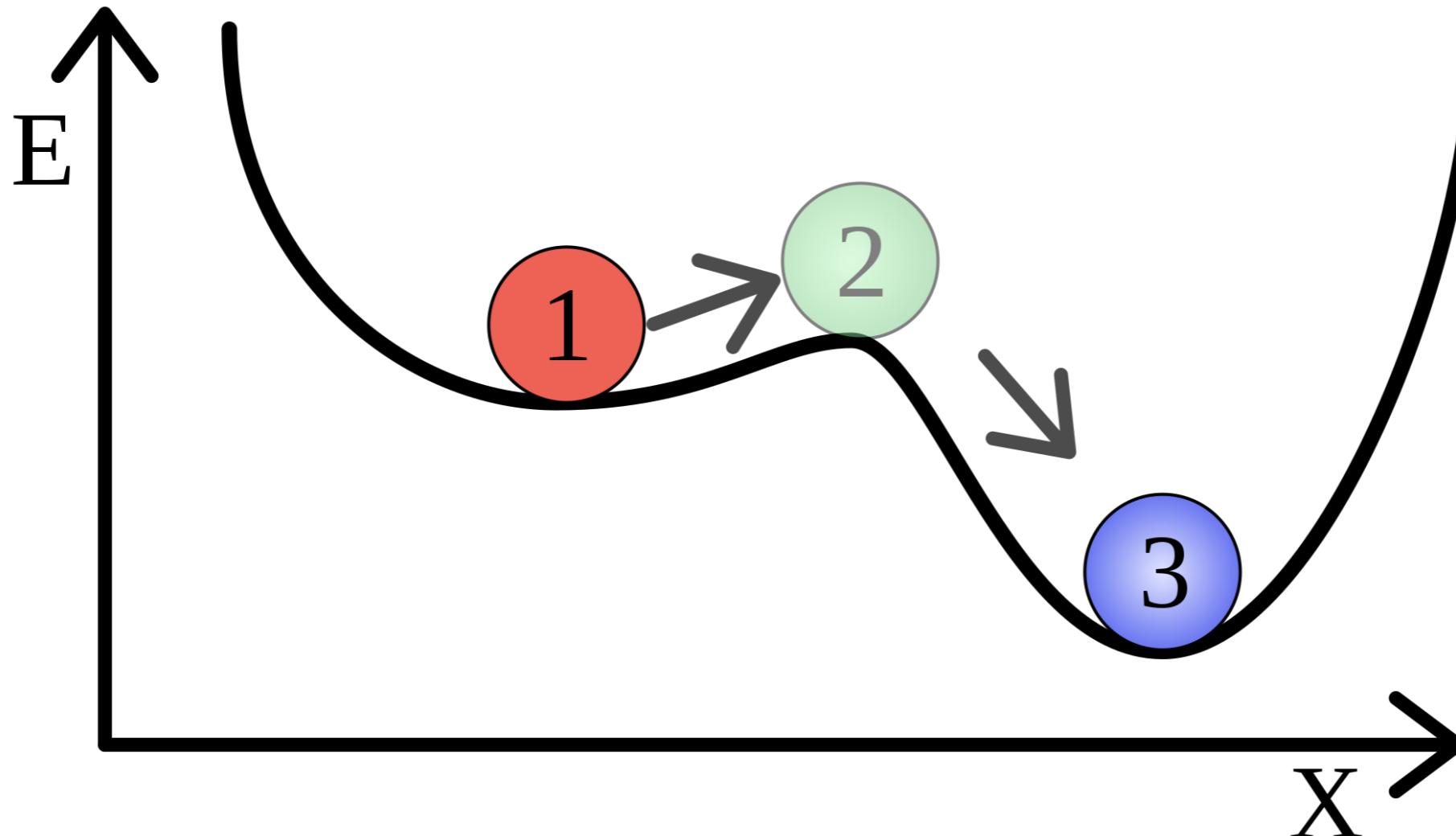
In this lecture we will derive this equation

See how problem can be alleviated

Derivation follows: “Metastability and Synchronizers: A tutorial” by R. Ginosar 2011

Paper is available in PingPong

Metastability

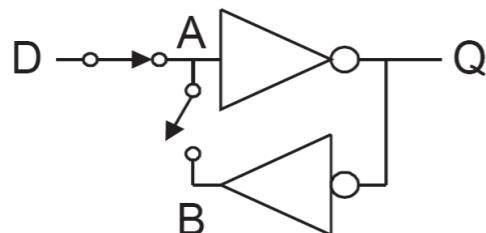


meta means “middle” or “in between”

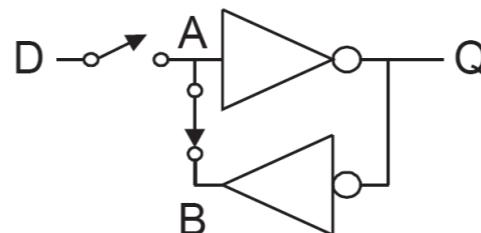
Figure: Wikimedia Commons. By Georg Wiora (Dr. Schorsch)

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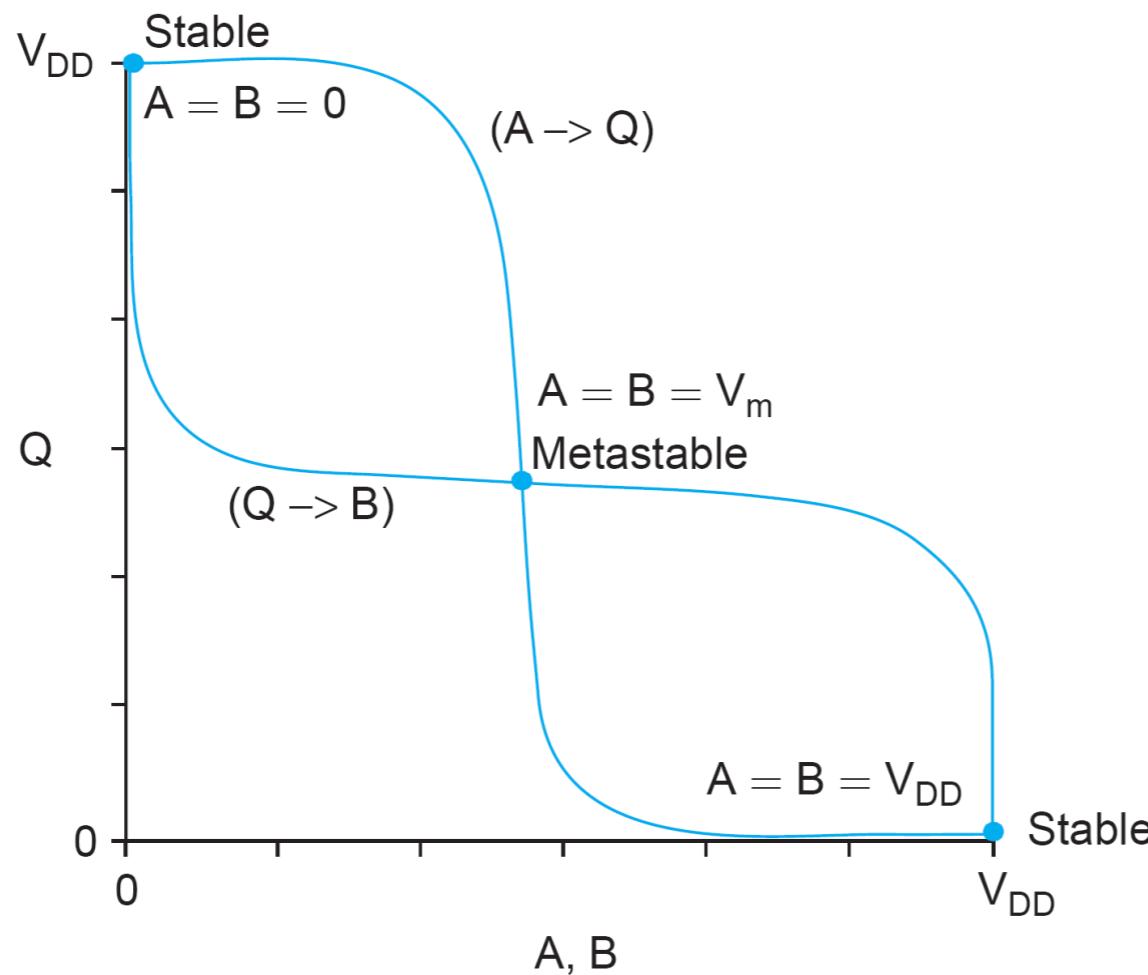
Metastability in latch



(a)

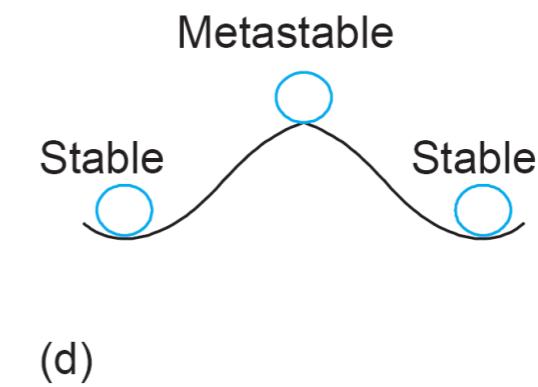


(b)



(c)

Figure: Weste & Harris
Fig. 10.42



(d)

Flip-flop = two latches

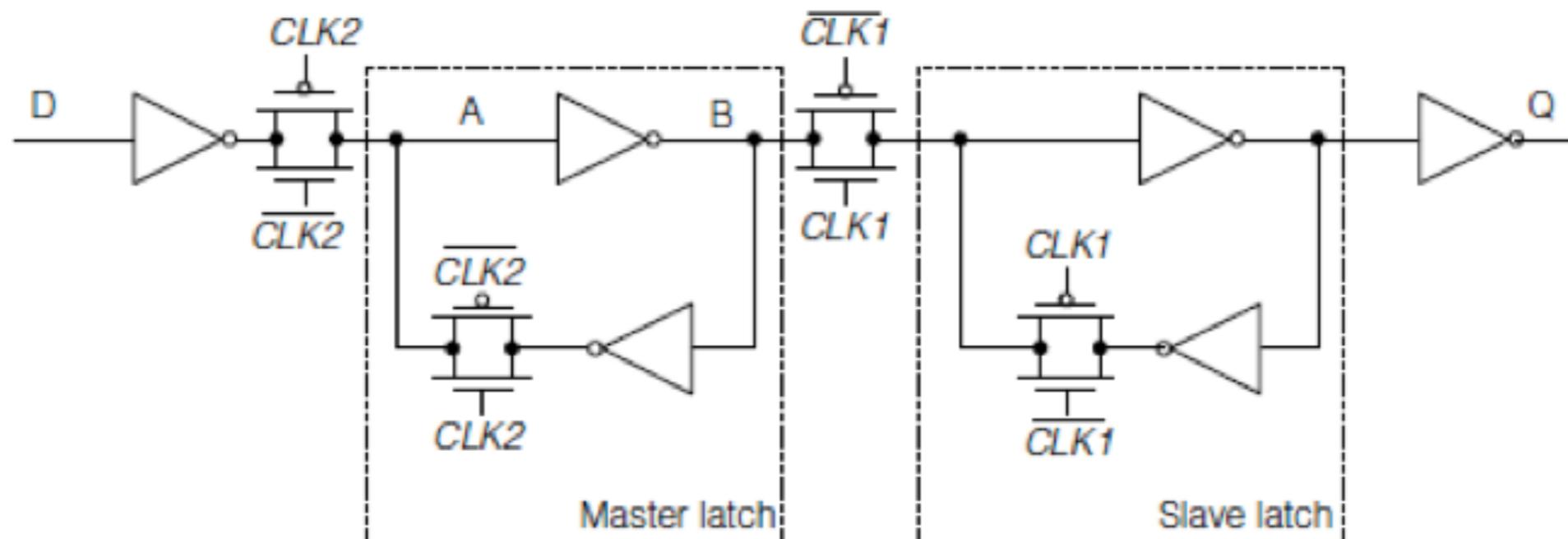
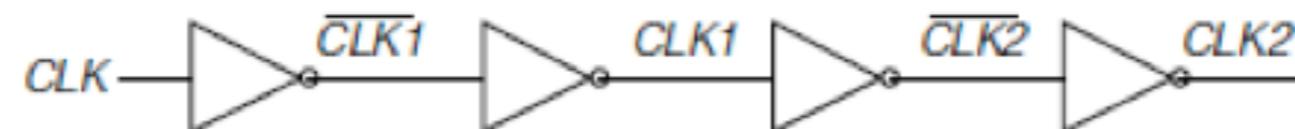


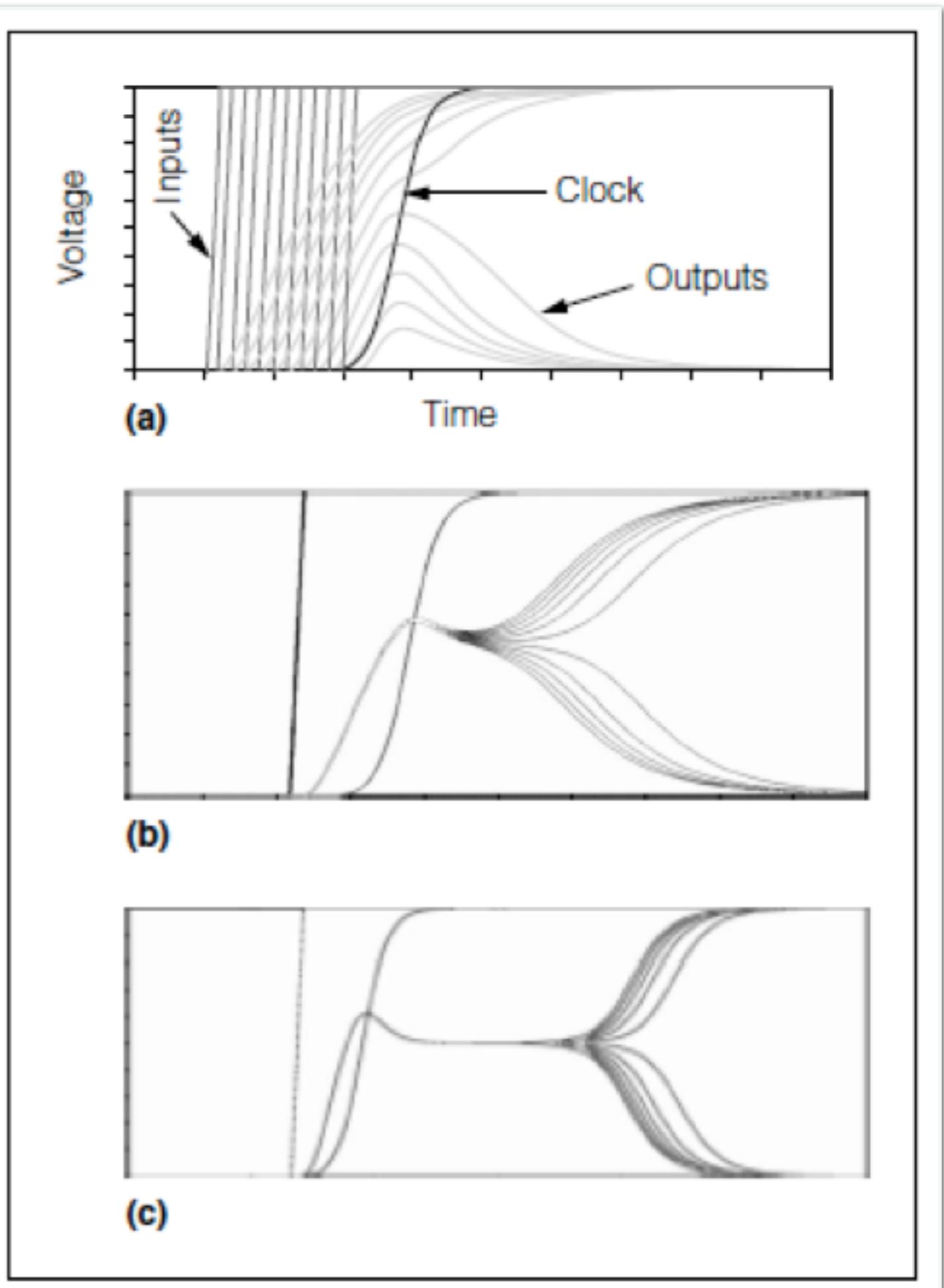
Figure 2(a)



Source: Ginosar 2011

Entering metastability

Figure 3. Empirical circuit simulations of entering metastability in the master latch of Figure 2 (a). Charts show multiple inputs D, internal clock (CLK2) and multiple corresponding outputs Q. The input edge is moved in steps of (a) 100 ps, (b) 1 ps, and (c) 0.1 fs.



Source: Ginosar 2011

Entering metastability

$$Rate = f_D T_W f_c$$

f_c = clock frequency

T_w = window of metastability

f_D = data rate at flip-flop input

Another way to express it:

$$Rate = f_D \frac{T_W}{T_c}$$

An example

- $f_c = 1 \text{ GHz}$
- $T_w = 20 \text{ ps}$
- $f_D = 100 \text{ MHz}$
- What is the rate for entering?

Exiting metastability

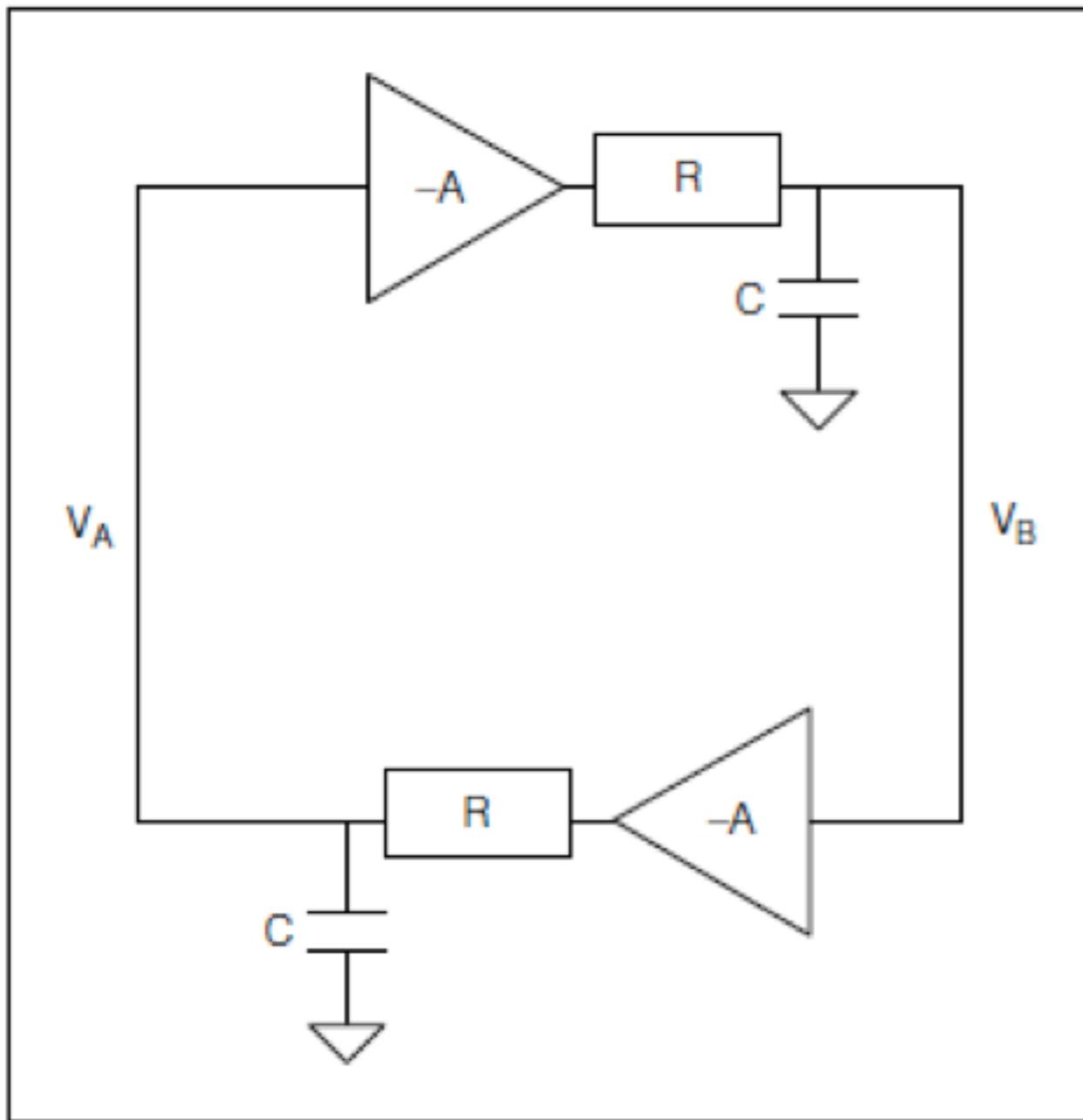
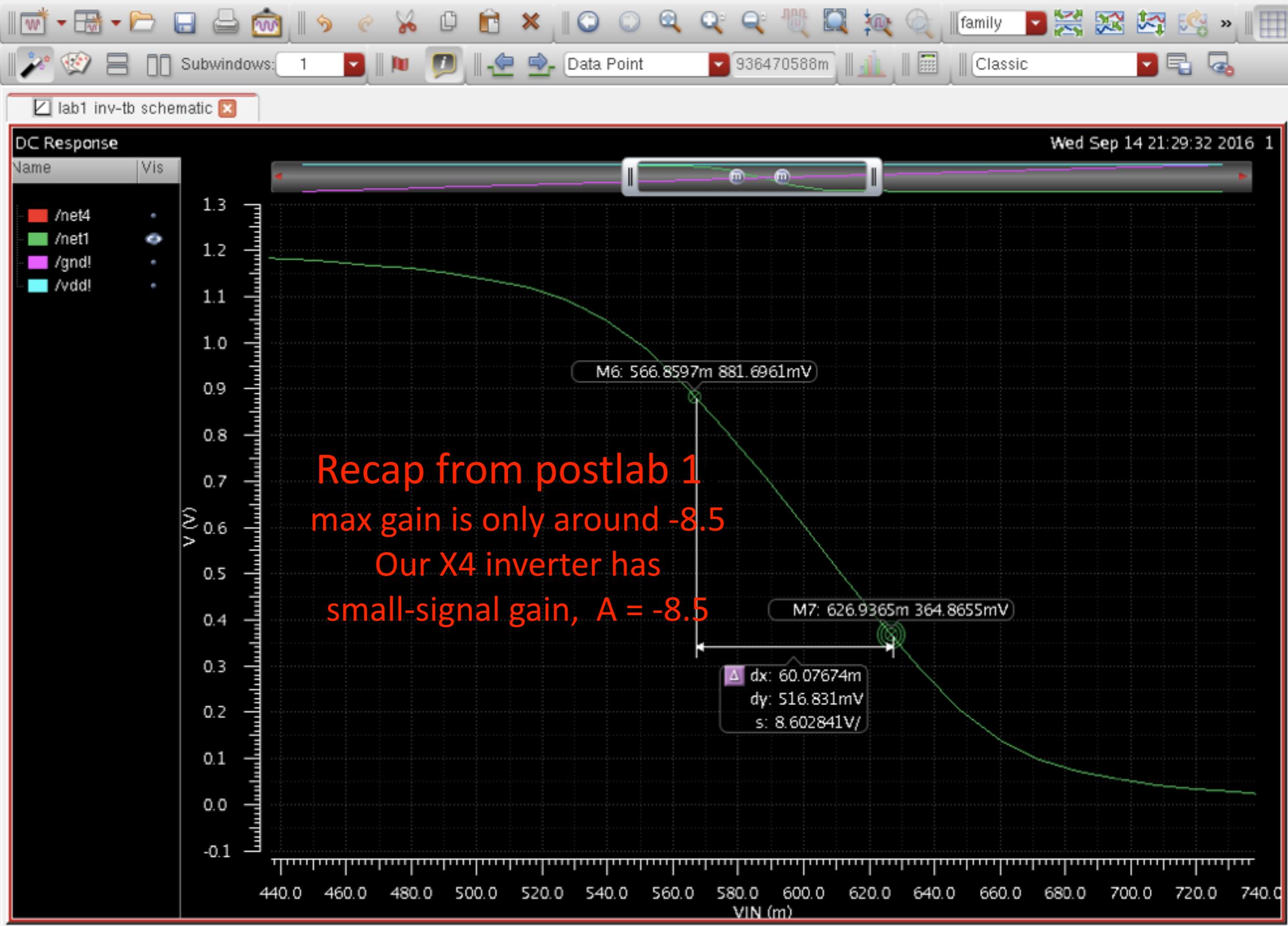


Figure 4. Analog model of a metastable latch; the inverters are modeled as negative amplifiers. Small-signal model:, $-A$ is small-signal gain, R is output resistance and C is input capacitance of other inverter.

Source: Ginosar 2011

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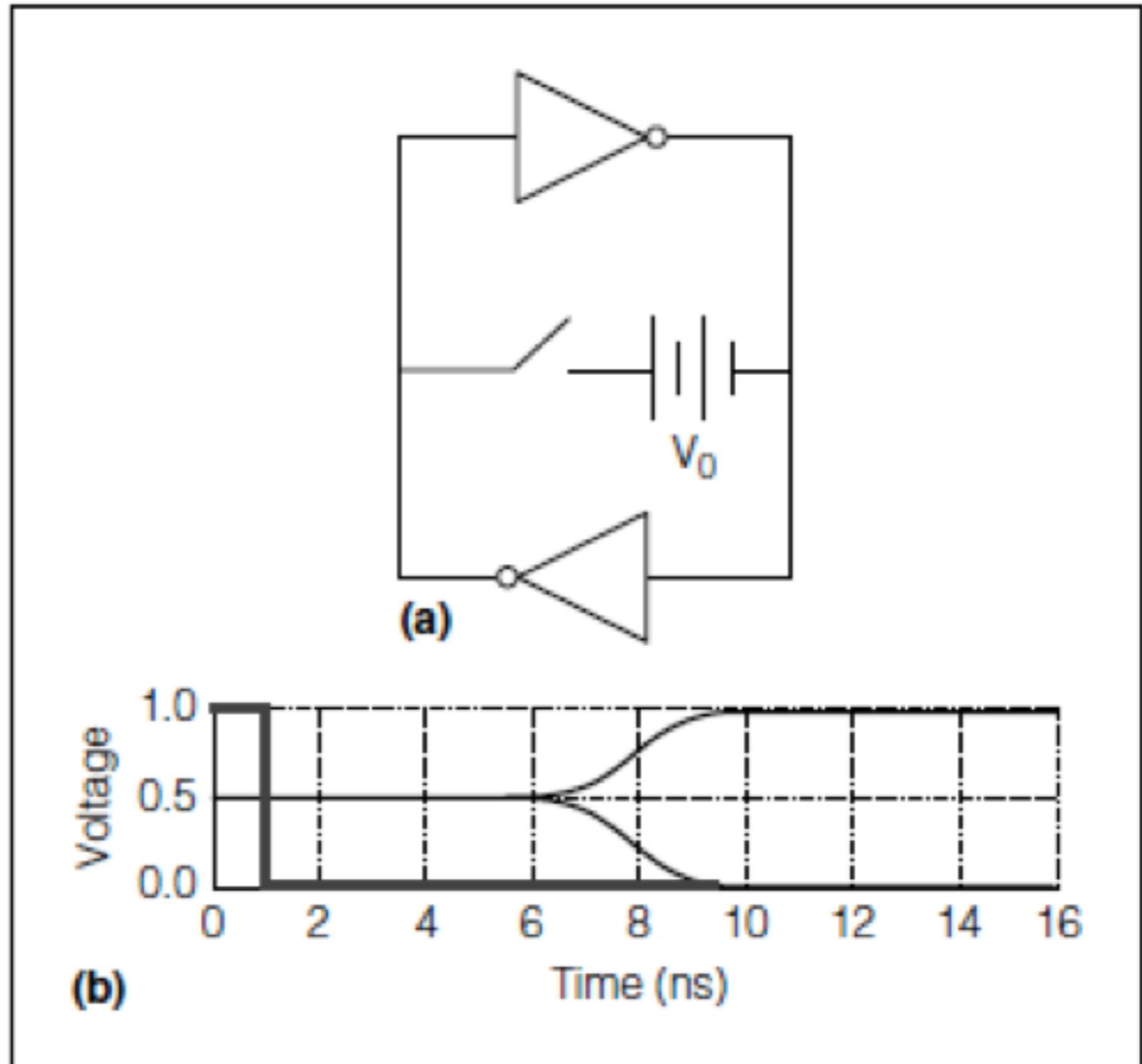
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Exiting

Figure 5. Simulation of exiting metastability: circuit (a) and voltage chart of the two latch nodes vs time (b).

The switch starts closed (applying $V_0 = 1 \mu\text{V}$) and then opens up (at $t=1 \text{ ns}$) to allow latch to resolve.



Source: Ginosar 2011

Exiting metastability

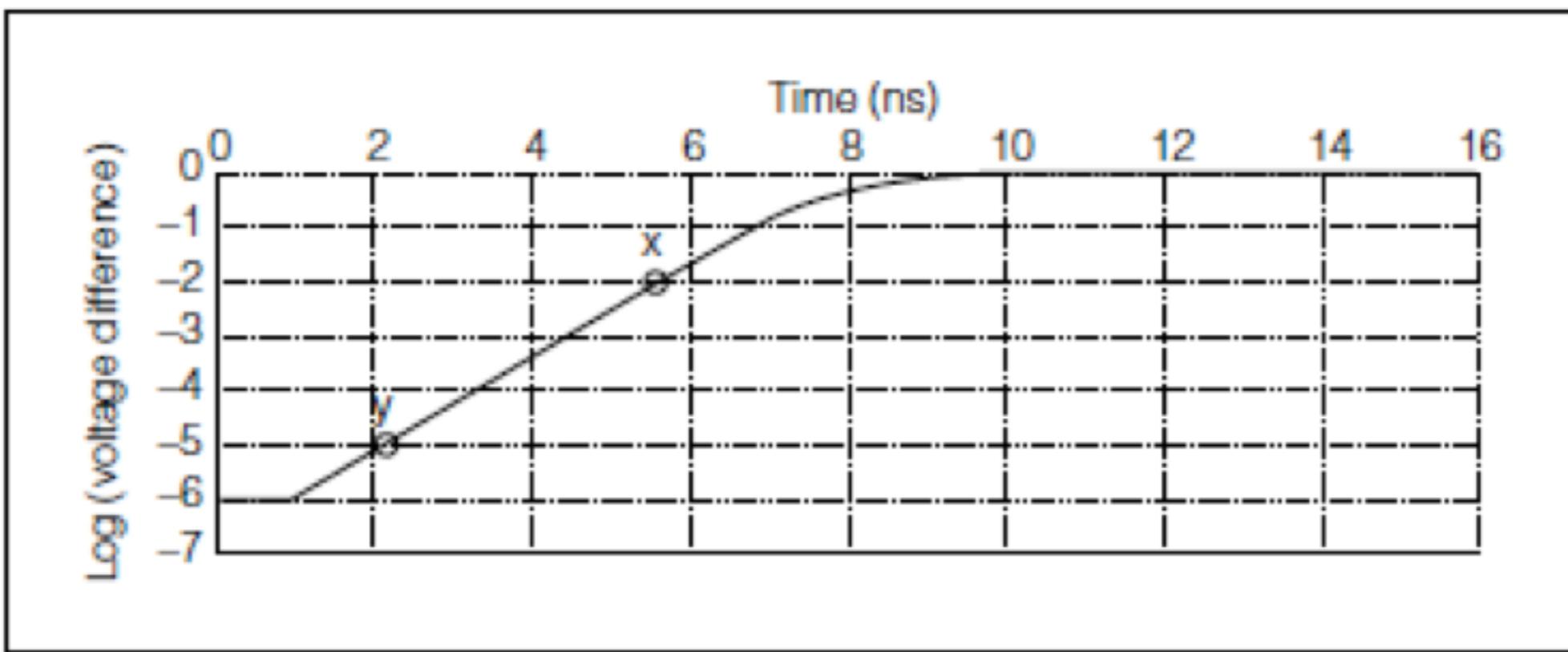


Figure 6. Log of the voltage difference of the two nodes of a resolving latch in Figure 5.

Points x and y can be used to determine time constant τ (assuming a straight line).

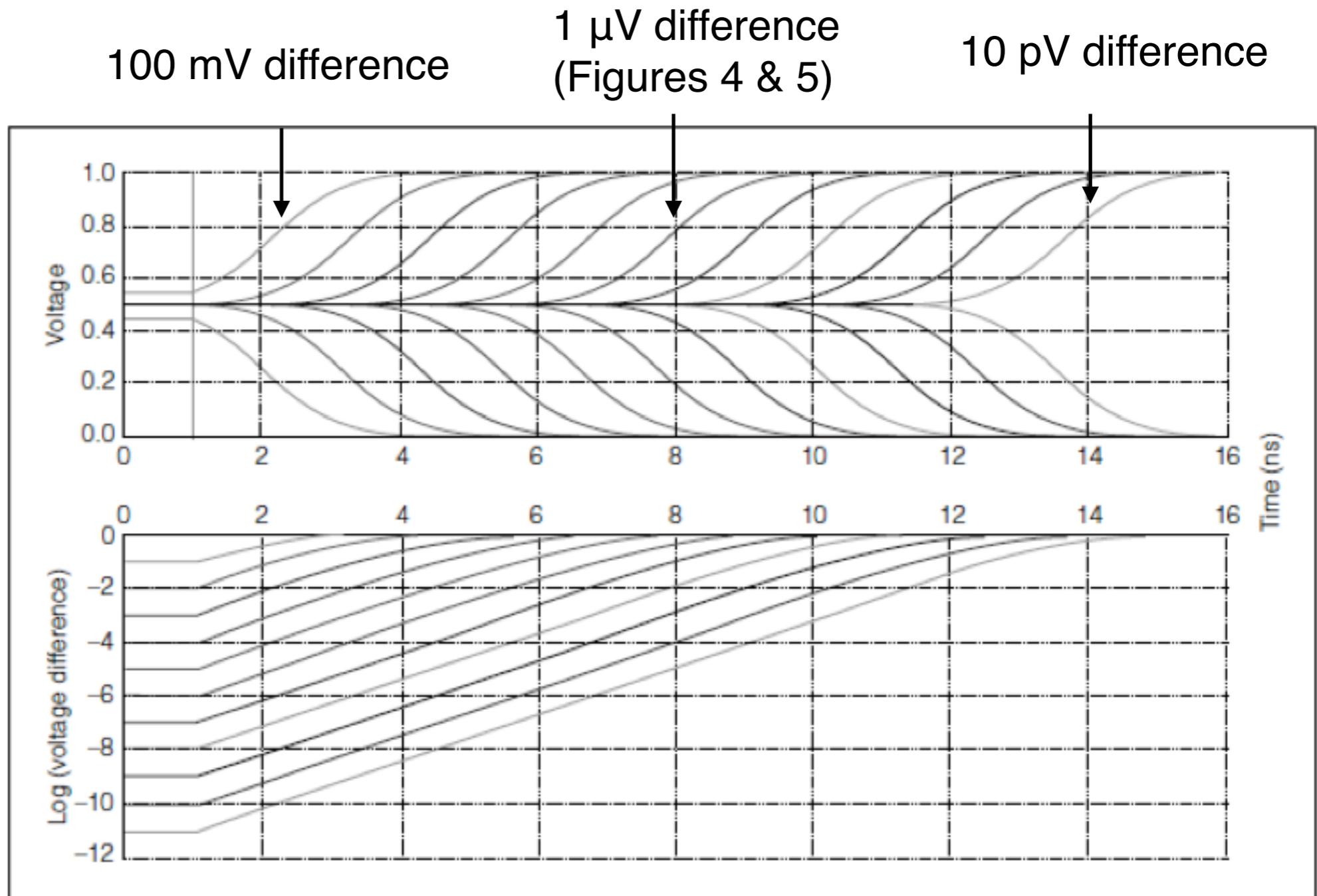
Source: Ginosar 2011

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Exiting metastability

Figure 7.
Simulations of
metastability
resolution with the
starting voltage
difference varying
from 100 mV (left)
to 10 pV (right) in
steps of factor 10;
the lower the
starting voltage
difference the
longer resolution
takes.



Time to exit

$$V_1 = V_0 e^{-\frac{t_m}{\tau}}$$

$$t_m = \tau \ln \left(\frac{V_1}{V_0} \right)$$

V_0 = starting voltage, V_1 = ending voltage,
 t_m = time to exit metastability
 τ depends on many things!
Often around 0.5 - 2 FO4 delays

Failure of synchronization

S = the allotted synchronization period

Probability of failure:

$$p(\text{failure}) = p(\text{entering}) \times p(\text{time to exit} > S)$$

$$\text{Rate}(\text{failures}) = T_W f_D f_c e^{-\frac{S}{\tau}}$$

$$MTBF = \frac{e^{\frac{S}{\tau}}}{T_W f_c f_D}$$

Avoiding synchronization failure

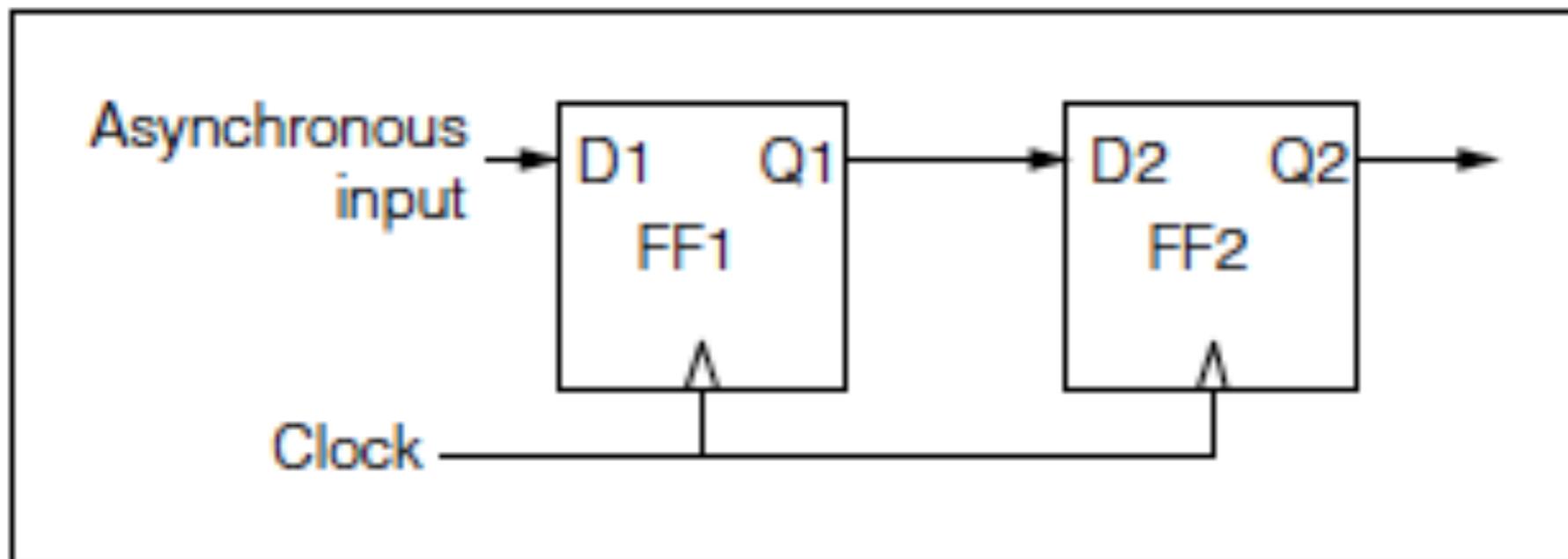


Figure 8. Two-flip-flop synchronization circuit.

6 cases

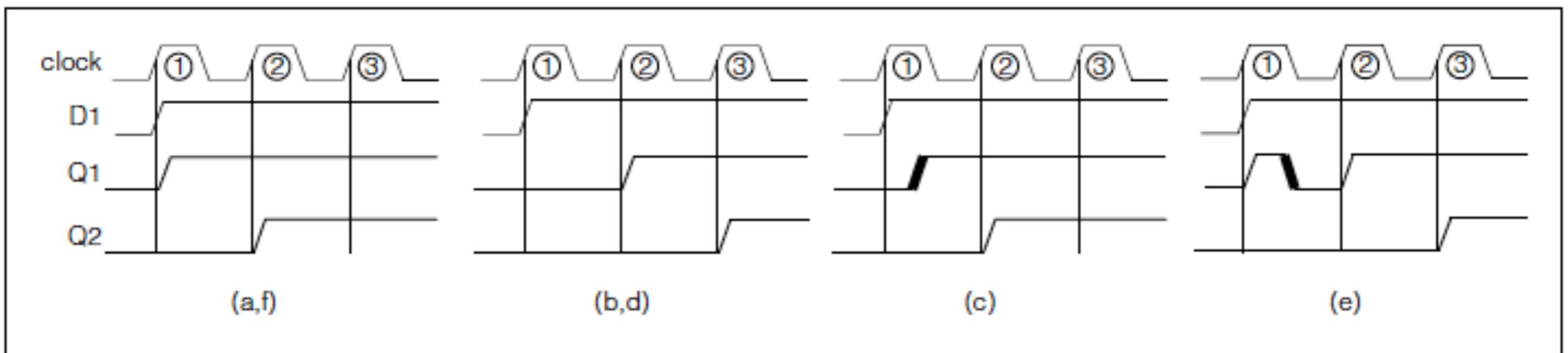


Figure 9. Alternative two-flip-flop synchronization waveforms.

Which are the 6 cases that can happen?

Many pitfalls

- Synchronizing the same signal more than once.
- Synchronizing buses
- Automated synchronizing solutions that do not work.
- For example with dynamic latches

Metastability and synchronization

MTBF is figure of merit with two parts:

Probability to enter

Probability to exit

Two FF synchronisers lower the MTBF

Many pitfalls - be paranoid!