Layout of CMOS gates

Week 4

- Monday lab2
  - Carry gate schematic
- Tuesday
  - Lecture Layout of CMOS gates
- Thursday
  - Prelab lab 3, Geometrical design rules
  - Postlab review lab 2
  - Tutorial POTW Layout (Victor)
- Friday Deadline prelab 3
  - Layout of carry ckt of full adder

From MUD cards

- Path delay optimization complicated to understand.
- Did not quite get the delay optimization example.
- More simple examples before a more complex one.
- Still confused to find out h, p.
- In $D=N \times f_{opt} + P$, why is P sum of all parasitic delay?

- Have the slides earlier before lecture? Not always possible, but the slides from last year are there.

Summary path delay optimization

Goal: minimize normalized path delay (that is, critical path delay)

Path effort $F = G \times H \times B$ (general expression for all cases)

path electrical effort: $H = C_L/C_{IN}$ (for entire path)

path branch effort: $B = b_1 \times \ldots\ldots \times b_N$ (for entire path)

path logical effort: $G = g_1 \times \ldots\ldots \times g_N$ (for entire path)

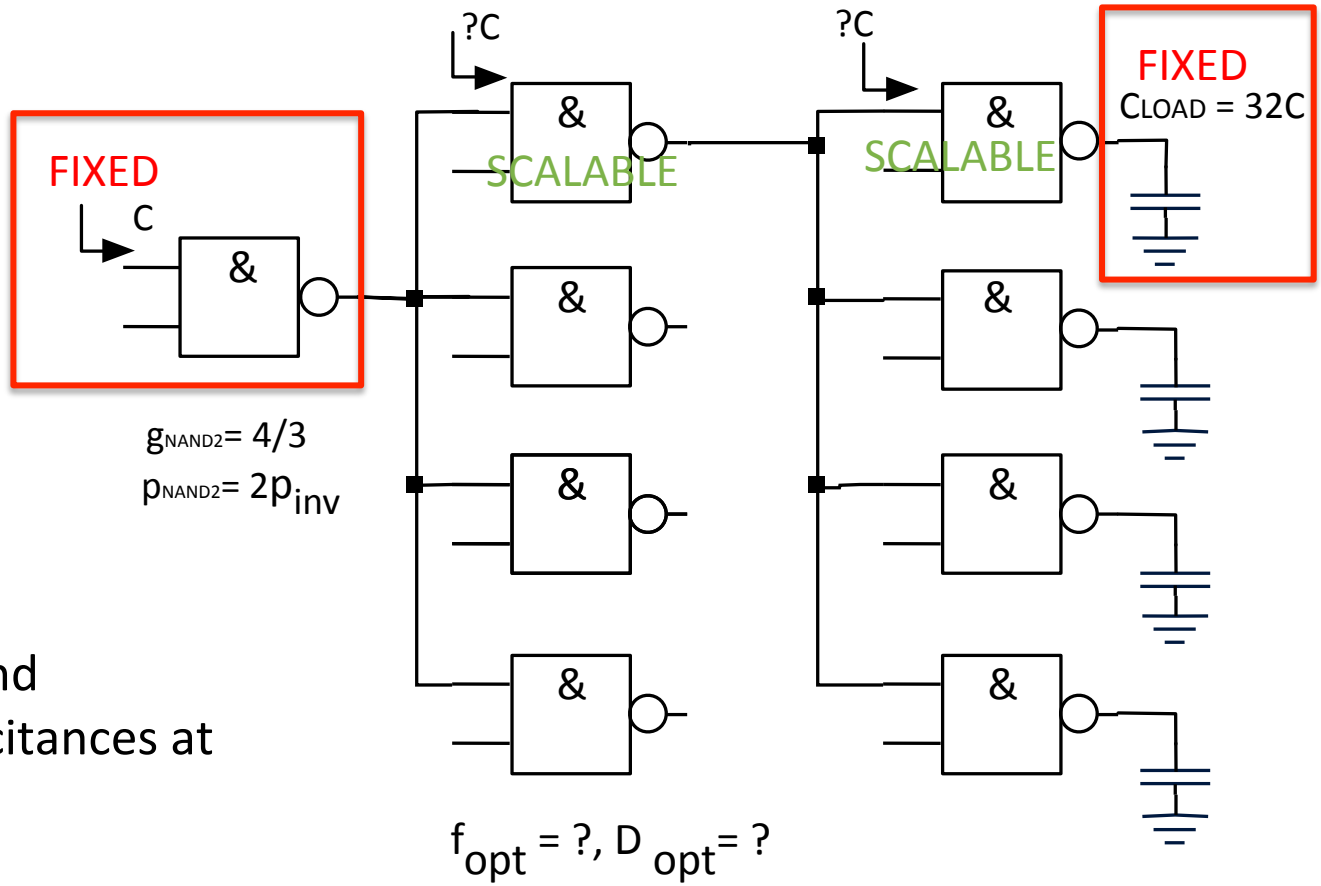
Optimal stage effort is $f_{opt} = \sqrt[N]{F}$

Optimal path delay D_{opt} is then: $D_{opt} = N \times f_{opt} + P$

where P is path parasitic delay = sum of all p in path

Read W&H section 4.5 Logical Effort of Paths

Clock tree task from latest exam



Find f_{opt}, D_{opt} and
the input capacitances at
stages 2 and 3

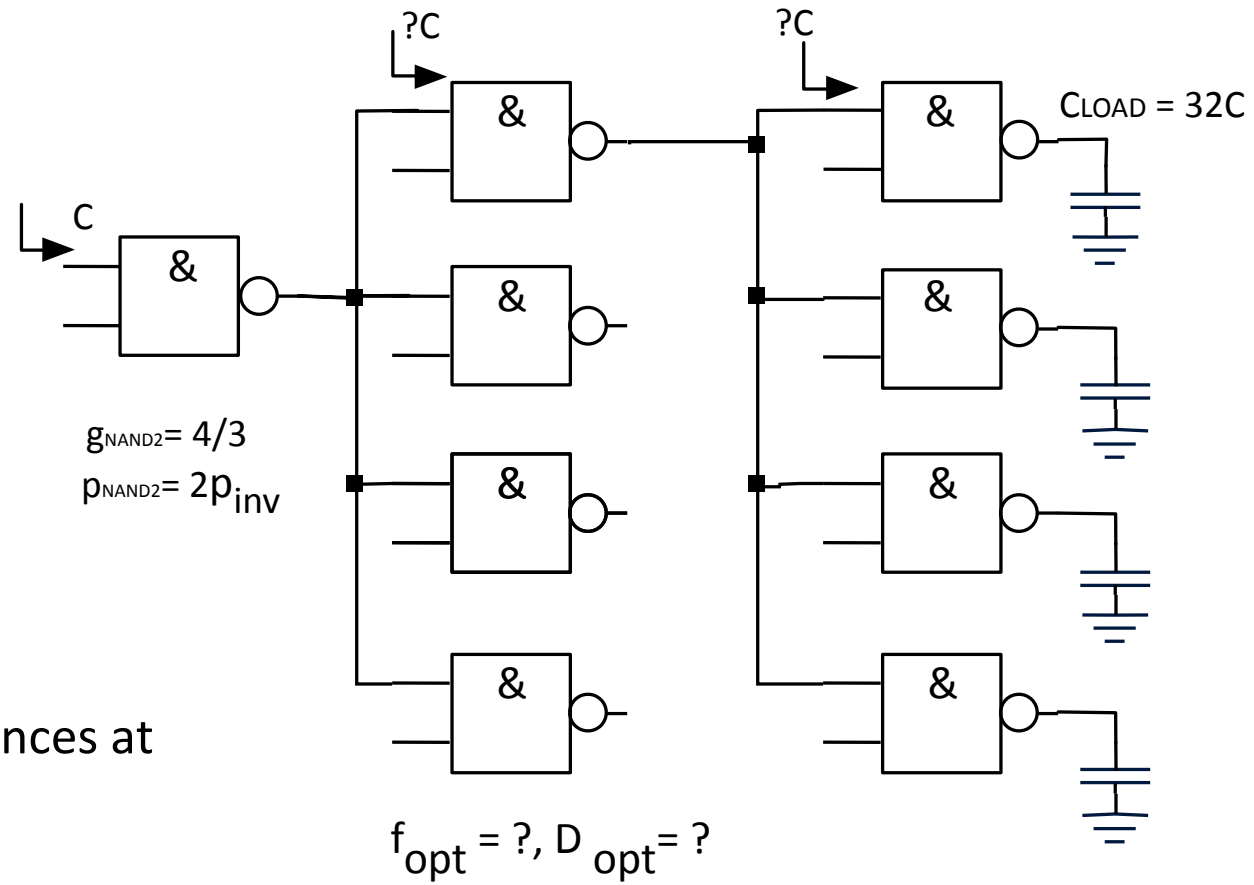
Work in small groups
Replies in socrative.com room: MCC0922018 as usual

Clock tree task from latest exam

First steps towards solution:

$F = G \times B \times H$

$F = (32/3)^3$



Find f_{opt}, D_{opt} and the input capacitances at stages 2 and 3

Work in small groups

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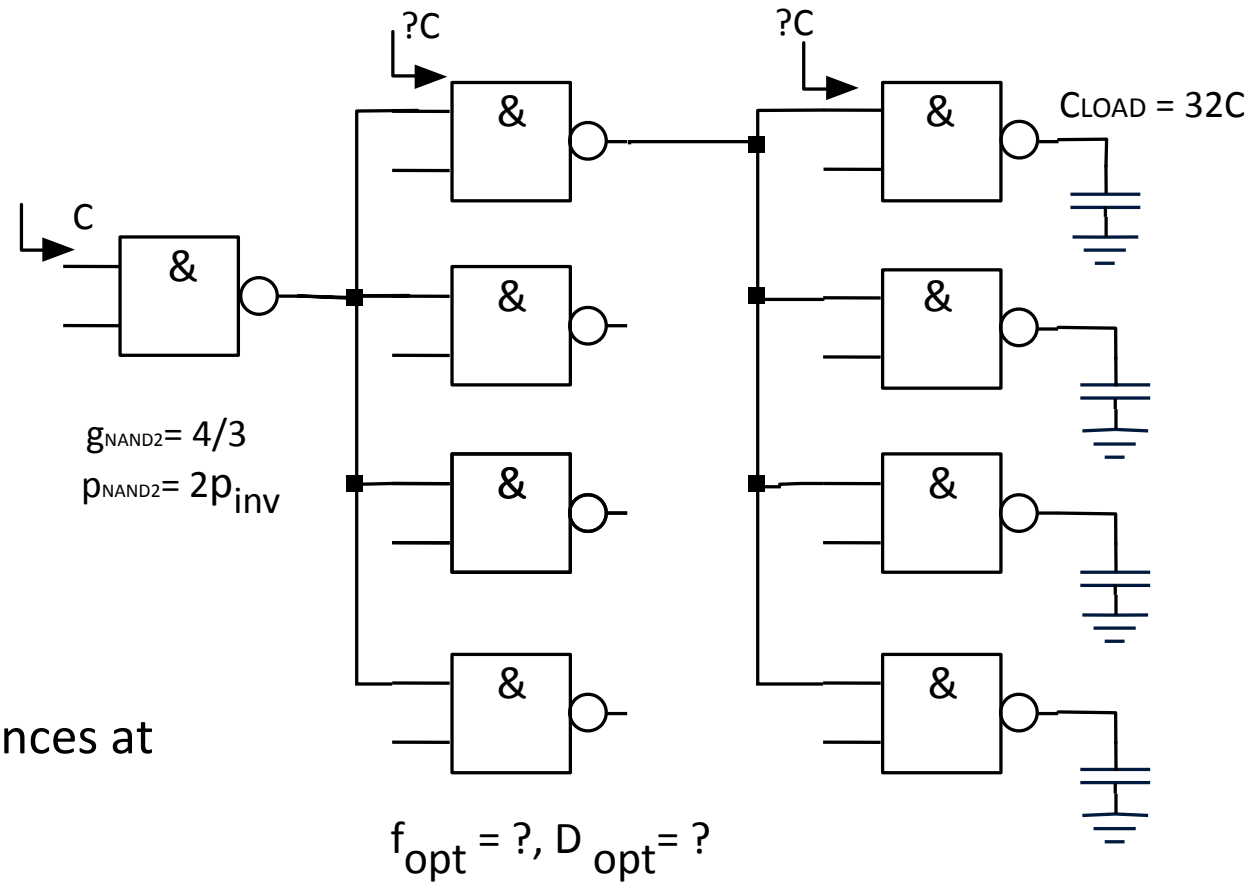
Clock tree task from latest exam

Solution:
$f_{opt} = 32/3$
$D_{opt} = 38$
(assuming $p_{inv} = 1$)



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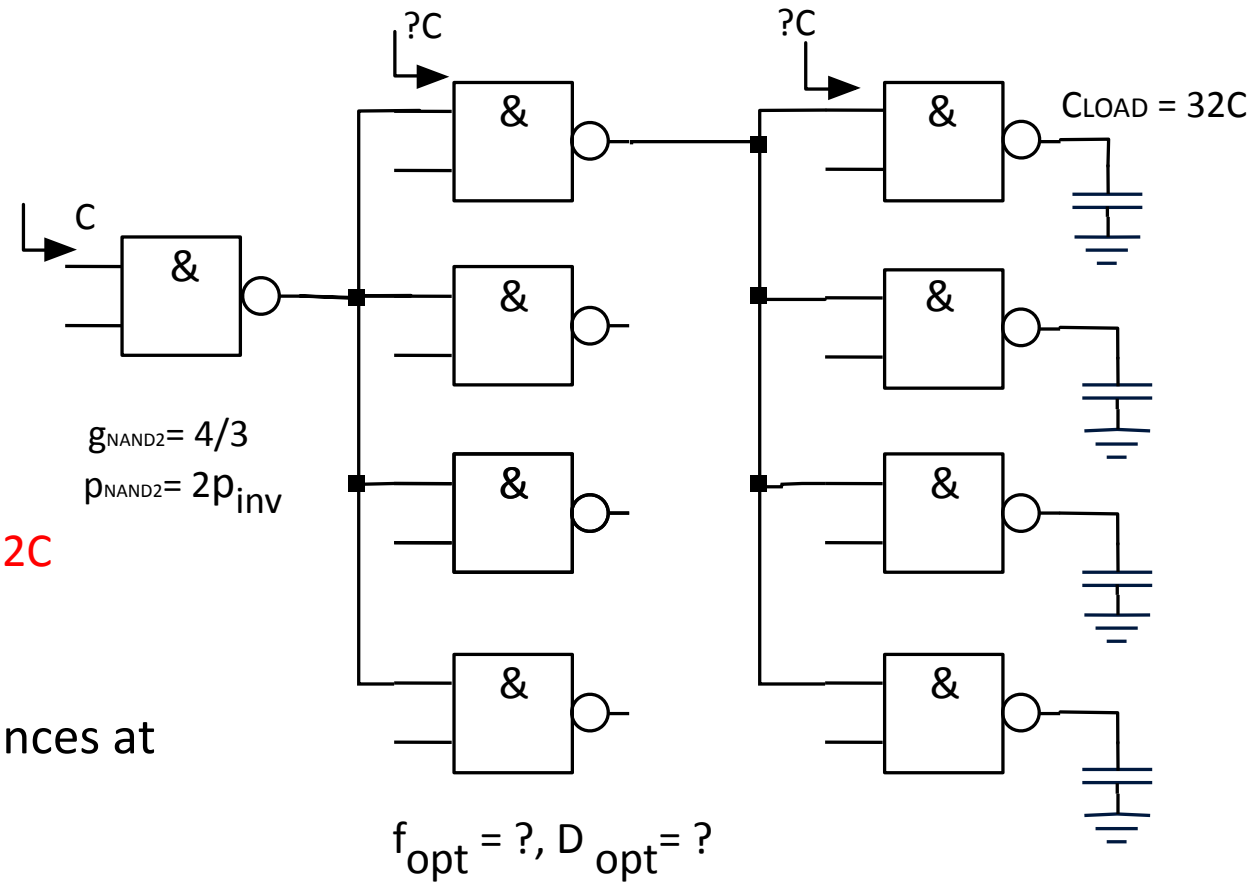
Clock tree task from latest exam

Solution:
$f_{opt} = 32/3$
$D_{opt} = 38$
(assuming $p_{inv} = 1$)

Stage 3: C_{IN} =
$(4/3) \times 32C/(32/3) = 4C$

Stage 2: C_{IN} =
$(4/3) \times (4C \times 4)/(32/3) = 2C$



Find f_{opt}, D_{opt} and
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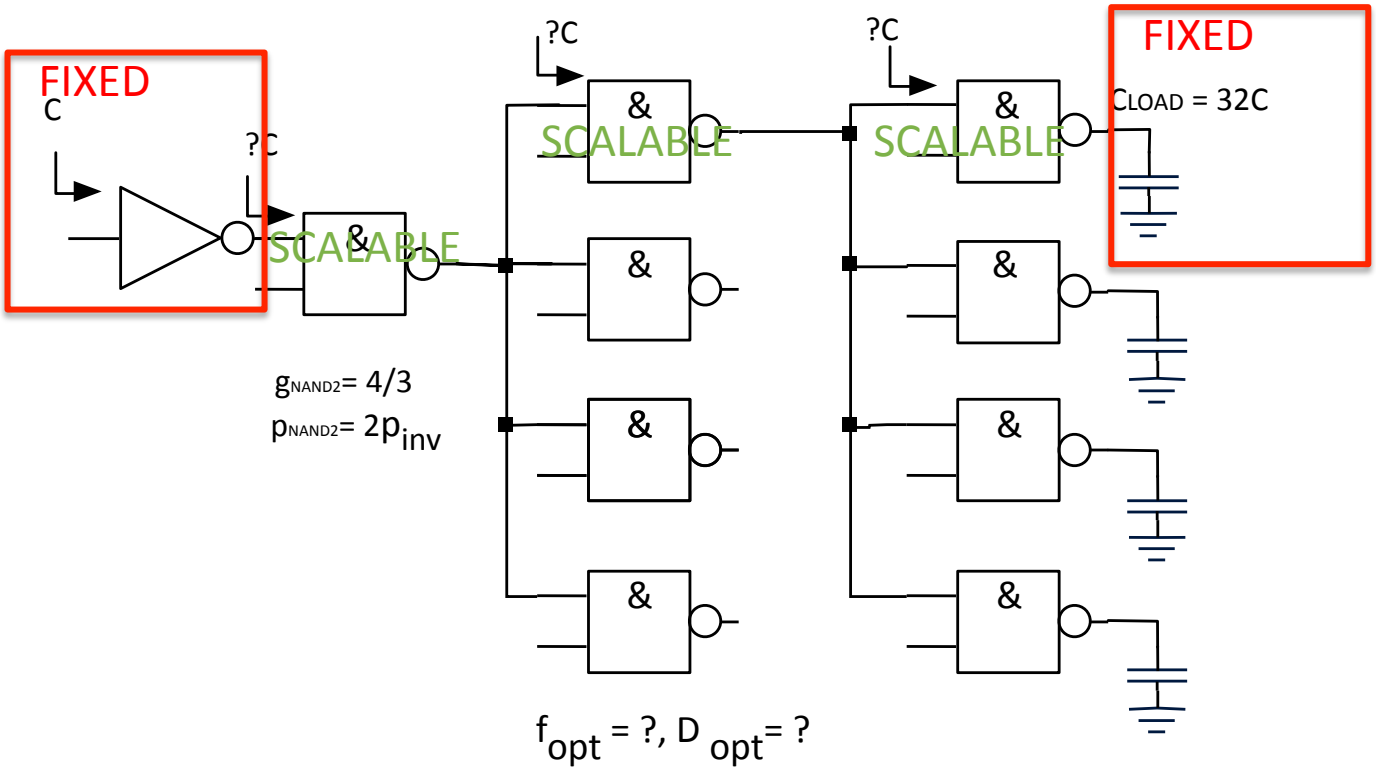
Work in small groups
Replies in socrative.com room: MCC0922018 as usual

Improve delay by adding one inverter stage – how much is path delay improved?

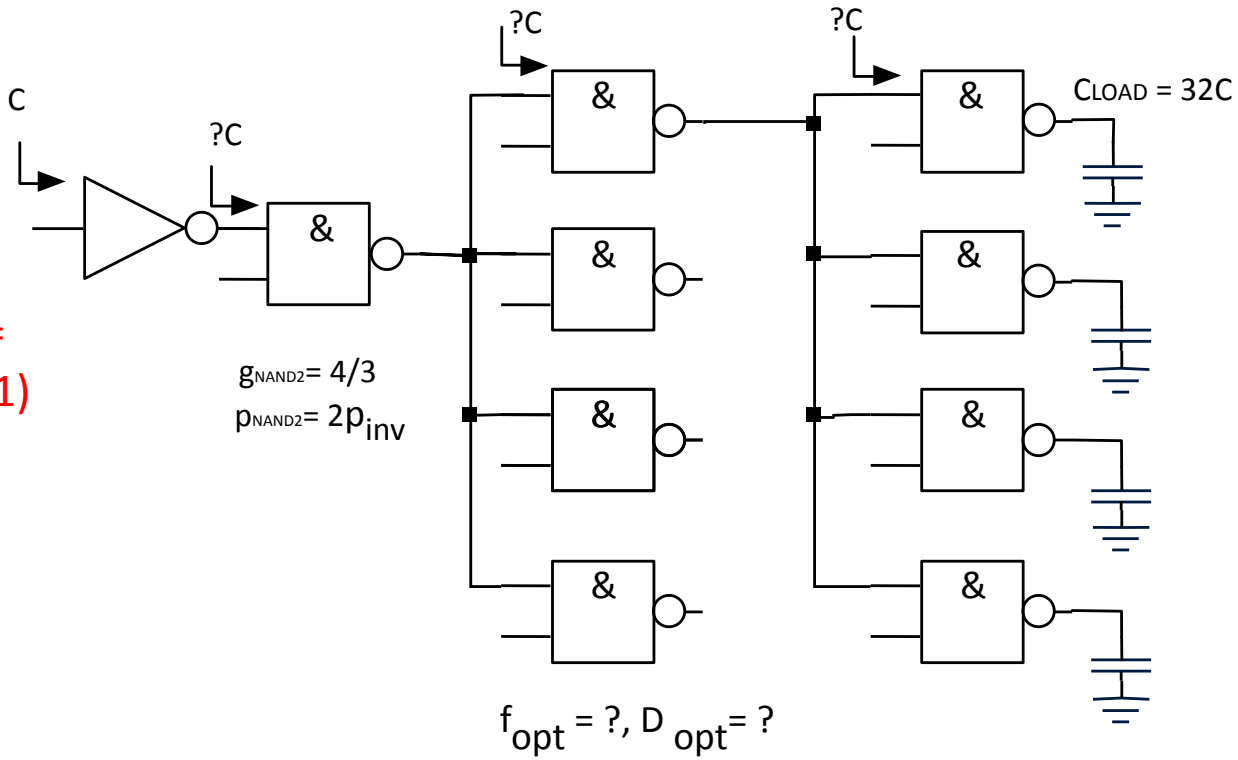


Find new
f_{opt}, D_{opt}
with added stage

Later you can calculate the sizes too
I will post those numbers

Improve delay by adding one inverter stage – how much is path delay improved?

Solution:
F =$(32/3)^3$
$f_{opt} = 4\sqrt{F} \approx 5.9$
$D_{opt} = 4 \times 5.9 + 7p_{inv} =$
30.6 (assuming $p_{inv} = 1$)



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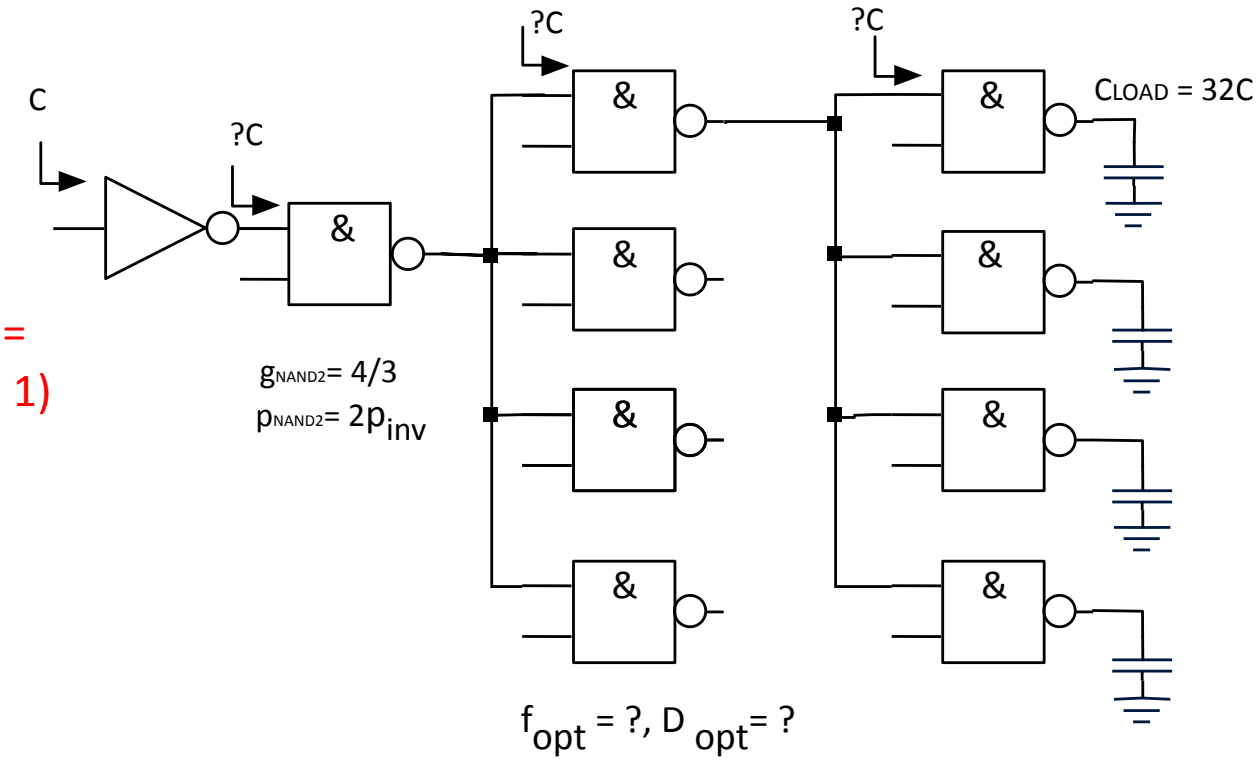
30.6 (assuming $p_{inv} = 1$)

$C_{IN2} = 5.9C$
$C_{IN3} = 6.5C$
$C_{IN4} = 7.2C$

Find new
f_{opt}, D_{opt}
with added stage



Later you can calculate the sizes too
I will post those numbers

Aim of lecture

- To give some basic understanding of layout trade-offs between wiring and transistors
- To provide guidelines for systematic and structured design using standard cell templates
- To discuss the influence of layout on performance
- To use Euler paths to minimize parasitics and letting MOSFETs share common source/drain areas
- To introduce methods for symbolic layout on virtual grids

The inverter -
- from schematic to layout

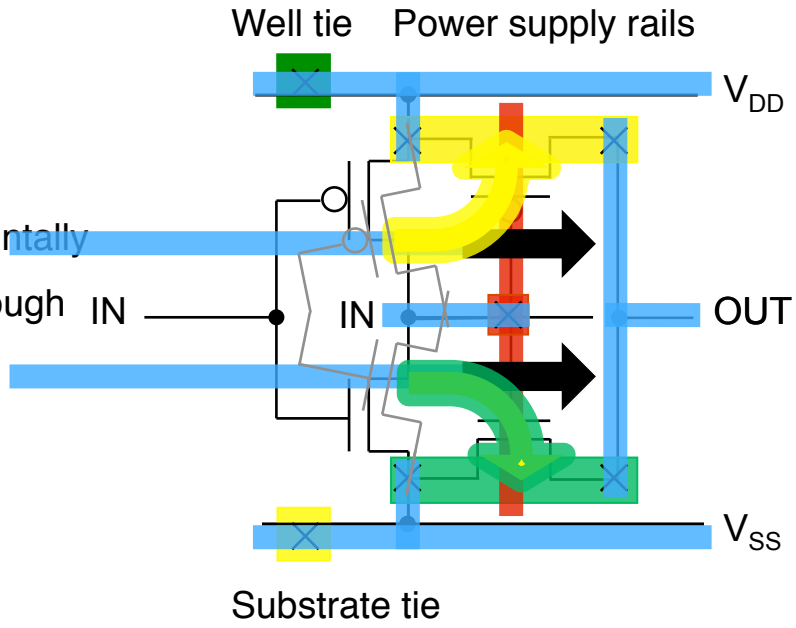
Inverter schematic

Metal wiring

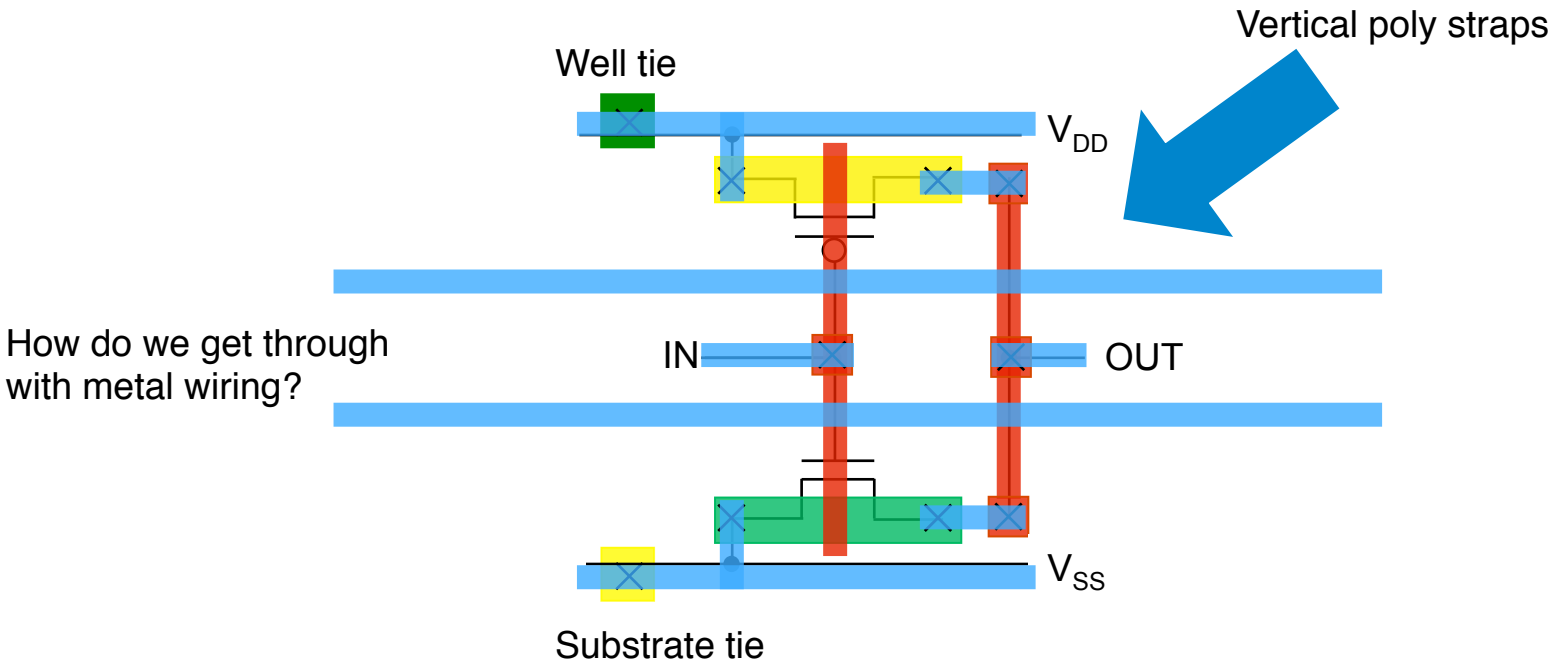
Poly only vertically

Metal mainly horizontally

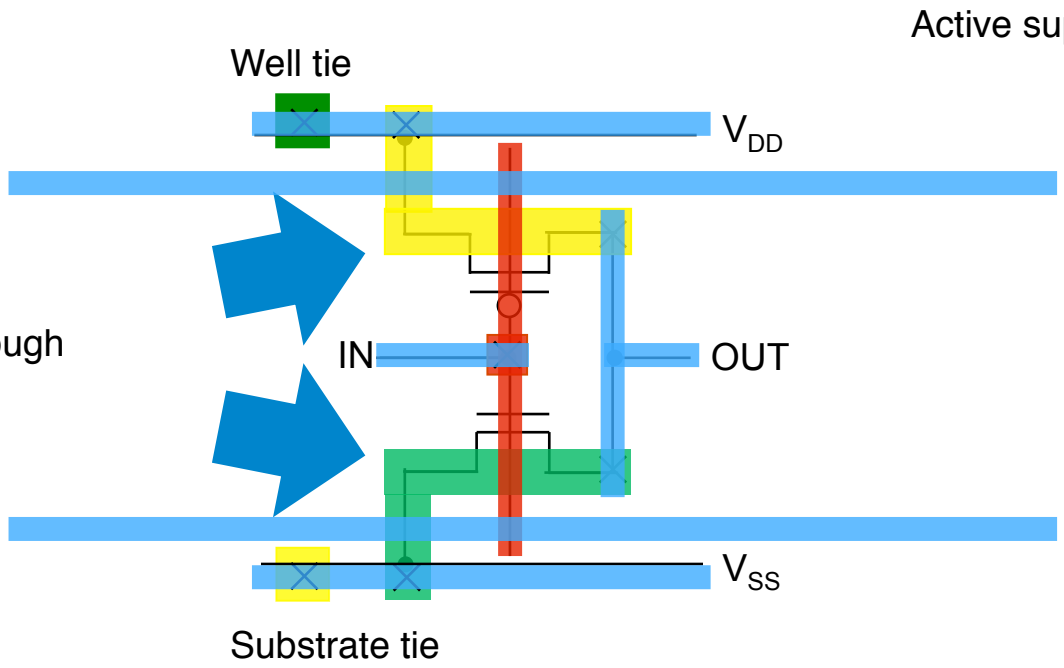
How do we get through with metal wiring?



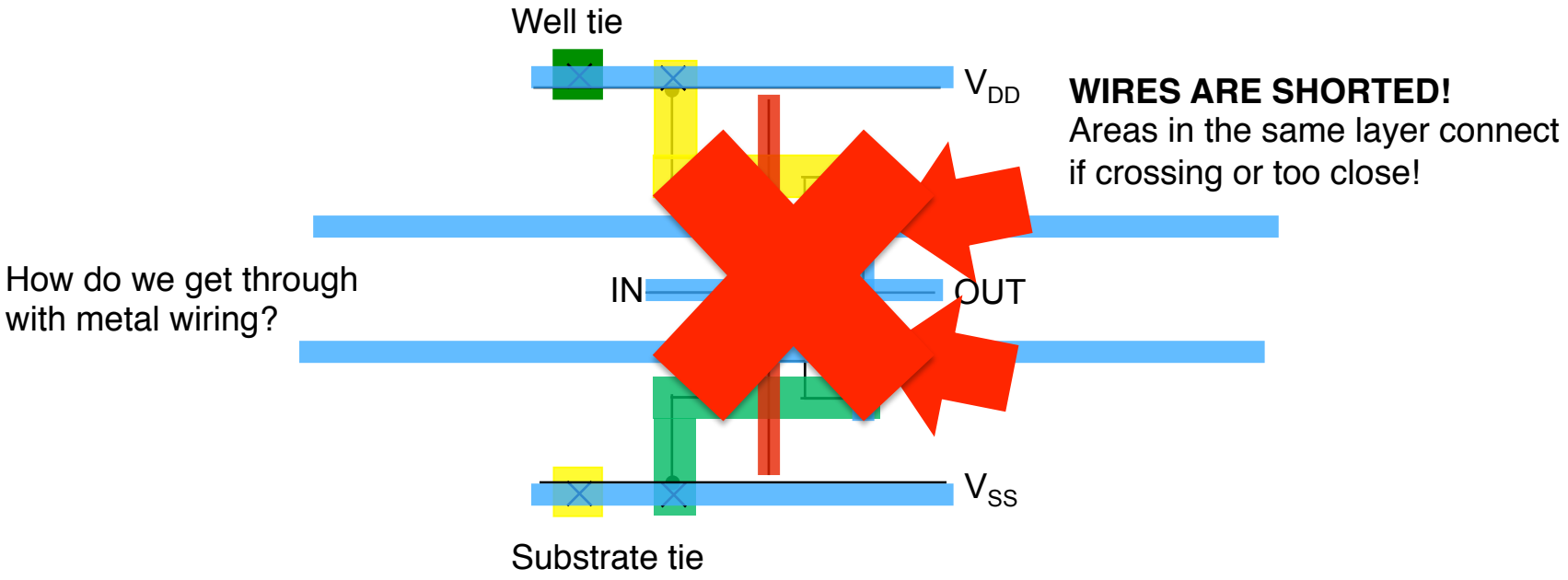
The inverter -
- from schematic to layout



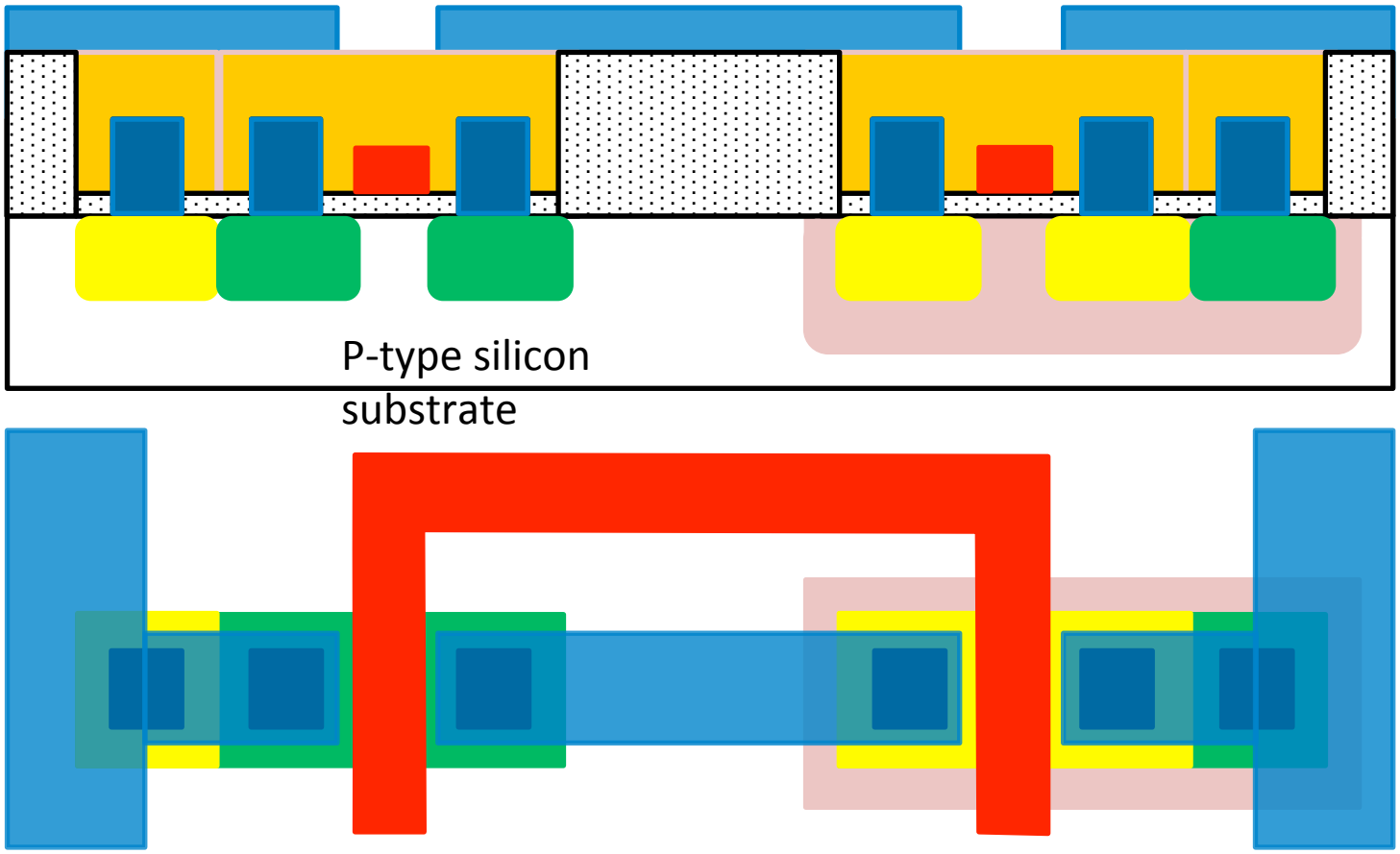
The inverter -
- from schematic to layout



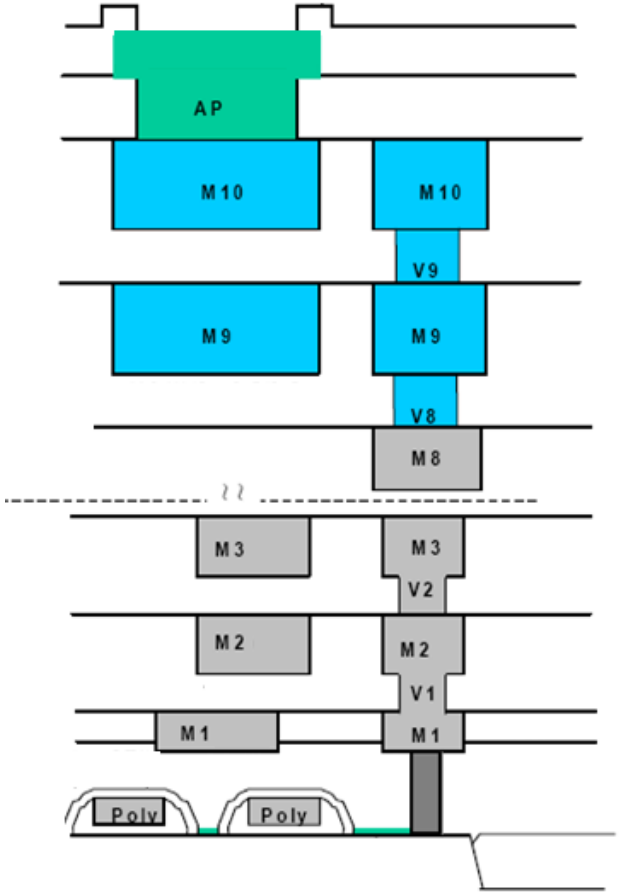
The inverter -
- from schematic to layout



Inverter mask set and fabrication



Above metal 1? A metal stack with many layers for wiring



Layers M2 and up
not used in cells.
Routed by tools.

Three types of wires:
Bottom/middle/top

Corresponds to wiring:
In cell/local/global

More about this next week!

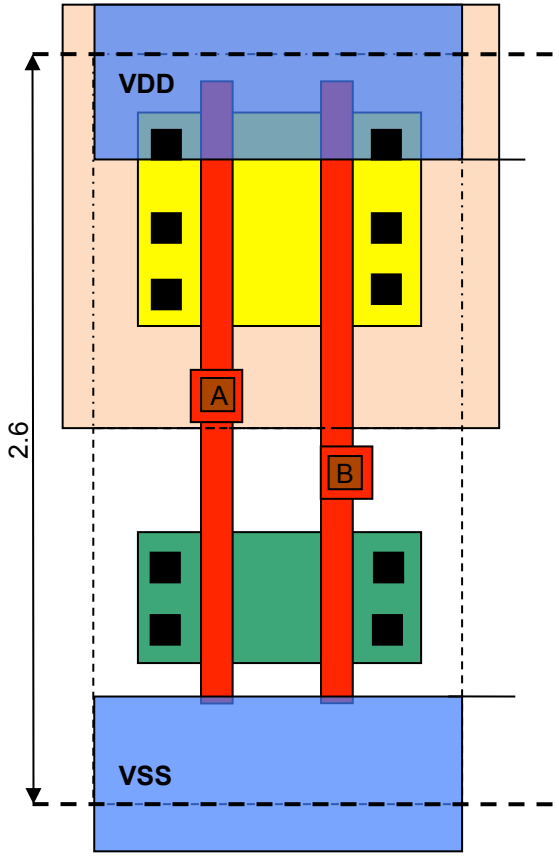
Standard cell architecture

Fixed cell height: 2.6 um

Fixed supply rails

Fixed n-well regions

Fixed contact size and positions



Standard cell architecture

Fixed cell height: 2.6 um

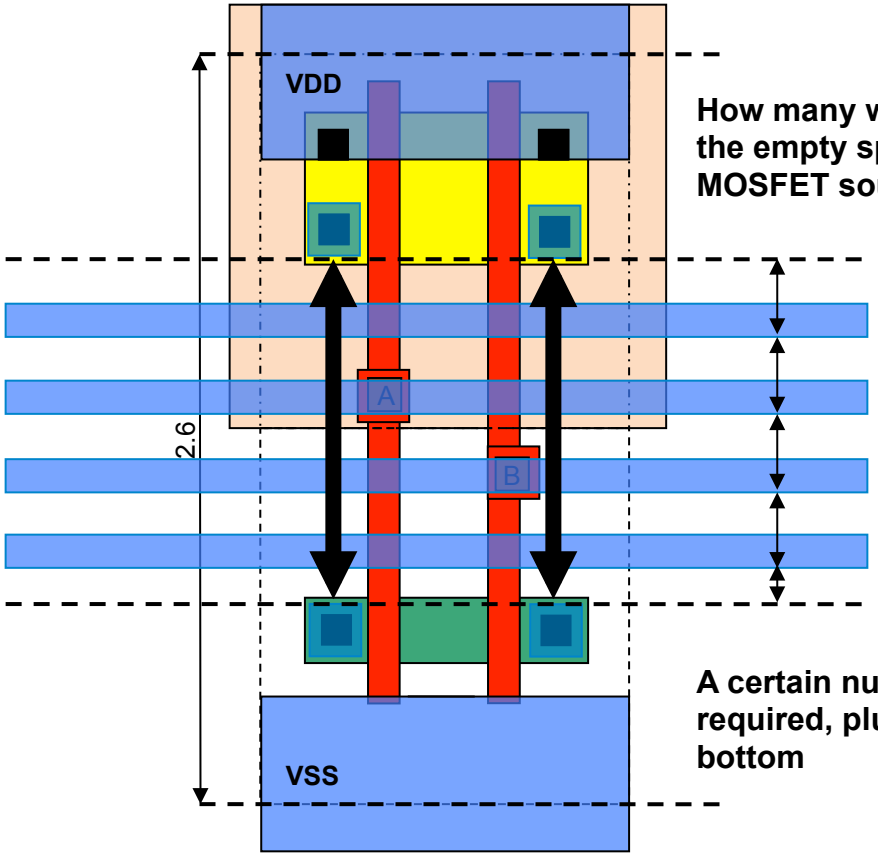
Fixed supply rails

Fixed well

Fixed contact size and positions

But MOSFET widths can be change within limits for different inverter sizes (within limits).

For even wider inverters put transistors in parallel.



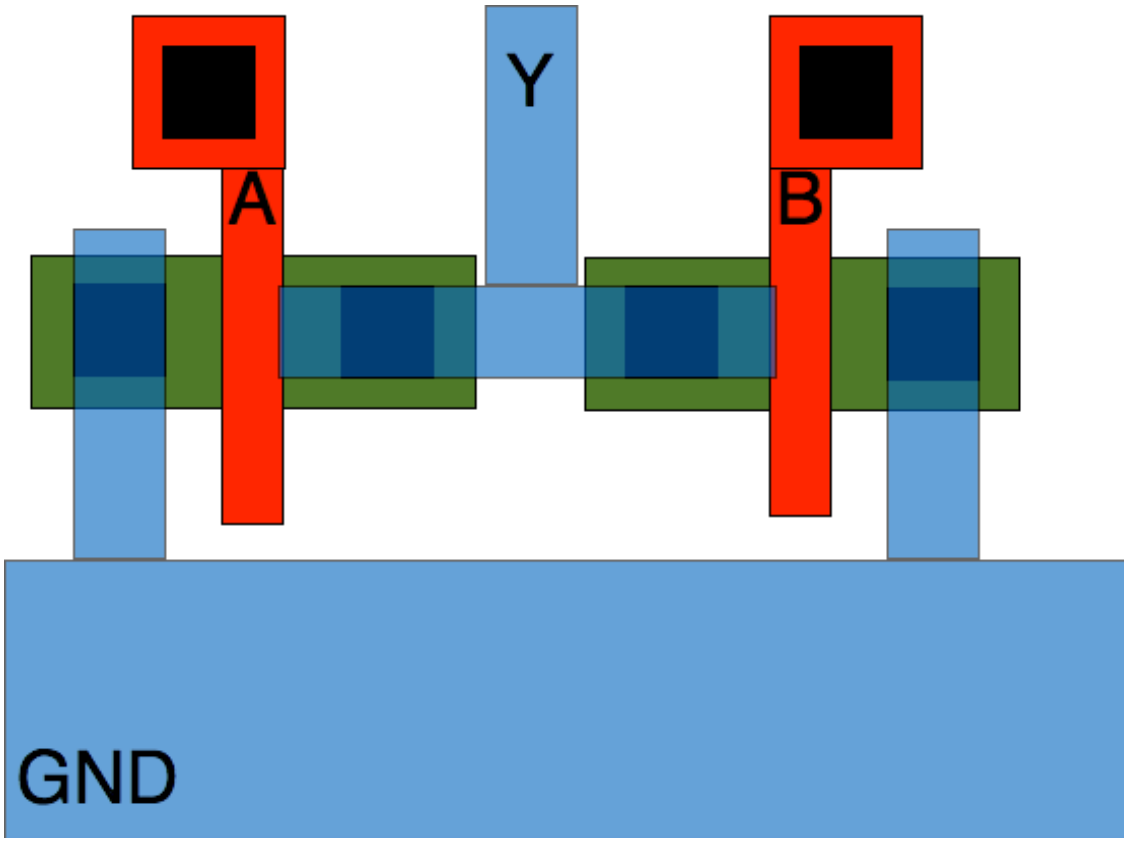
How many wire tracks can fit the empty space between the MOSFET source/drain contacts?

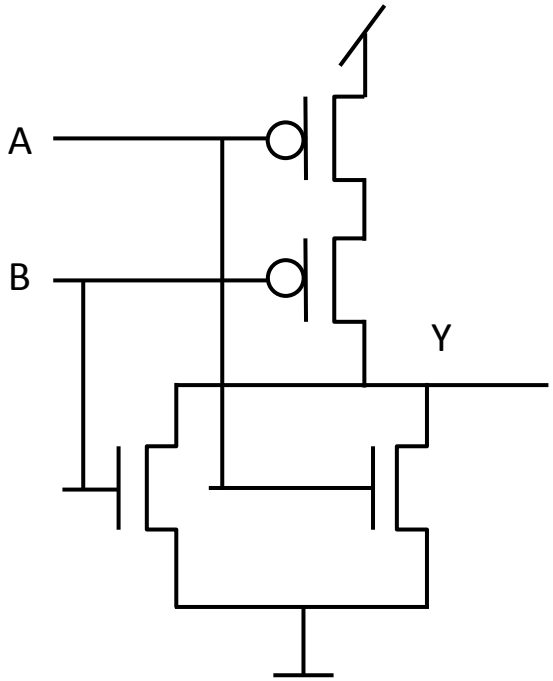
A certain number of pitches are required, plus one extra space at bottom

Stick Diagrams

- *Stick diagrams* help plan layout quickly
  - Need not be to scale
  - Draw with color pencils or dry-erase markers

Merging drain areas example NOR2 n-net





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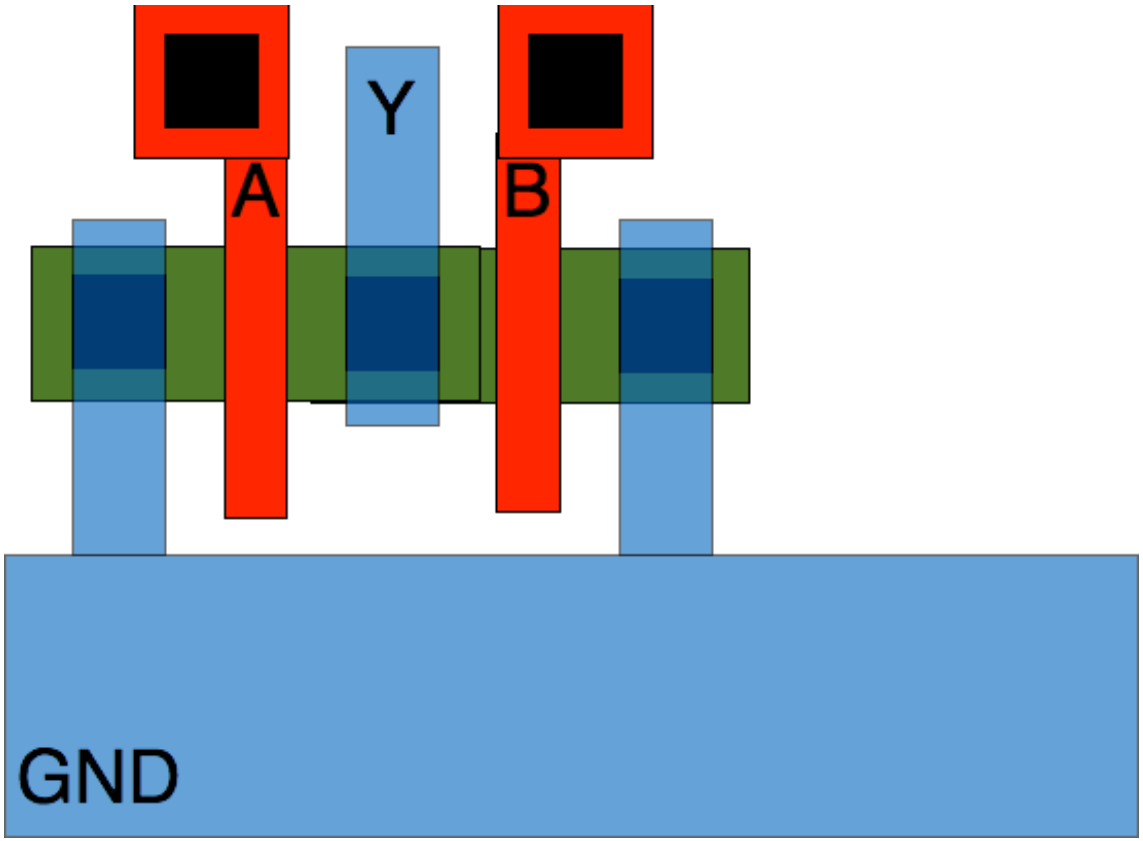
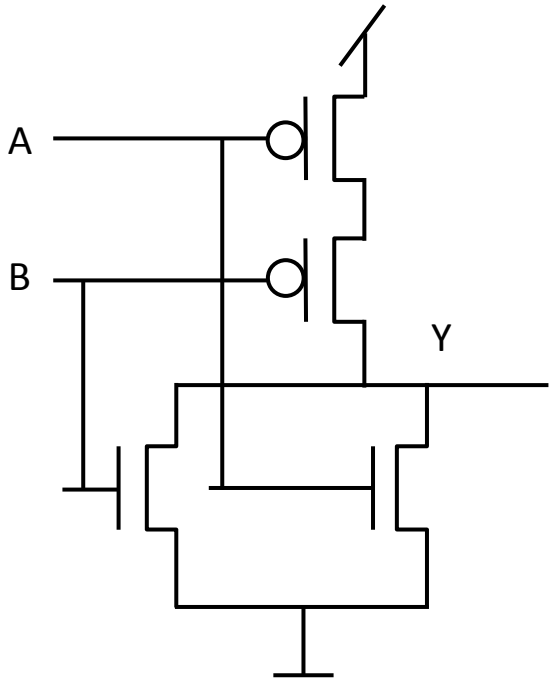
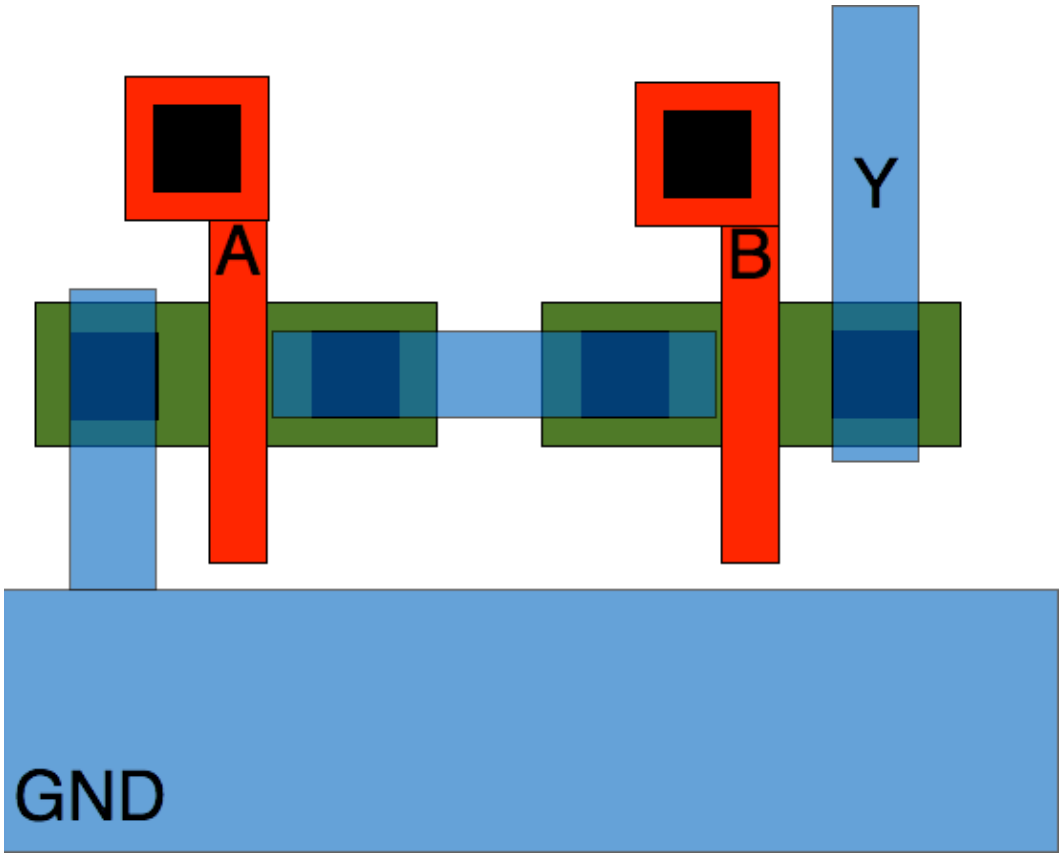
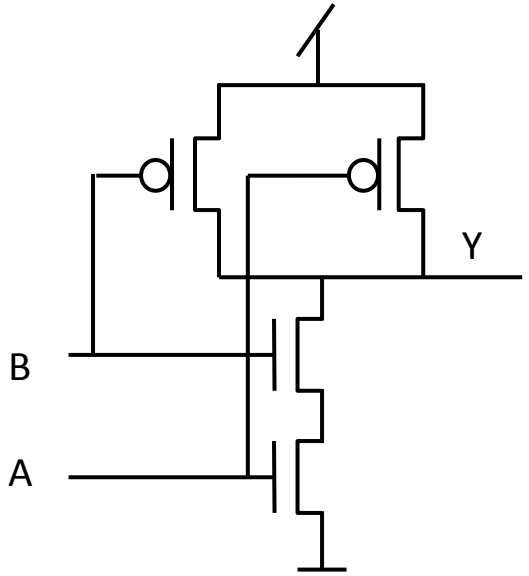




Merging drain areas example NAND2 n-net





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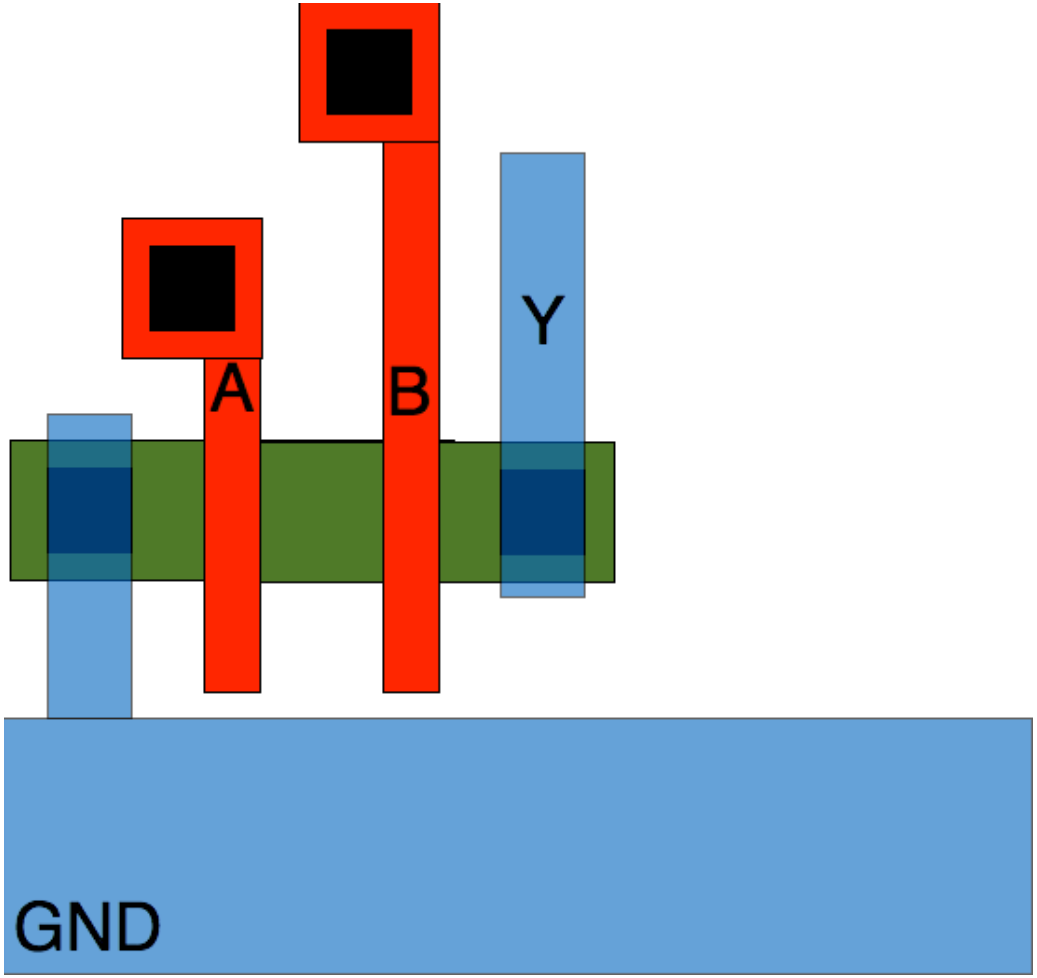
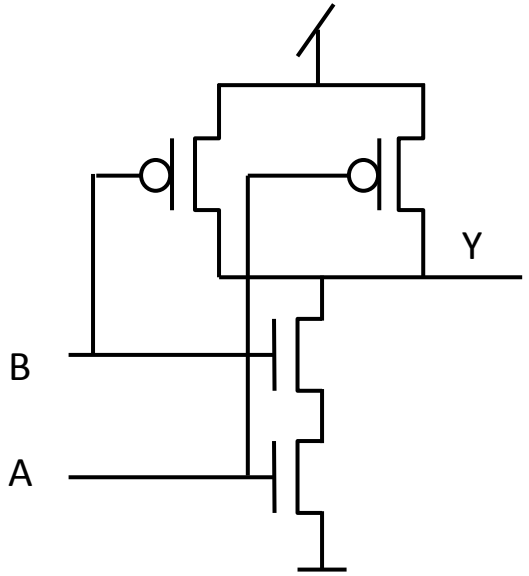
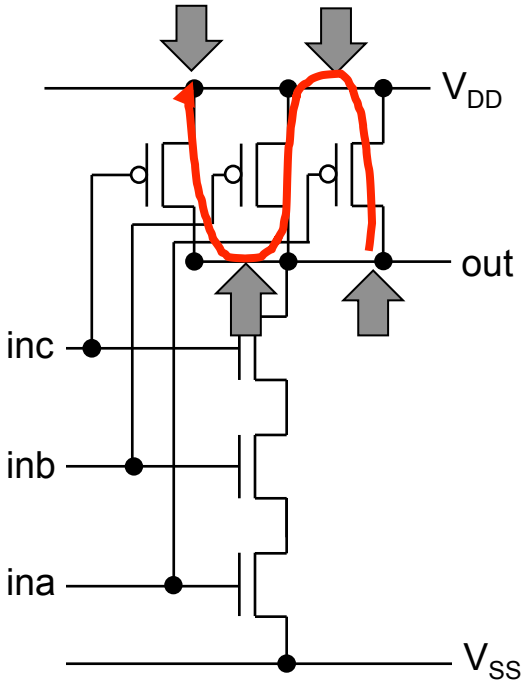
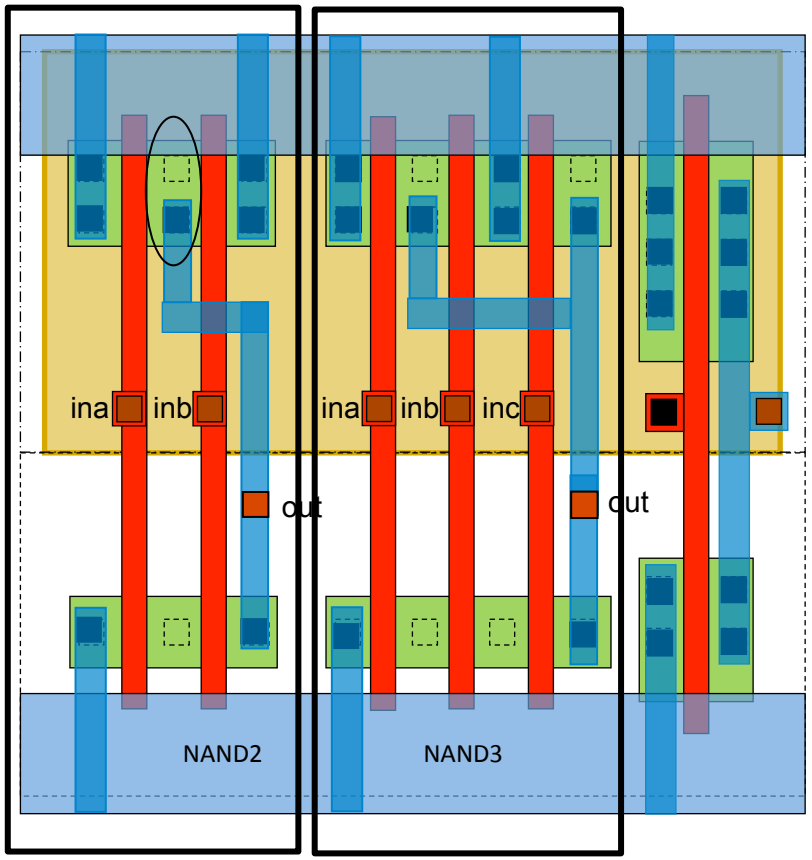


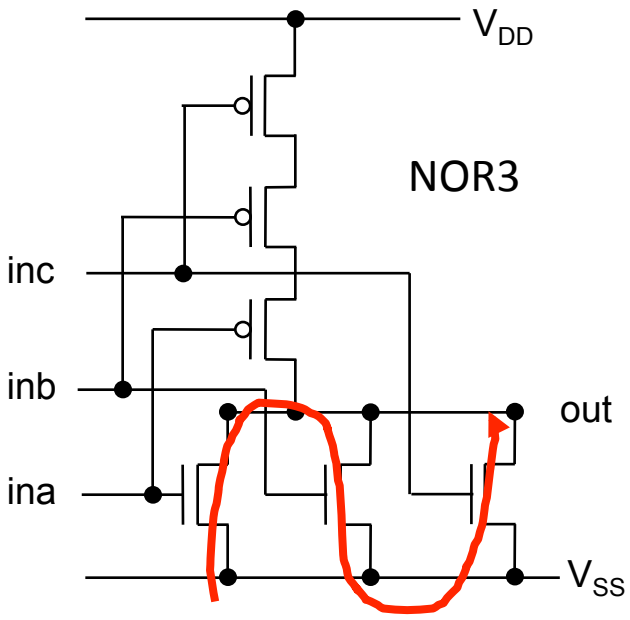


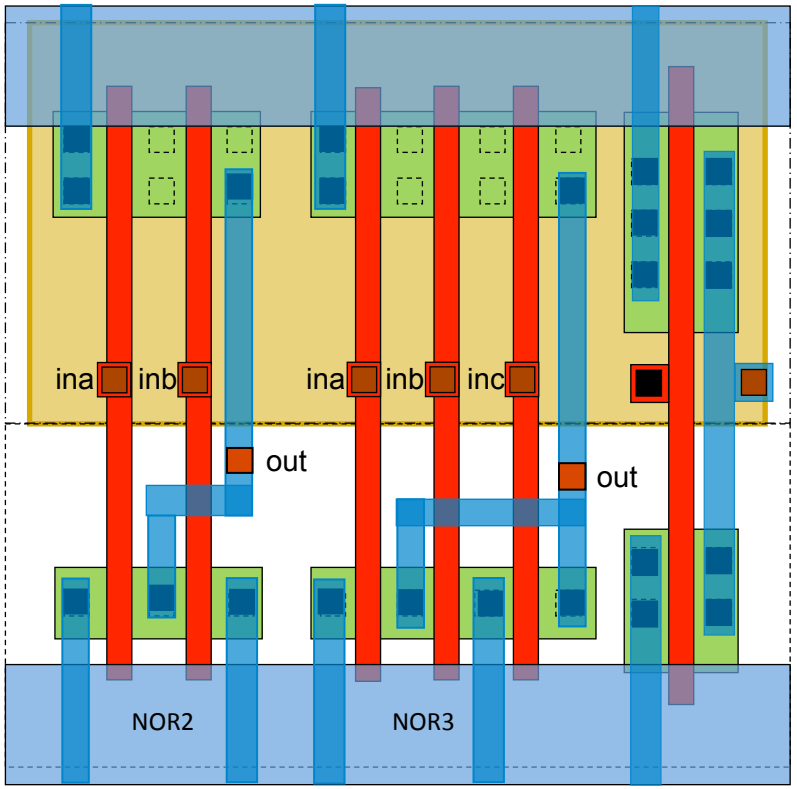
The NAND3 gate



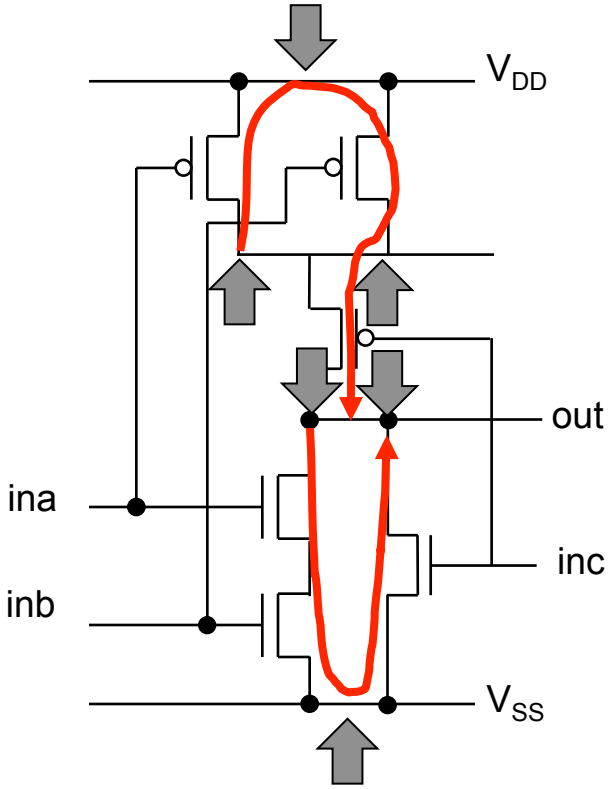


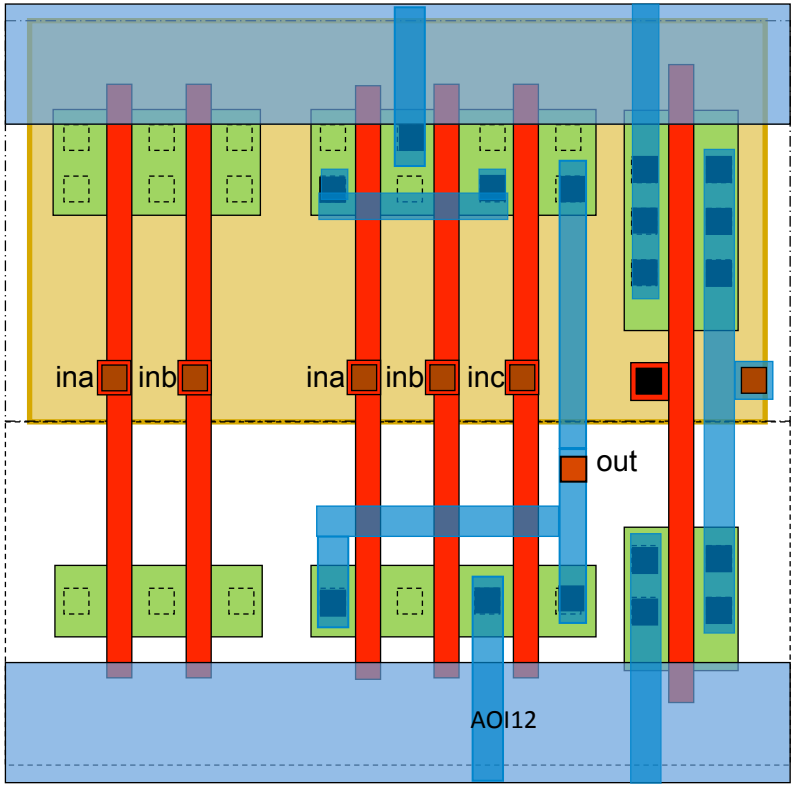
The NOR3 gate



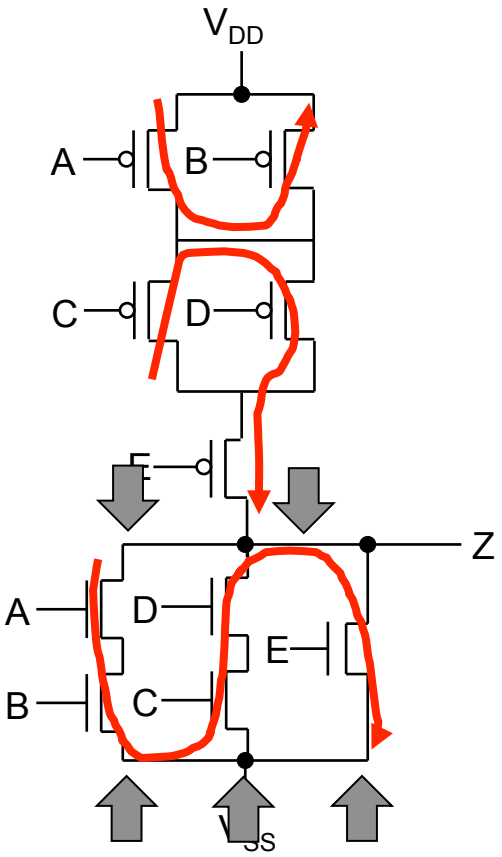


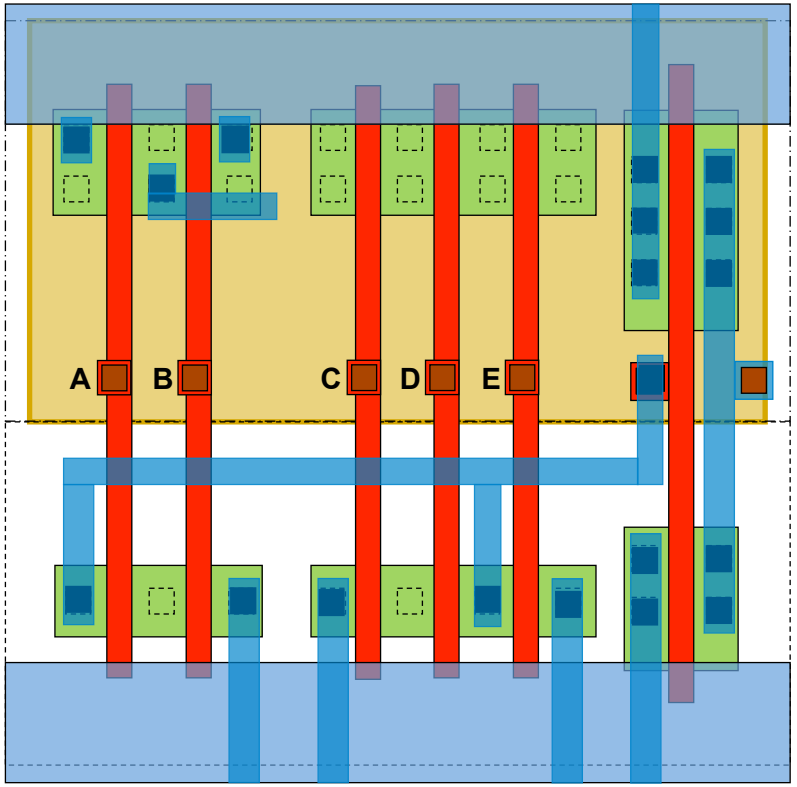
The AOI12 gate



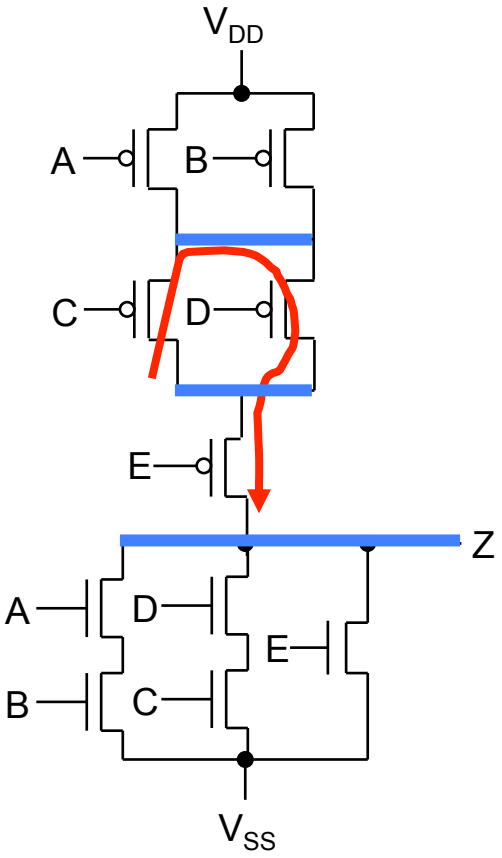


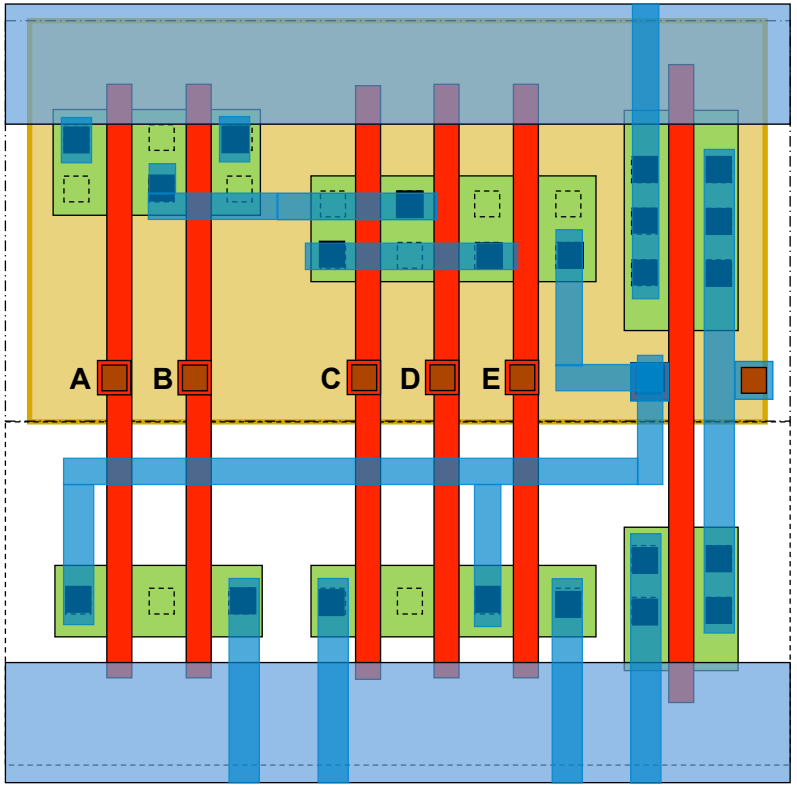
The AO212 gate





The AO212 gate

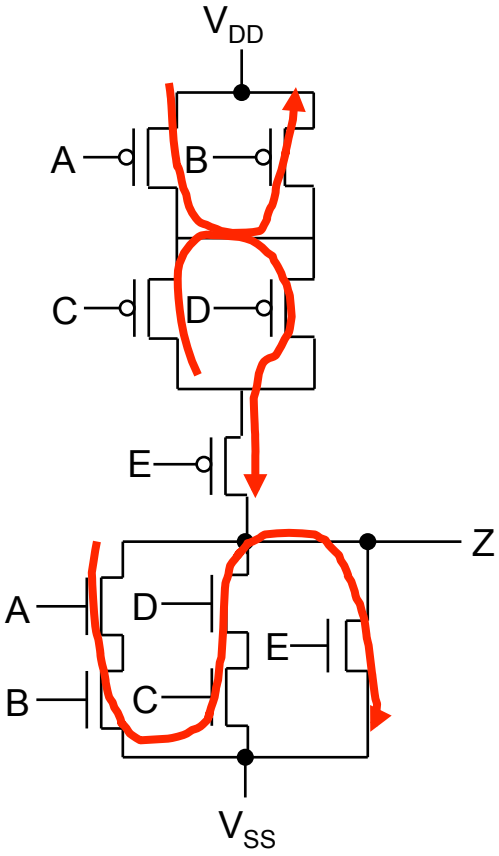


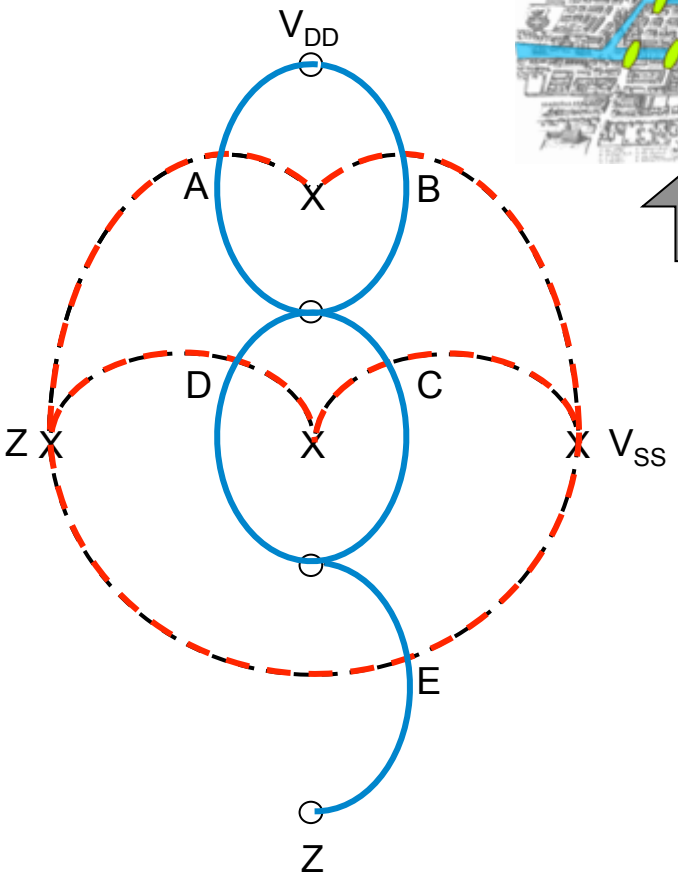


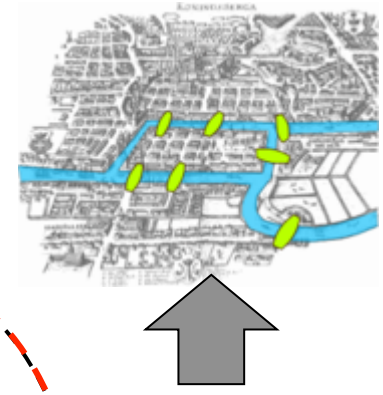
Single line of diffusion

- **Goal:** compact cell layout with as few extra contacts and metal-1 wires as possible.
  - That is: small area
  - That is: low parasitics at output and intermediate nodes.
- **Proxy:** single line of diffusion
  - That is: draw the entire p/n diffusion without "lifting the pen"
- **Tool:** Euler path

Graph theory: Euler paths







Euler path

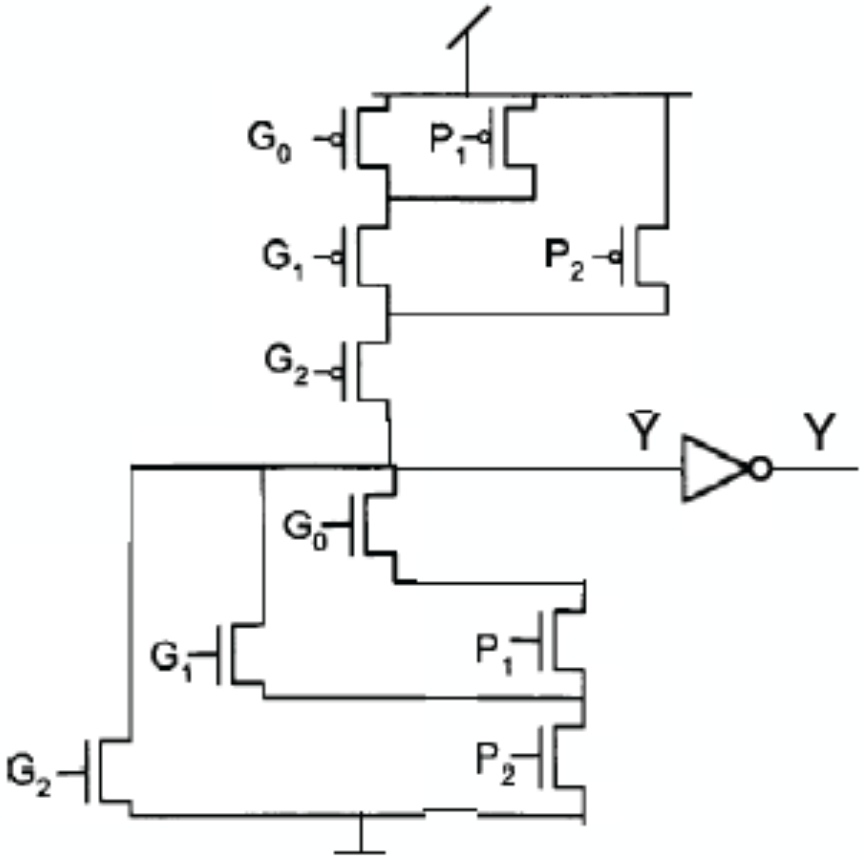
- Graph consists of vertices (circuit nodes) connected by edges (transistors).
- Euler path traverses every edge exactly once.
- An Euler path exists if:
  - Exactly two or zero vertices have an odd degree.
  - If two vertices have an odd degree the path starts and ends in these vertices

Example Euler paths

Is it possible to layout p-net, **as drawn,** with a single line of diffusion?

Is with it possible to layout n-net **as drawn,** with a single line of diffusion?

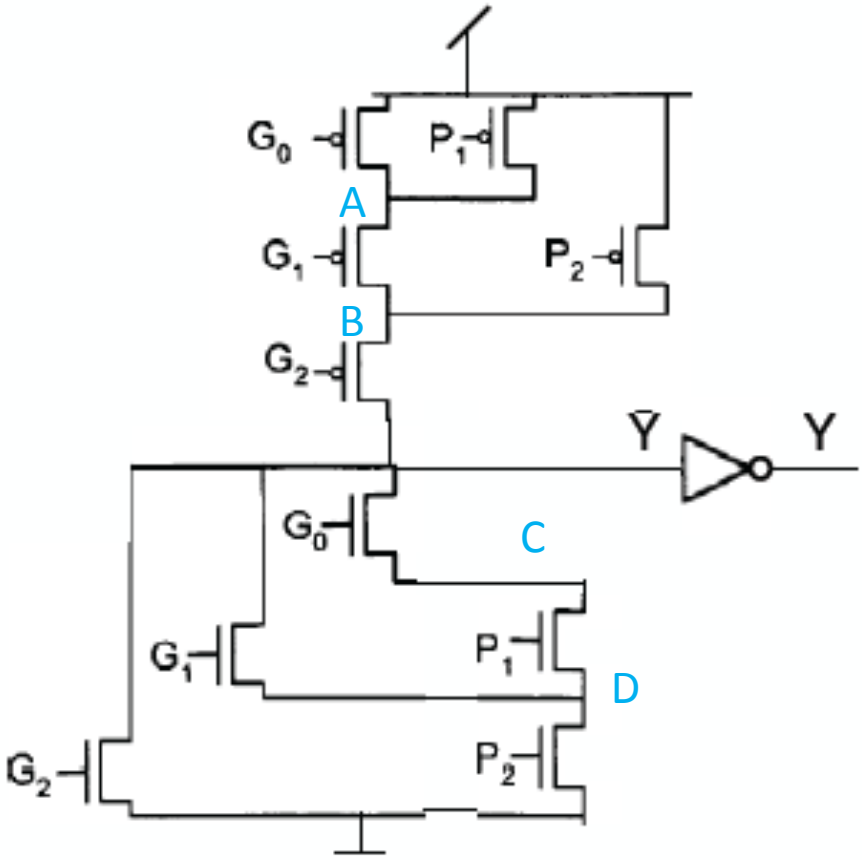
From exam 2017-10-26



Example Euler paths

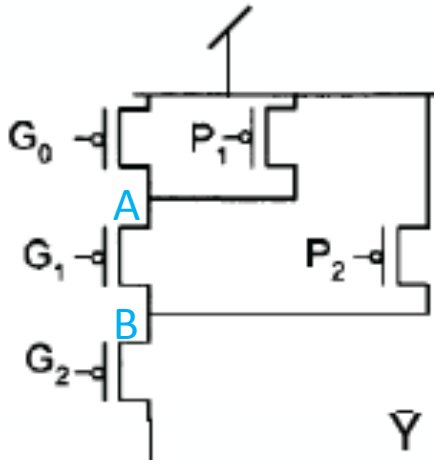
It is a good idea to label the circuit nodes that are neither the output, nor VDD or VSS.

I have done so here.
There are four such nodes:
A, B, C, D.



Example Euler paths

How many transistors are connected to each of the circuit nodes in the **p-net**?
VDD: 3
A: 3
B: 3
Y': 1

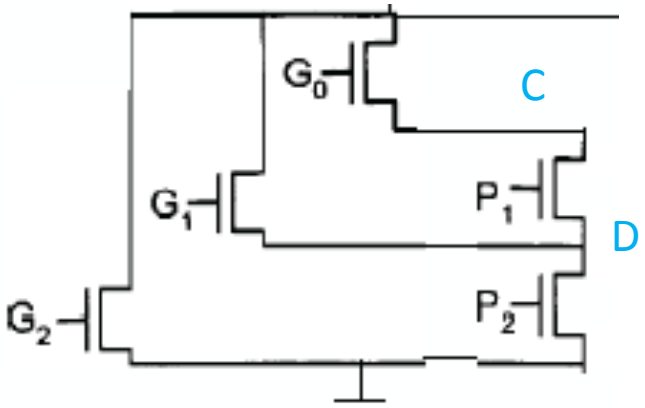


For an Euler path to exist there can only be 0 or 2 vertices (that is circuit nodes) with odd number of edges (that is transistors).

So with this schematic for the p-net there is no Euler path.

Example Euler paths

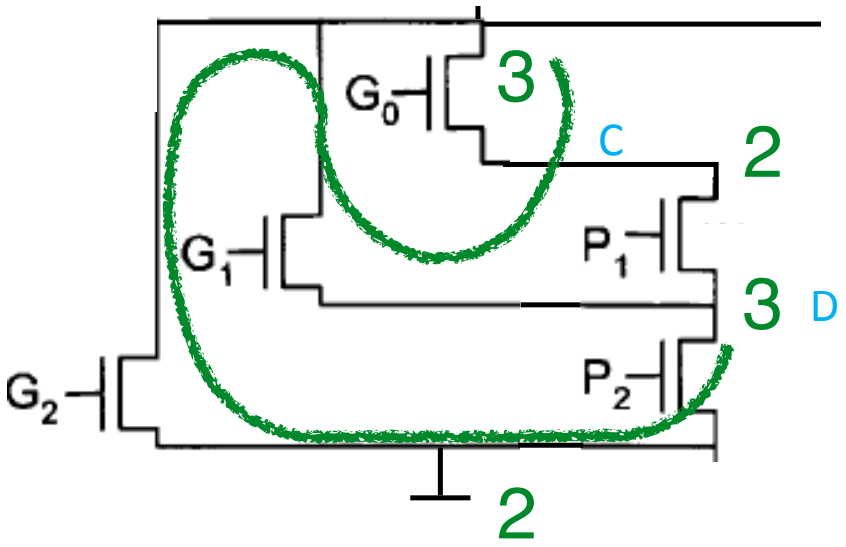
How many transistors are connected to each of the circuit nodes in the **n-net**?
VSS/gnd: 2
D: 3
C 2
Y': 3
There are two vertices (circuit nodes) with an odd number of edges (transistors) . Thus, an Euler path can be formed. It has to start and end in the circuit nodes with odd number of transistors: The output, Y, and internal node D.



Example Euler paths

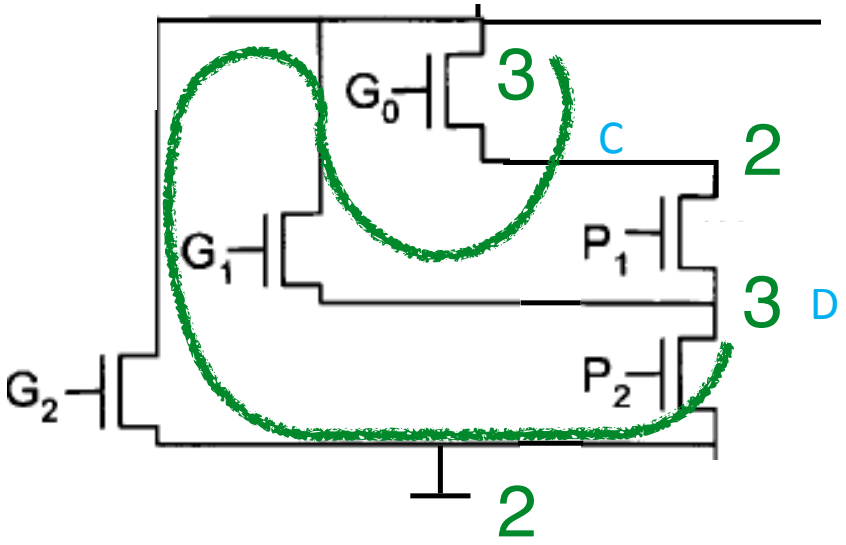
We have to start in a odd node and end in the other odd node.

Here is one solution. There are several other possibilities.

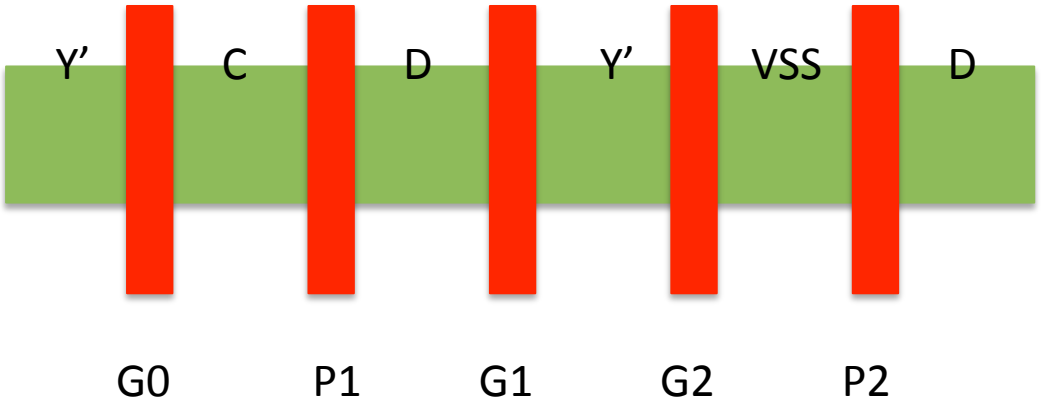


Example Euler paths

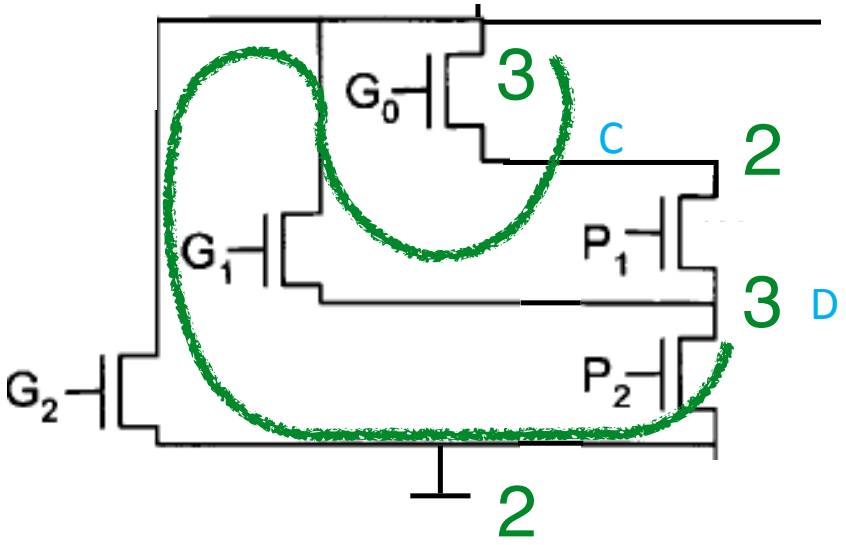
To map Euler path to a continuous line of diffusion start by labeling the transistors with theit signal name starting at one end of Euler path.



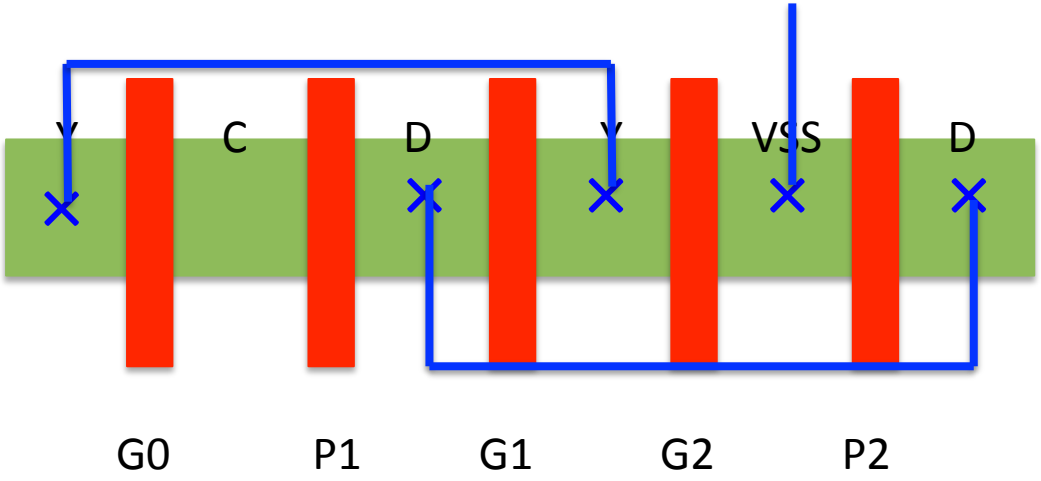
Example Euler paths



Then label also the circuit nodes along the path.

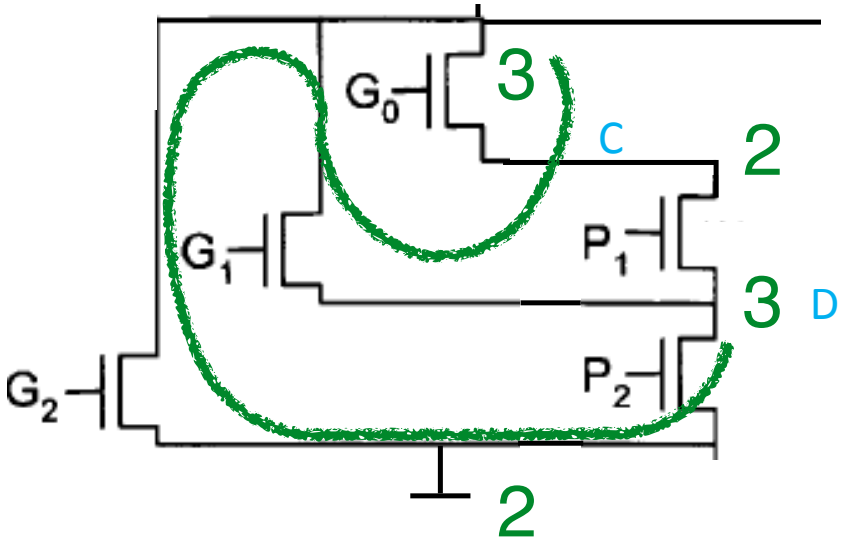


Example Euler paths



The make the connections for the source-drain areas that have the same circuit-node label.

I just draw it as a stick diagram here.



Example with quiz

Draw the schematic for a static CMOS gate with the logical function:

$$f=\overline{(A\cdot B+C\cdot D)\cdot(E+F+G)}$$

1 The n-net can be laid out with single line of diffusion. T/F

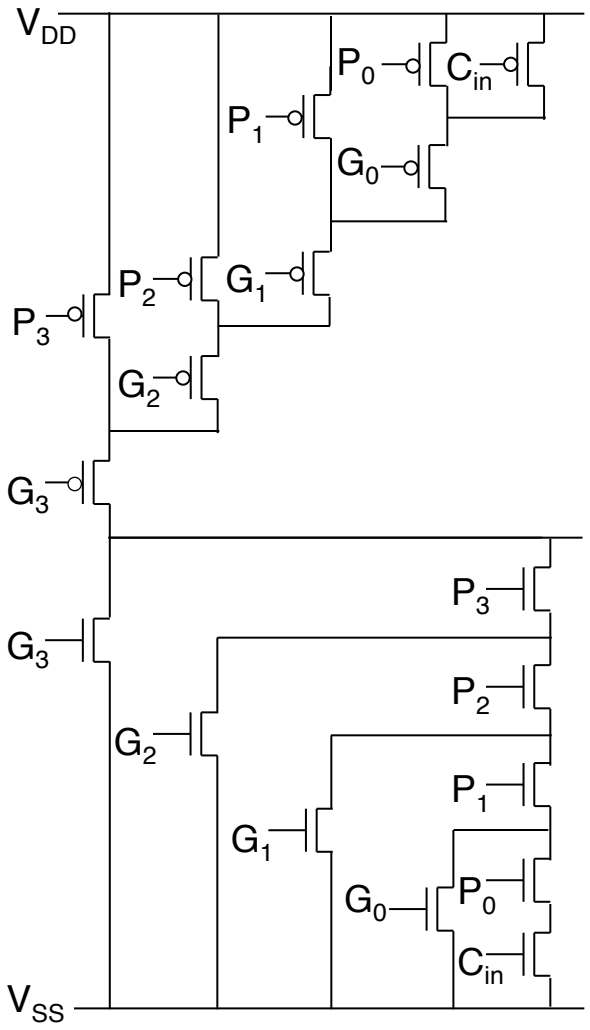
2 The p-net can be laid out with single line of diffusion. T/F

3 Can you make the order ABCDEFG work for the n-net?

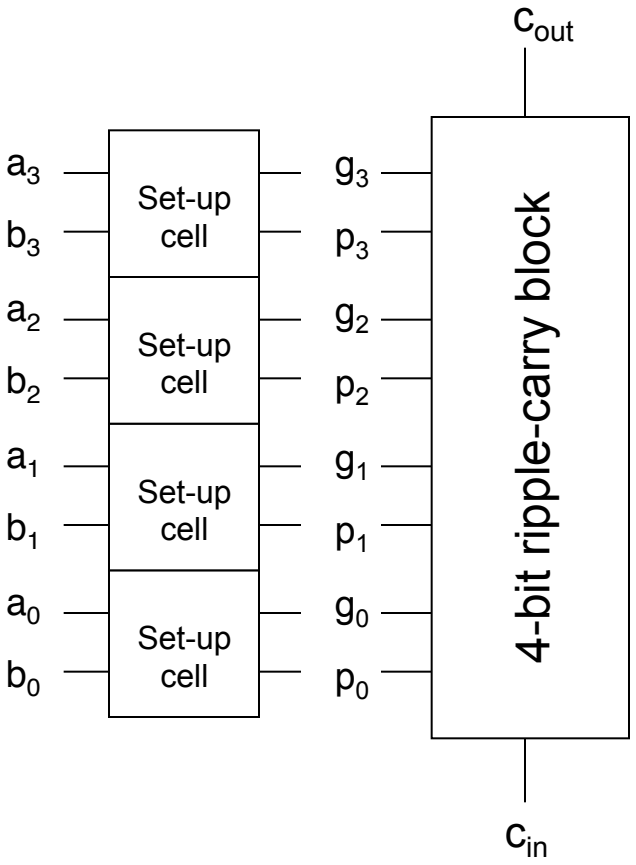
4 Can you make the order ABCDEFG work for the p-net?

5 It is possible to find a order of the input so that single-line-of-diffusion layout for is possible for both the n-net and the p-net at the same time. T/F

Gate Matrix Layout

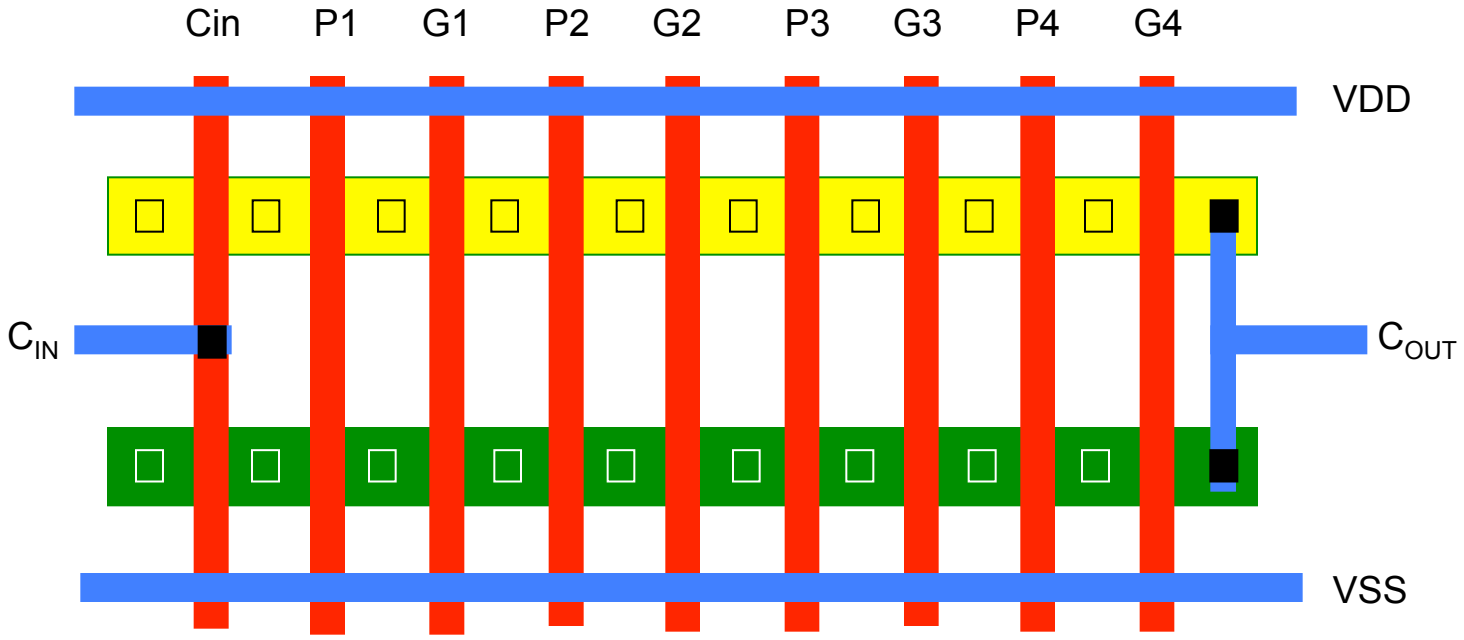


$C_{out}=G_3+P_3(G_2+P_2(G_1+P_1(G_0+P_0C_{in})$

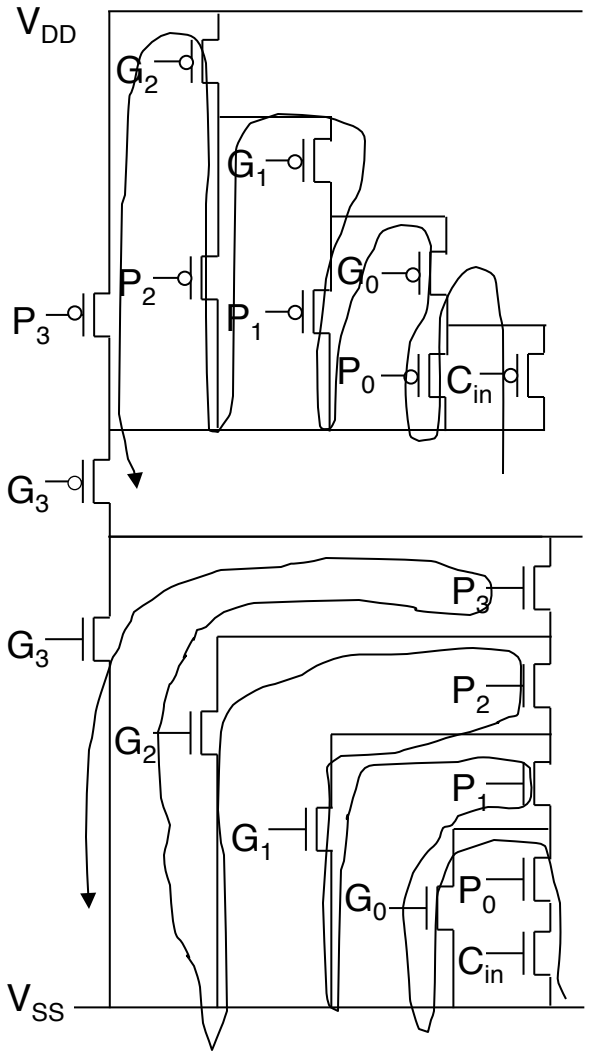


Gate Matrix Layout

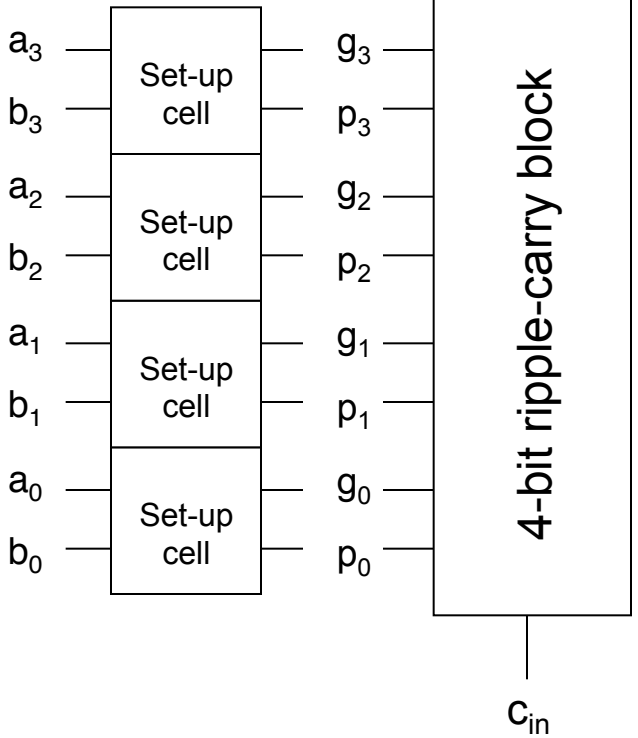
Our task in this example: We have been given the seemingly impossible task to layout the 4-bit ripple-carry block using the layout template given below, with the given gate order!!



Gate Matrix Layout

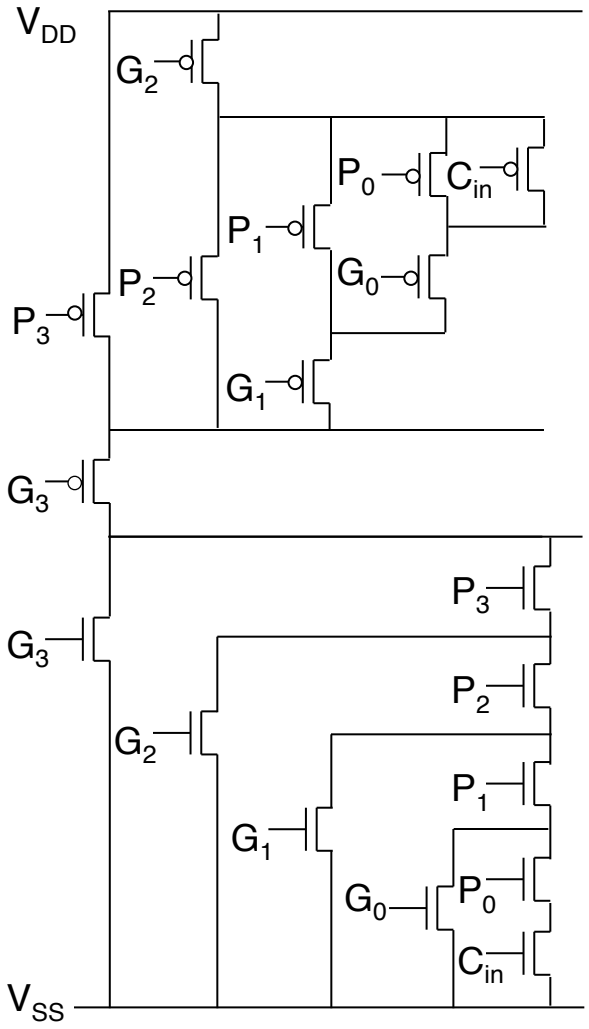


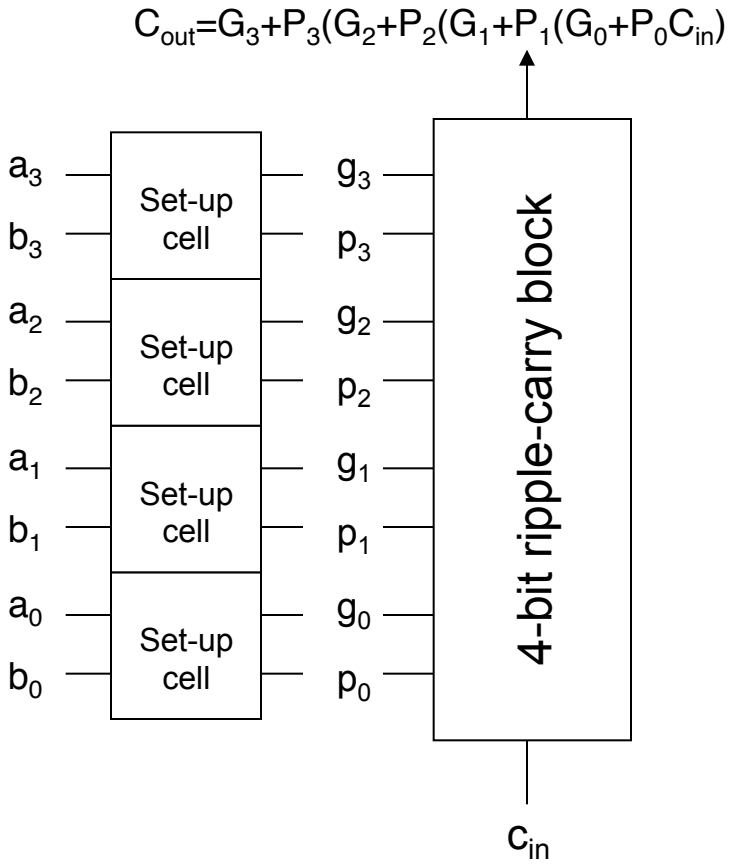
$C_{out}=G_3+P_3(G_2+P_2(G_1+P_1(G_0+P_0C_{in}))$



It seems impossible to pass all MOSFETs in the given order without passing some MOSFETs twice!

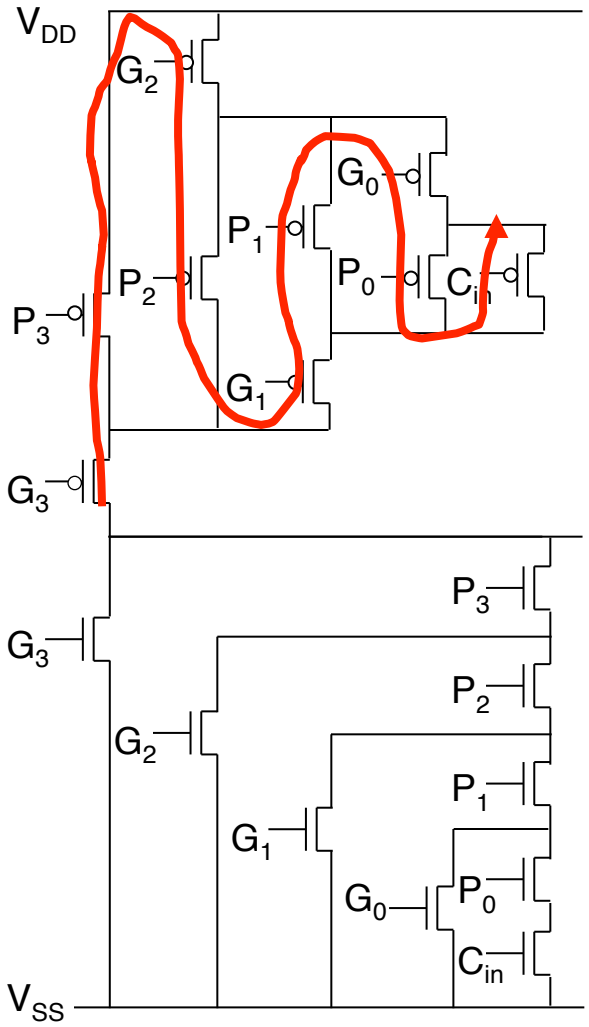
Gate Matrix Layout

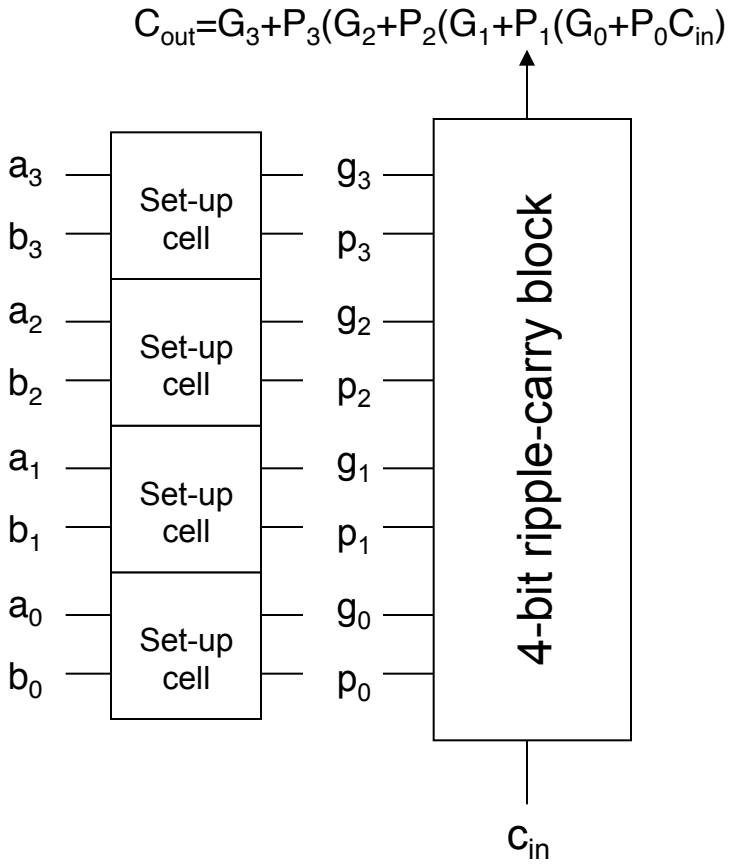




However, there is a solution! MOSFET blocks can be rearranged in the schematic with same functionality.

Gate Matrix Layout





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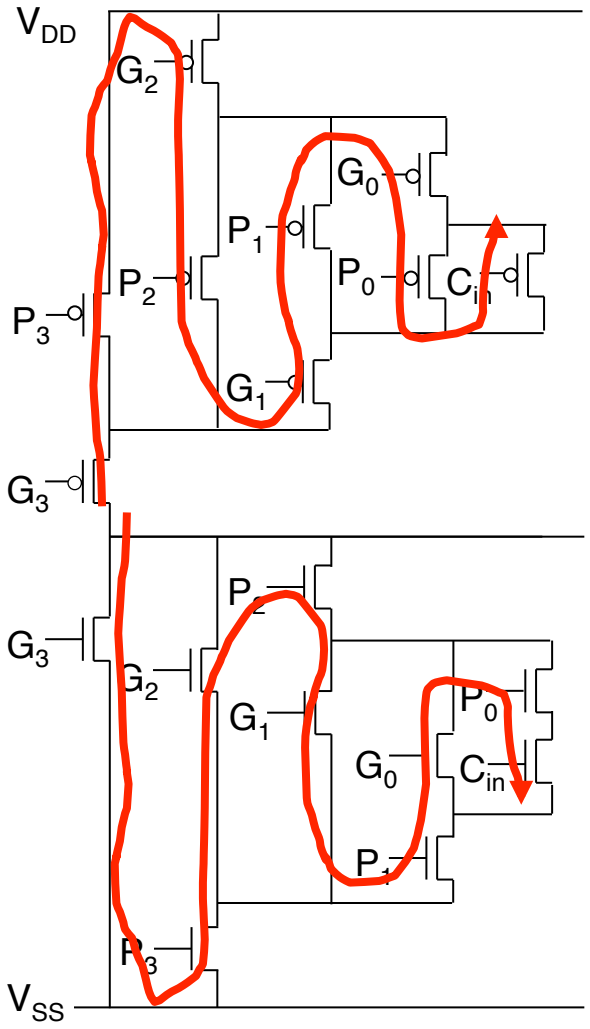
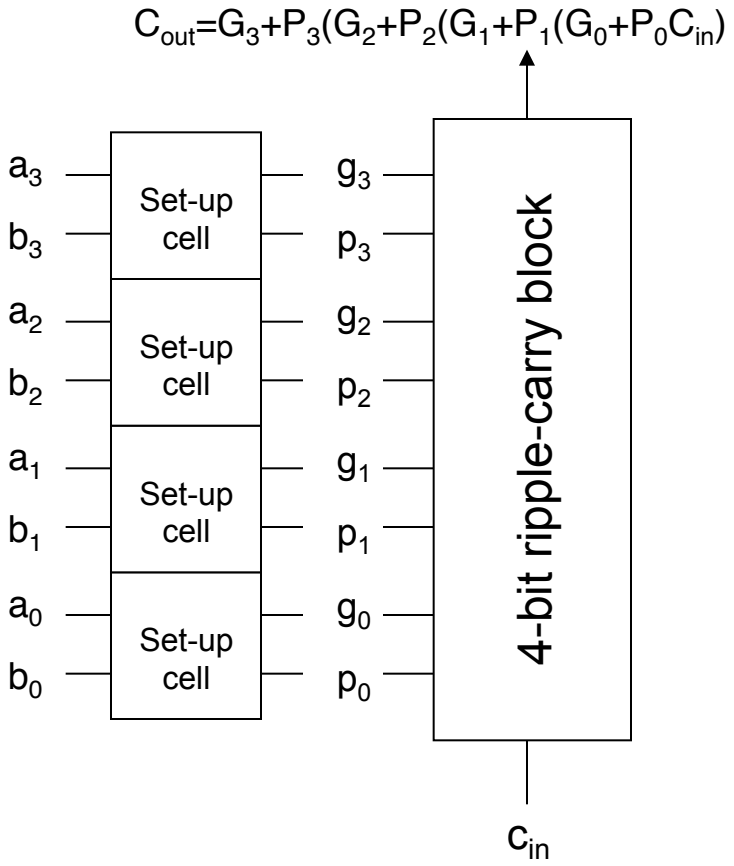
Gate Matrix Layout

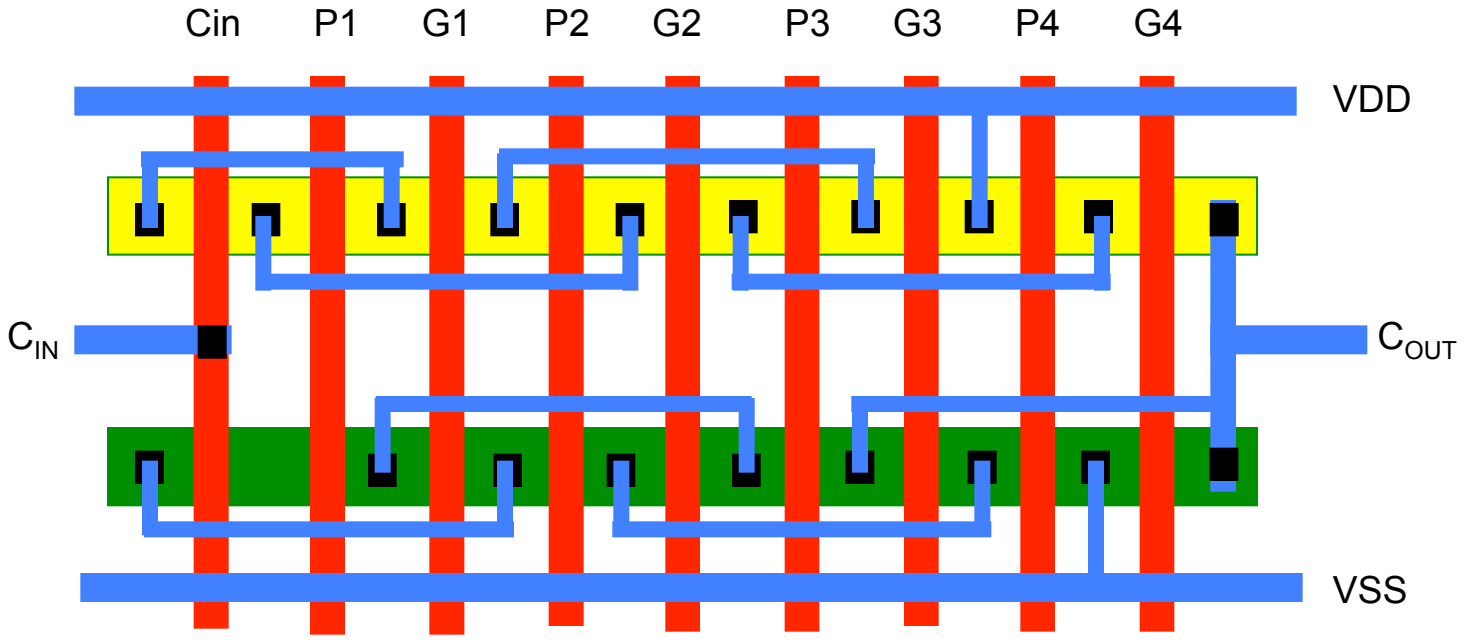




However, there is a solution! MOSFET blocks can be rearranged in the schematic with same functionality.

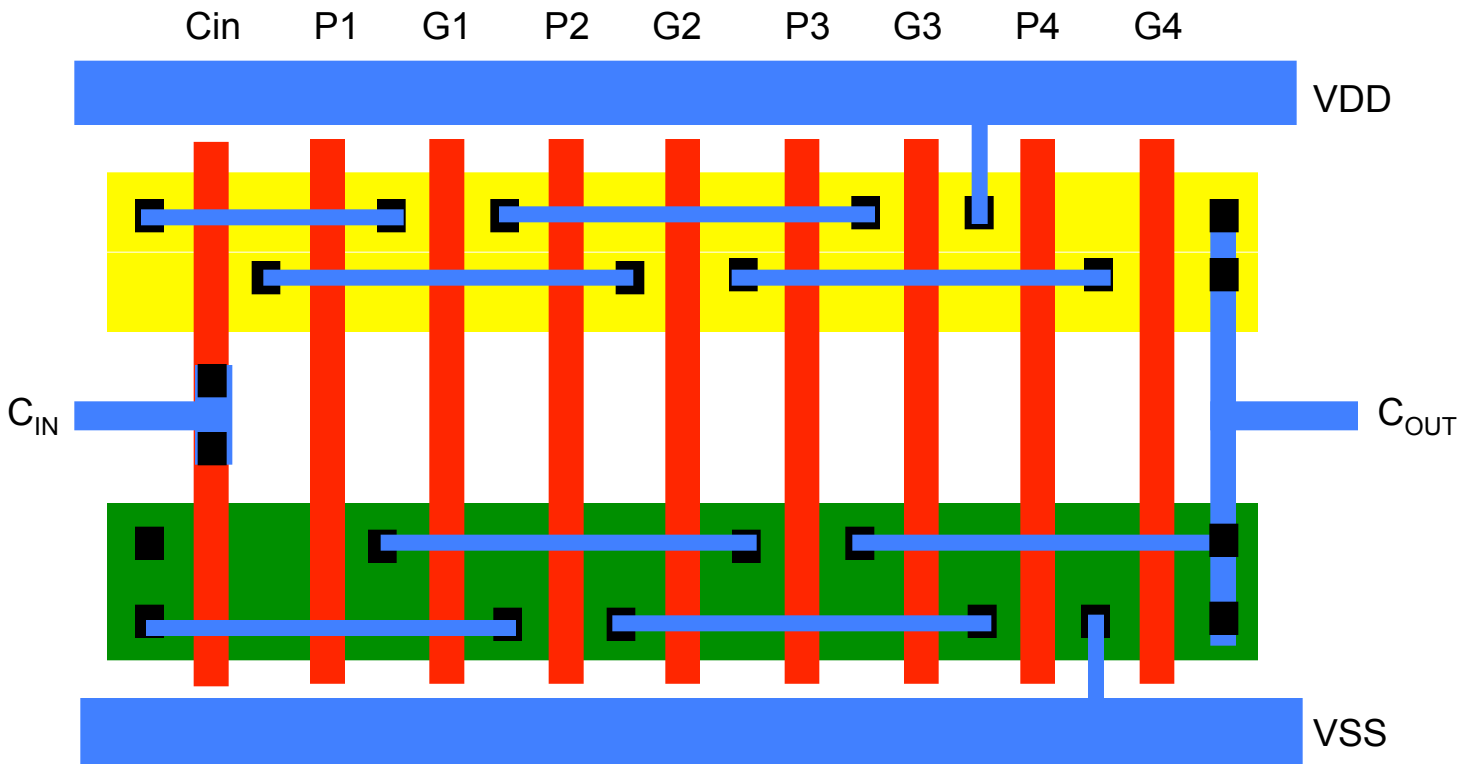
Gate Matrix Layout

Here is the resulting layout!



Gate Matrix Layout

The layout again, a bit more refined!

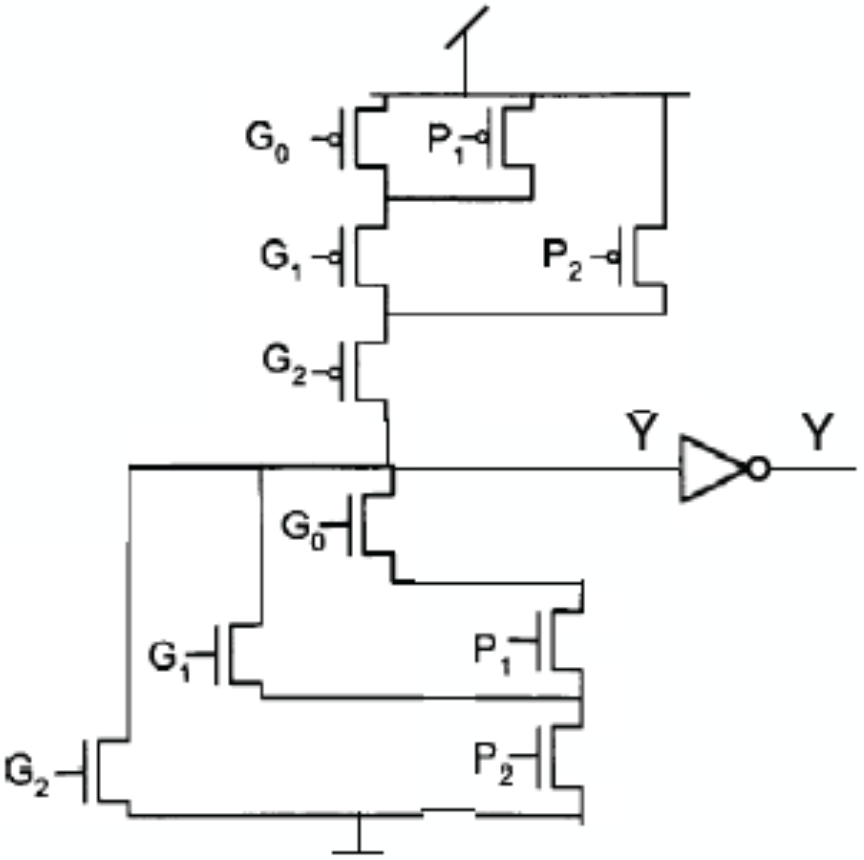


The layout is very compact and elegant, however, only post-layout circuit simulations with node capacitances extracted from the layout will reveal the exact performance of the cell.

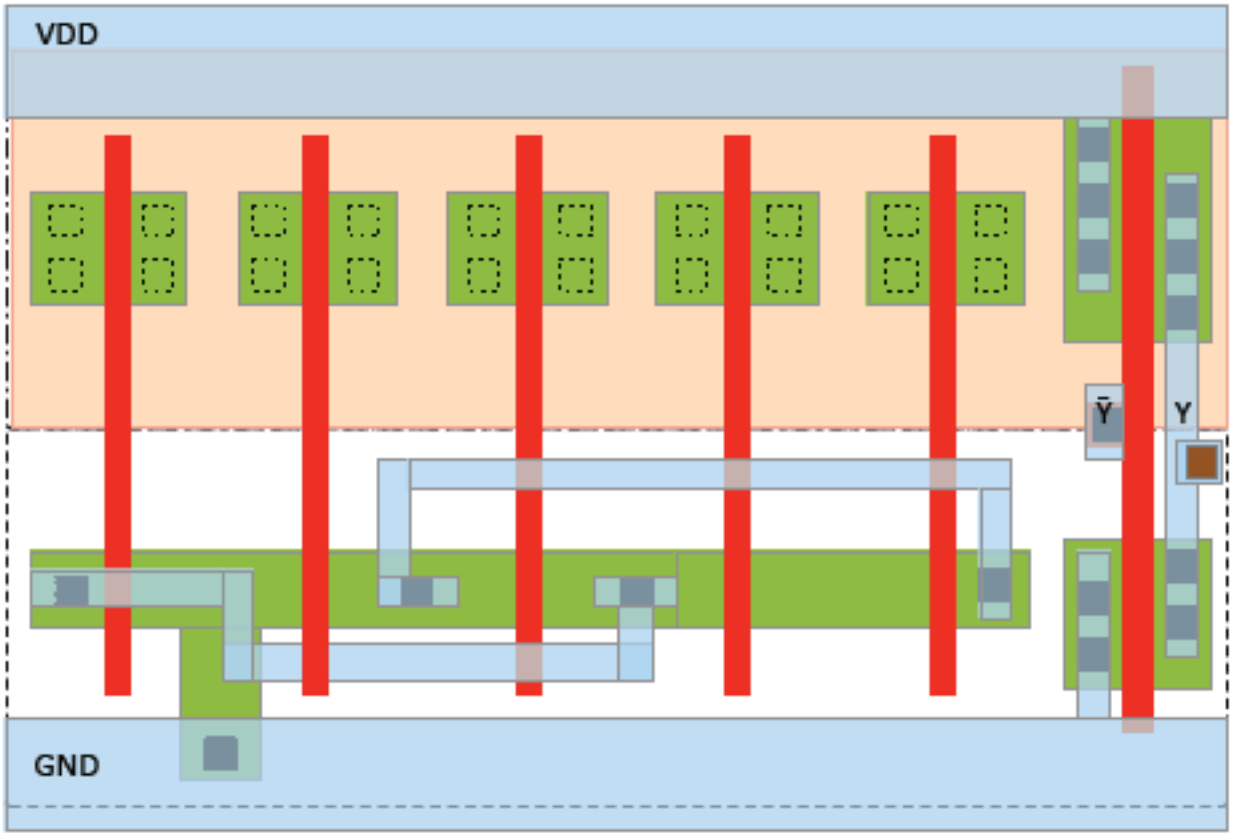
Example Layout

Complete the layout of this cell shown in the template in 3 where the n-net has already been completed. Note that for simplicity all transistors have the same widths in the template, although that may not be optimal.

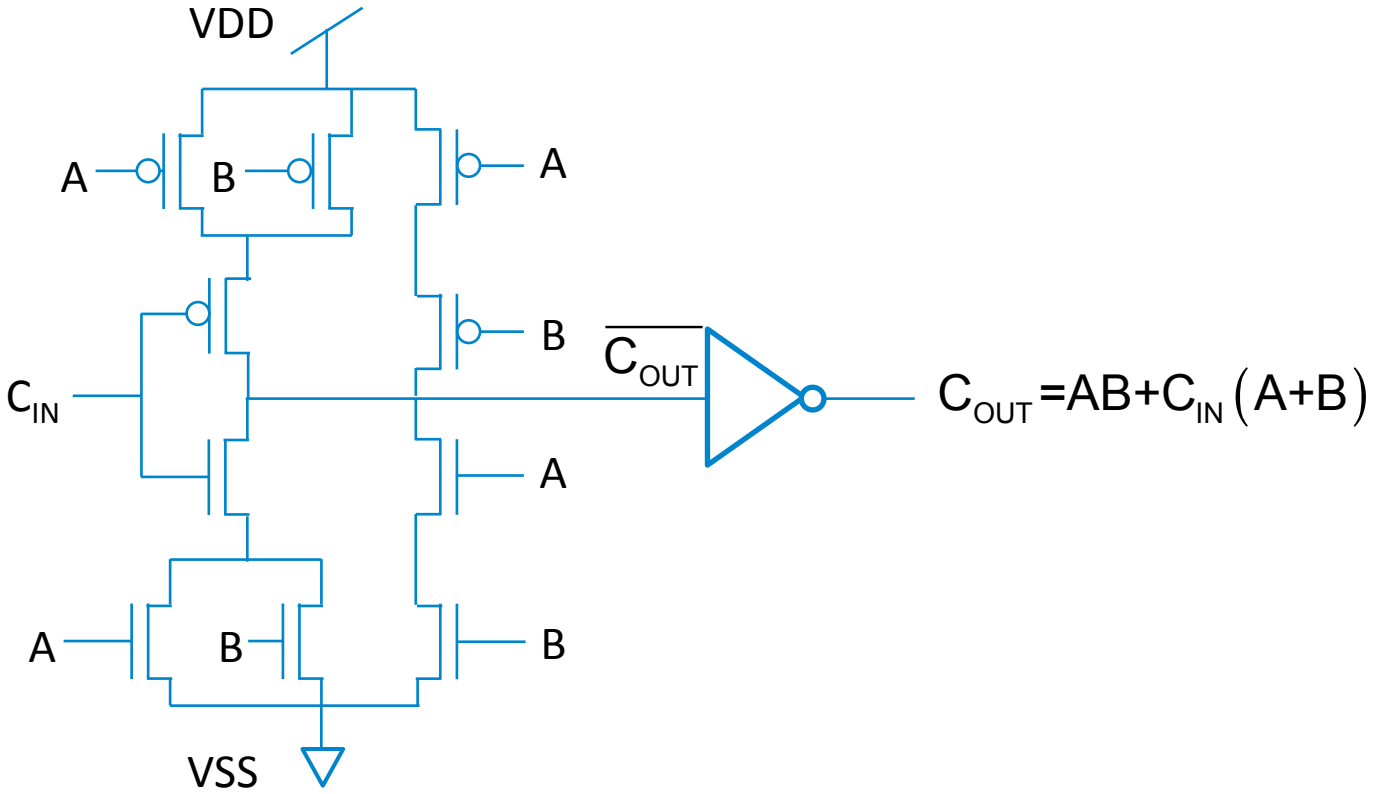
Identify the five inputs and mark them clearly in the template. Then draw the required connections for the p-net. Merge as many p-di usion areas as possible to simplify your layout.

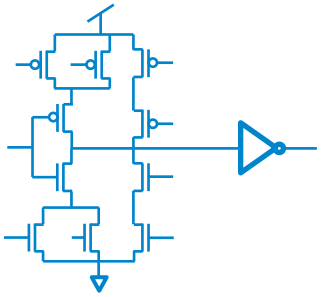


Example layout



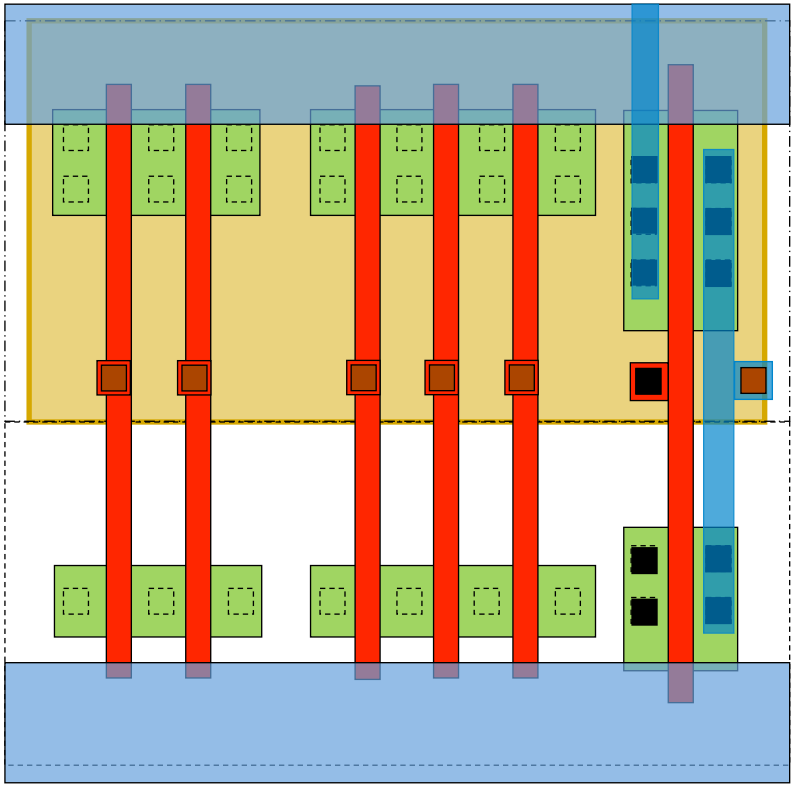
Layout of the carry cell

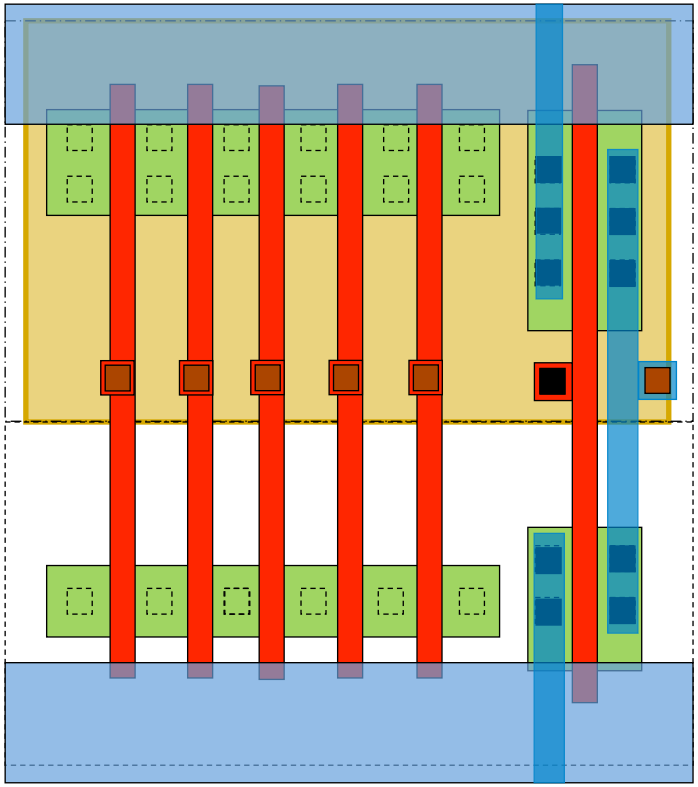




Layout of the carry cell

$$C_{OUT} = AB + C_{IN}(A+B)$$



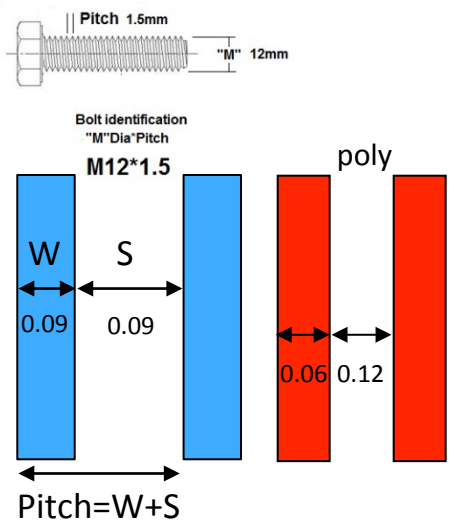


Connecting to a standard cell

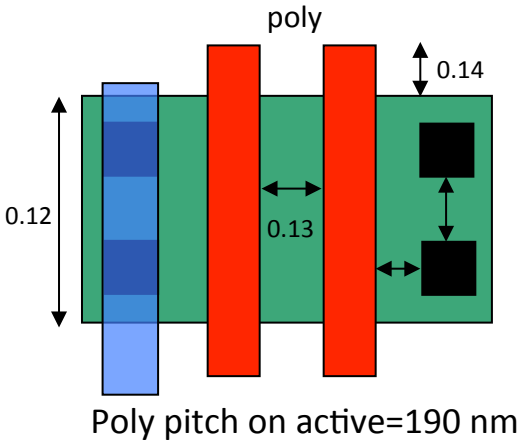
- Standard cell input/output ports can be placed anywhere in the cell
  - Router routes in higher metal layers to port
  - But there can be only one connection port per signal!
- Lab 3 cells should be abutted
  - C_{in} input on the edge of one end
  - C_{out} output on the edge of other end
  - Treat A & B as if they can be connected anywhere in the cell.

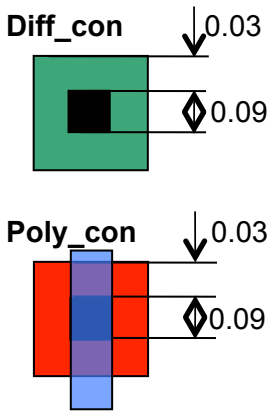
Design rules

- We will talk about geometric design rules in more detail on Thursday, but . . .
- . . . you probably need to know already now that there are intralayer rules and interlayer rules
- Intralayer rules: width and spacing rules for each individual layer



- Interlayer rules between layers





General rules for CMOS layout

- Run supply lines for VDD and VSS along the upper and lower cell boundaries
- Run a vertical poly wire for each input signal
- Order the poly wires to obtain maximal connectivity between transistors through abutment of source/drain areas. Connected transistors then form transistor segments.
- Place n-transistor segments close to the bottom VSS supply rail and p-transistors close to the top VDD supply rail
- Wires necessary to complete the design are drawn in metal, poly, or, if necessary in diffusion (for instance when connecting segments to the supply rails).
- Remember to keep internal node capacitances at a minimum!