# Introduction to on-chip interconnect

Lecture 7

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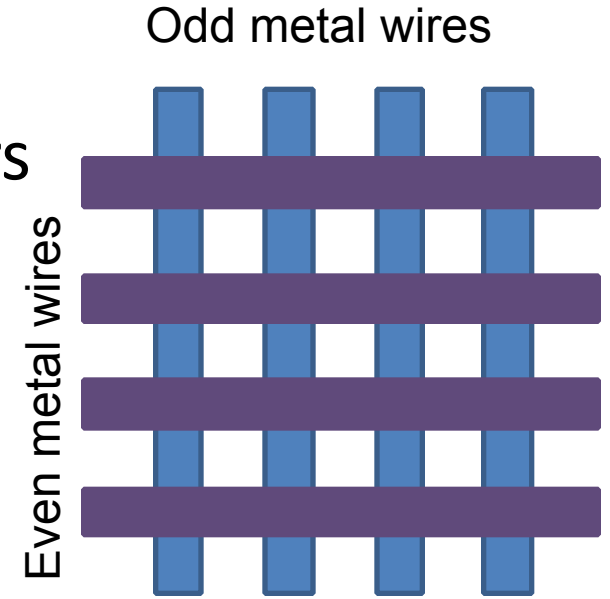
# Outline

- Introduction
- Interconnect Modeling
  - Wire Resistance
  - Wire Capacitance
- Wire RC Delay
- Elmore delay model
- Handling wires with branches

# Introduction

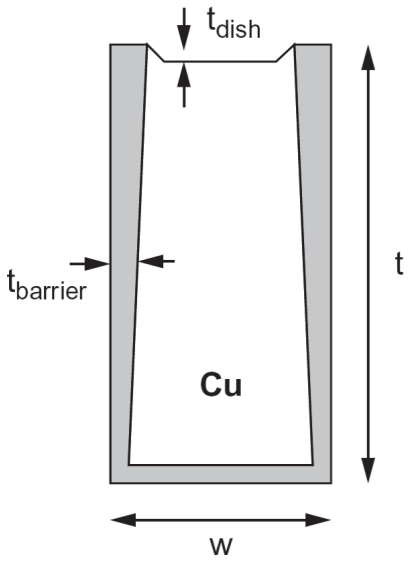
- Chips are mostly made of wires called *interconnect*
  - In stick diagram, wires set size
  - Transistors are little things under the wires
  - Many layers of wires
- Wires are as important as transistors
  - Speed
  - Power
  - Noise
- Alternating layers run orthogonally



# Choice of metals

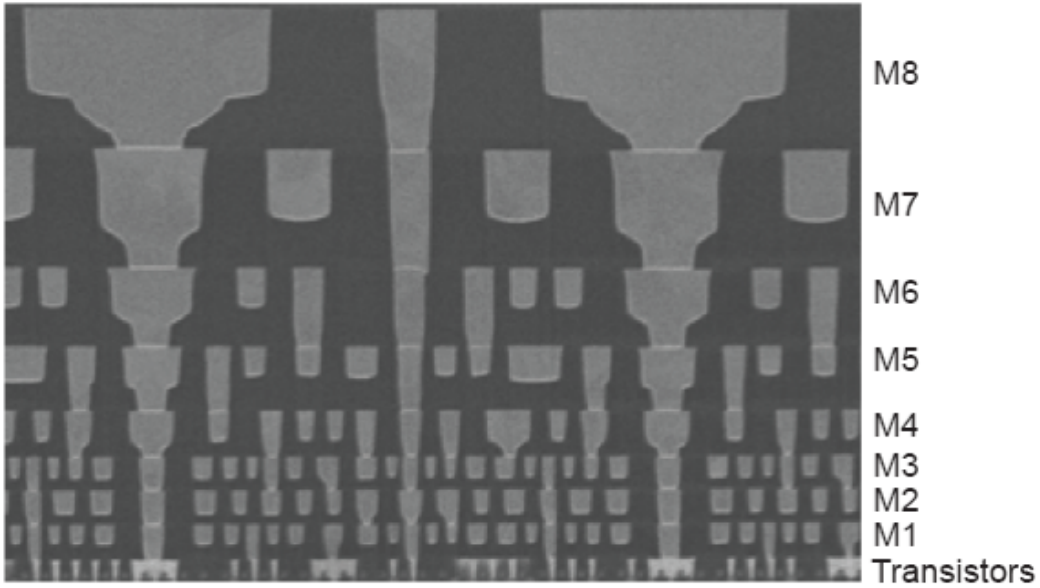
- Until 180 nm generation, most wires were aluminum
- Contemporary processes normally use copper
  - Cu atoms diffuse into silicon and damage FETs
  - Must be surrounded by a diffusion barrier

| Metal | Bulk resistivity (μΩ·cm) |
|---|---|
| Silver (Ag) | 1.6 |
| Copper (Cu) | 1.7 |
| Gold (Au) | 2.2 |
| Aluminum (Al) | 2.8 |
| Tungsten (W) | 5.3 |
| Titanium (Ti) | 43.0 |

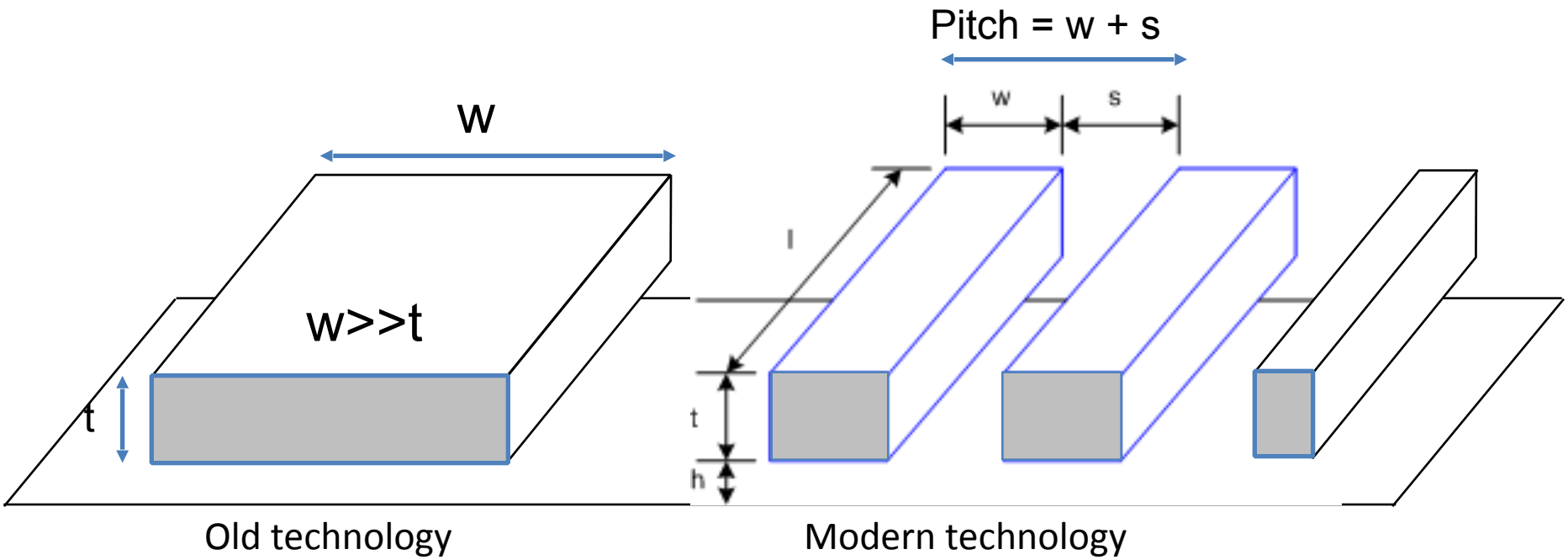


# Layer stack

- AMS 0.35 μm process has 3 metal layers
  - M1 for within-cell routing
  - M2/M3 for vertical/horizontal routing between cells
- Modern processes use 6-10+ metal layers
  - M1: thin, narrow (< 1.5 × minimum feature size)
    - High density wiring in cells
  - Mid layers: thick, wide
    - Global interconnect
  - Top layers: THICK, WIDE
    - For $V_{DD}$, GND, clk



# Wire geometry




Today: pack in many skinny wires!

For long skinny wires resistance cannot be neglected since cross sectional area shrinks with feature size, wire length stays the same or increases.

Hence: wire resistances can no longer be neglected!

# Wire geometry

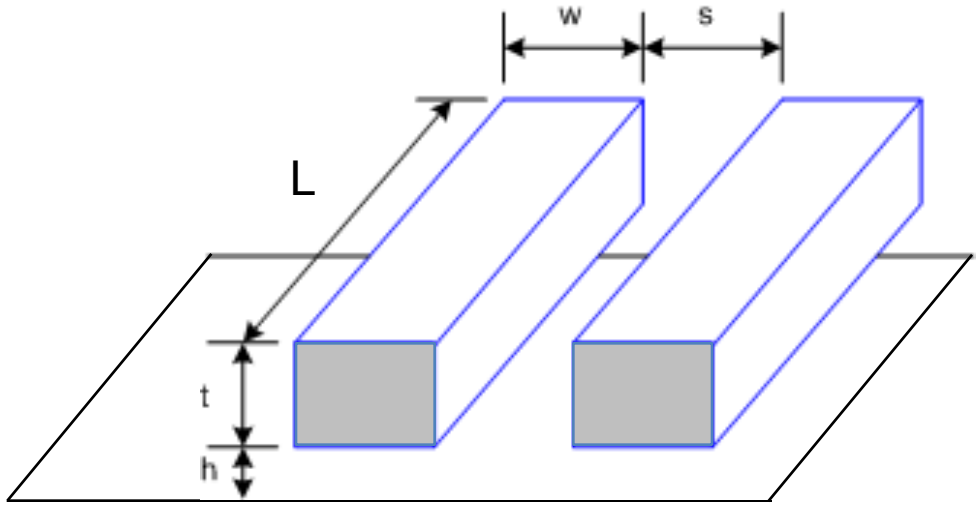
- Long skinny wires
  - wire resistance cannot be neglected

$$R = \rho \frac{L}{A} = rL$$

- Wire length is increasing with large chips
- Wire cross sectional area shrinks with feature size
- Wires can no longer be modeled as capacitances alone
- We need improved wire models that considers wire resistance along with wire capacitance!
- Model must be distributed between at least two circuit nodes!

# Wire resistance

$$R = \rho \frac{L}{A} = rL$$



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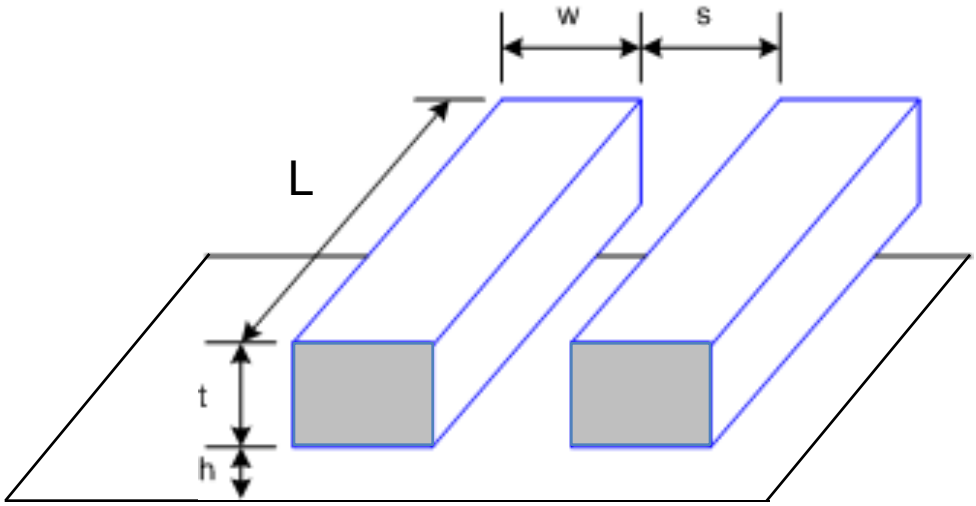

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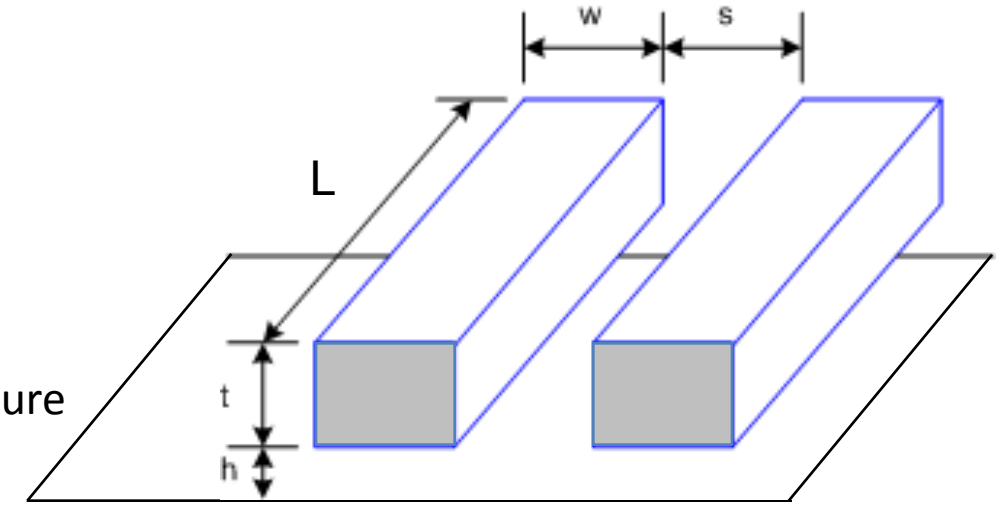

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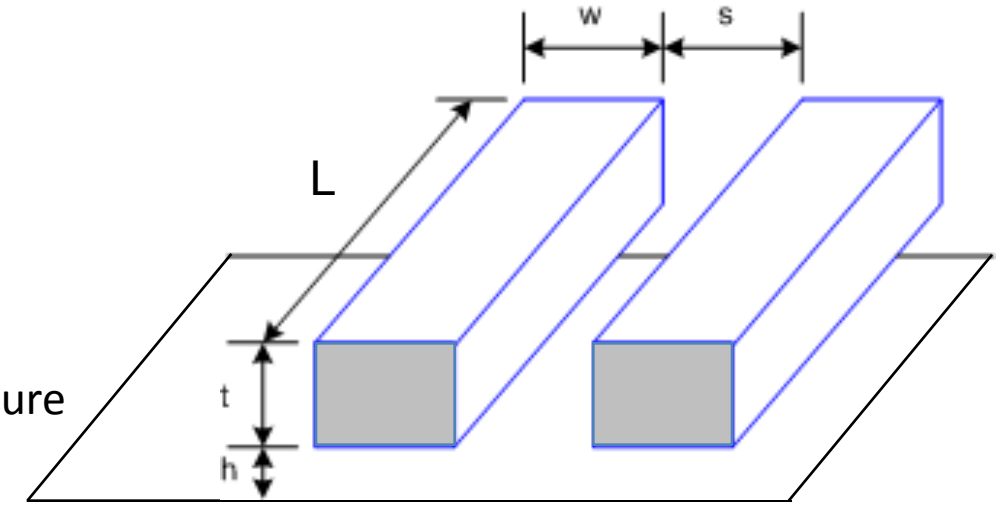

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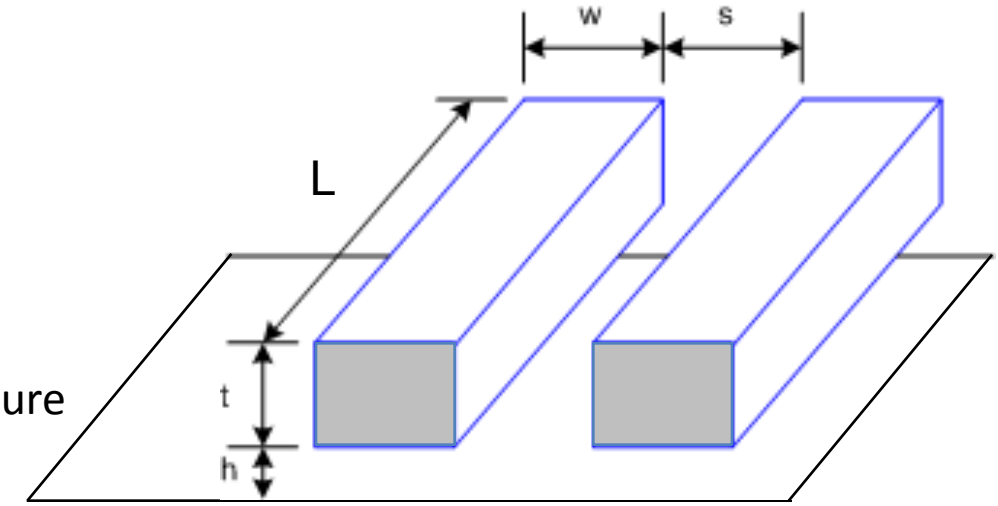


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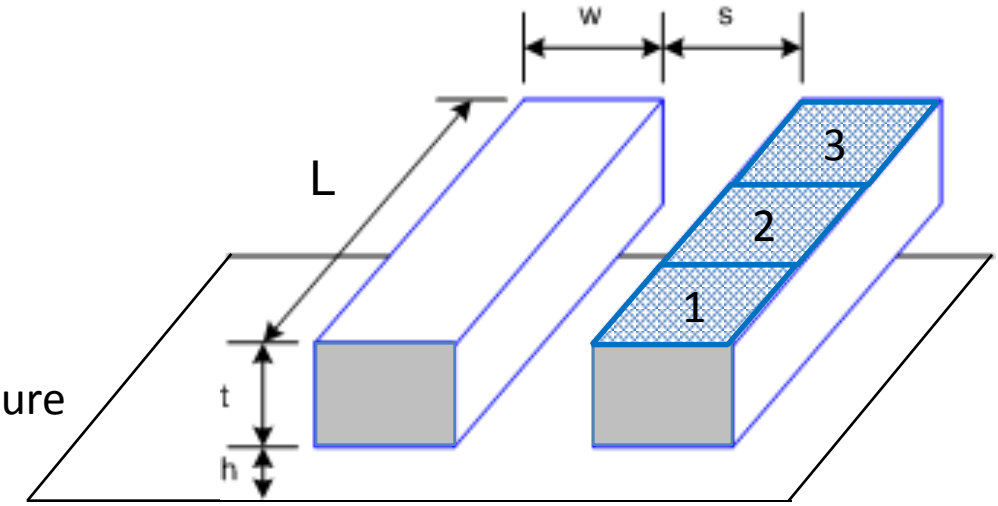


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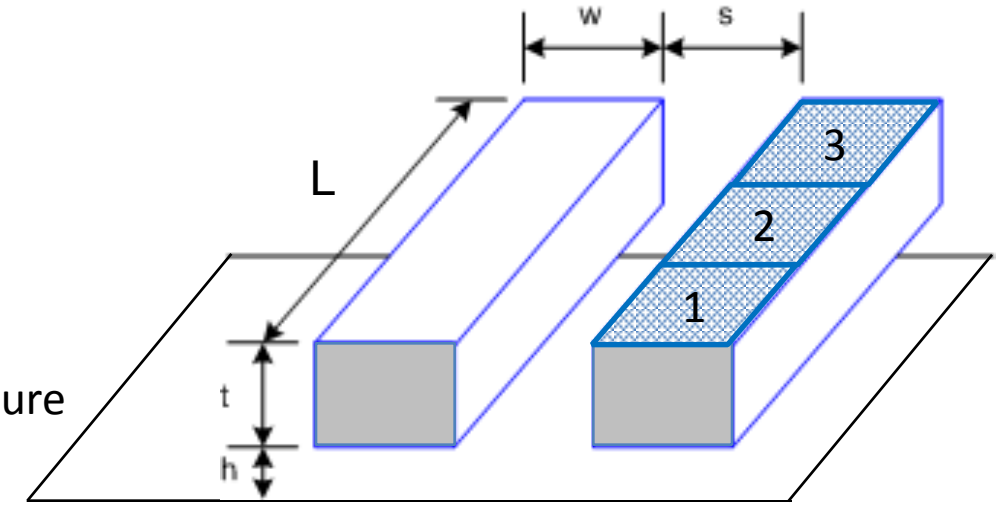


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The ”number of squares” in the direction of current flow is L/W

If we assign a certain width, $W_0$, to all wires in certain layer they will all have the same resistance per unit length, $r=R_S/W_0$

# Example

- Estimate the sheet resistance of a 220 nm thick copper wire if the resistivity of the thin copper film is 22 nΩ·m.

$R_S$ =

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- Find the total resistance if the wire is 0.125 μm wide and 1 mm long. (Ignore the barrier layer)

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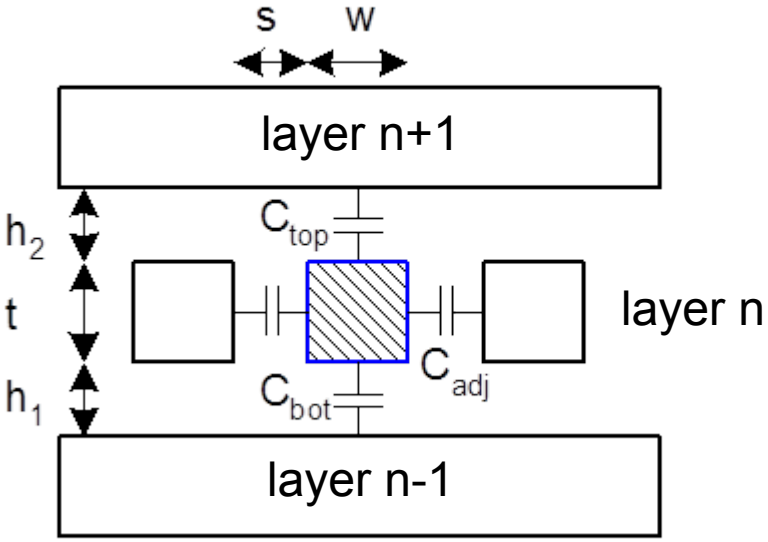
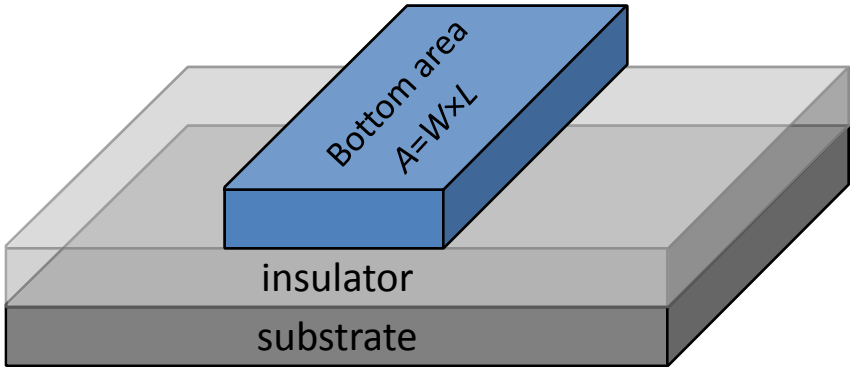
- Wires 125 nm wide have a resistivity per unit length of 800 Ω/mm

# Wire capacitance

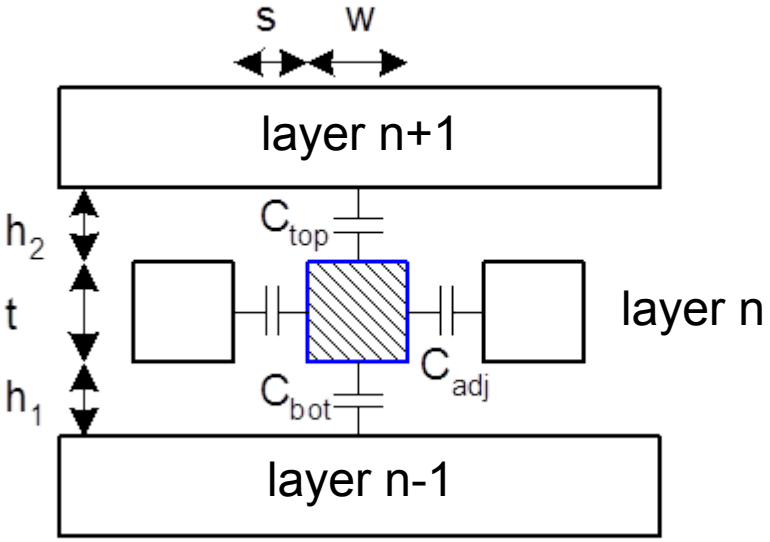


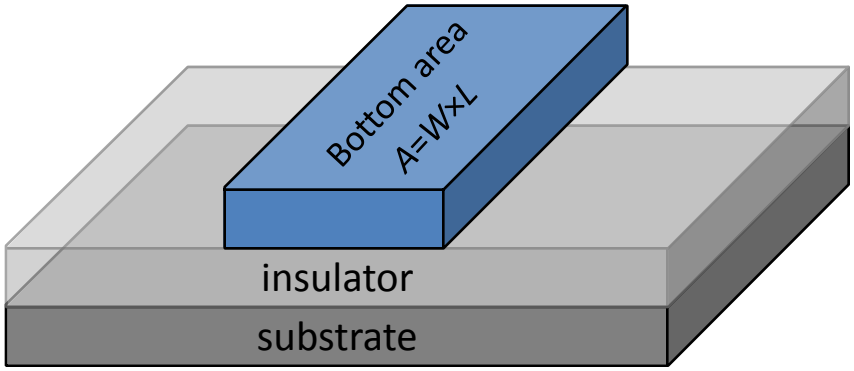




Wires have a capacitance *c* per unit length

- to neighbors in the same layer
- to layers above and below

# Wire capacitance

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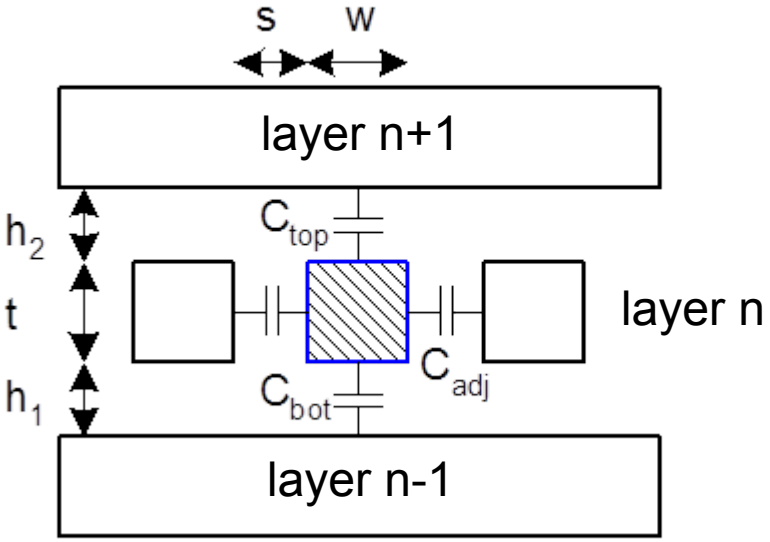
Parallel-plate capacitance equation

- $C_{pp} = \varepsilon A/h$, where top/bottom area $A=W\times L$
- $\varepsilon=\kappa\varepsilon_0$, $\varepsilon_0=8.85\cdot10^{-12}$ F/m in vacuum
- $SiO_2$ permittivity is $\kappa\approx4$
- low-kappa materials have $\kappa<3$

# Wire capacitance

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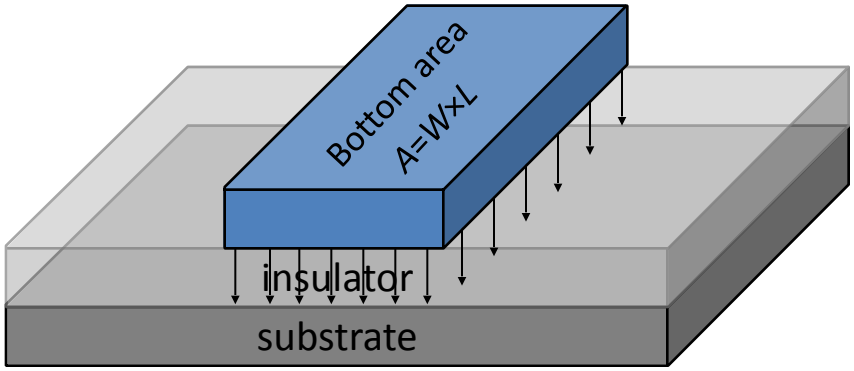


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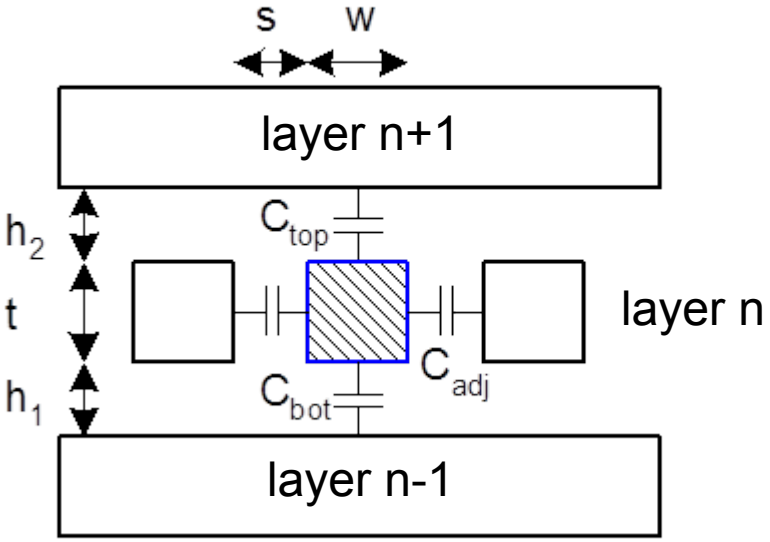


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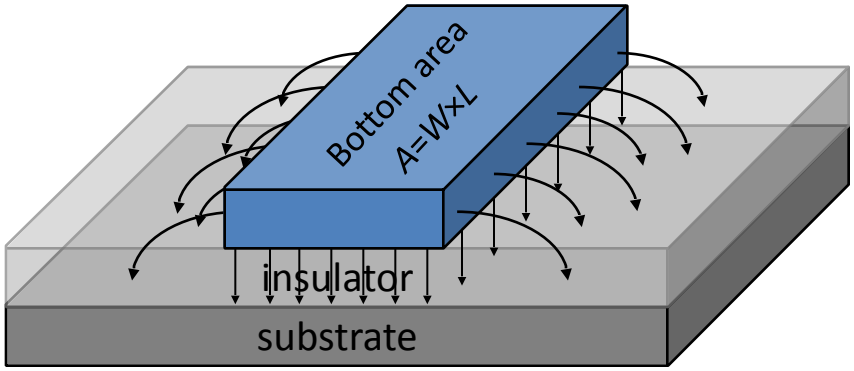


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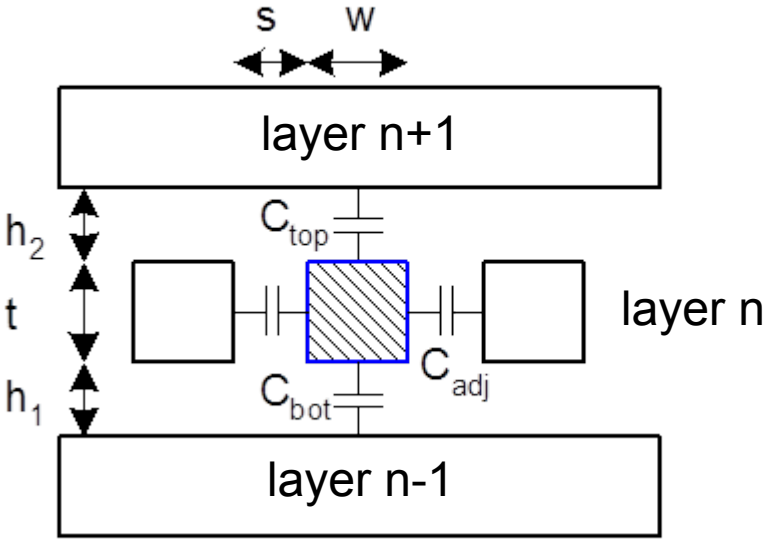


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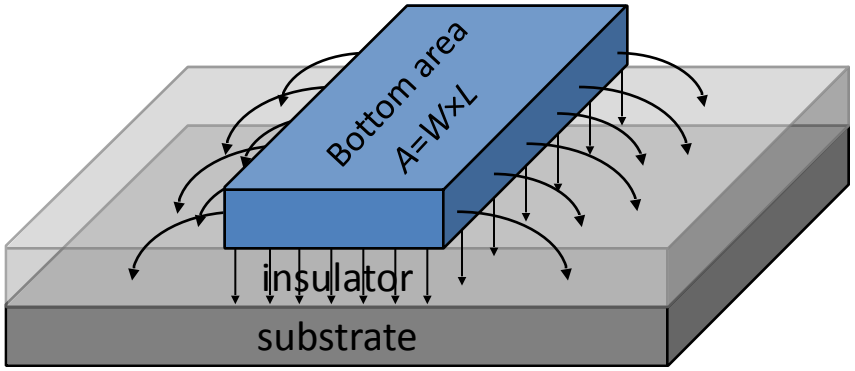


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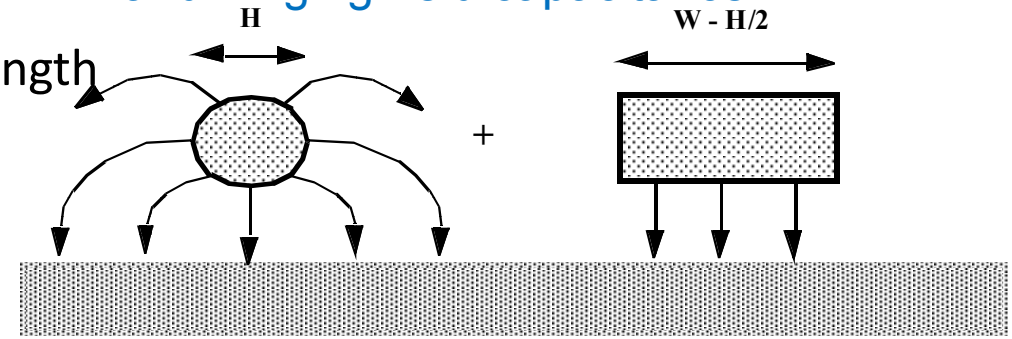


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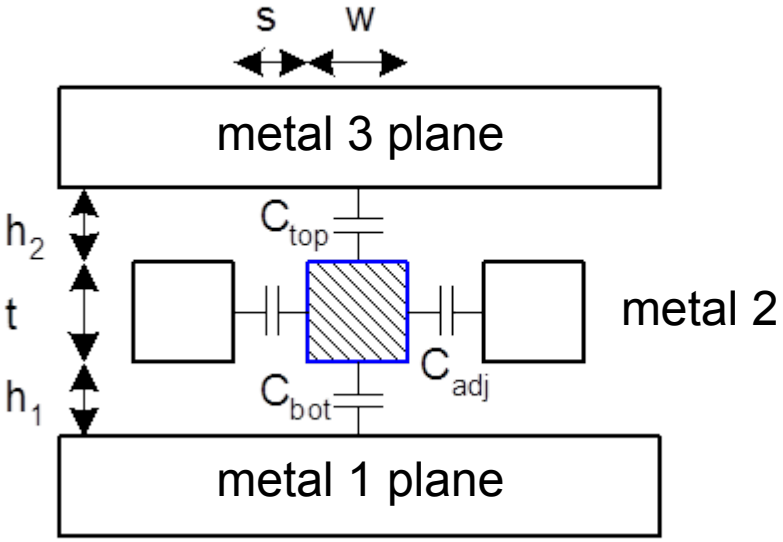
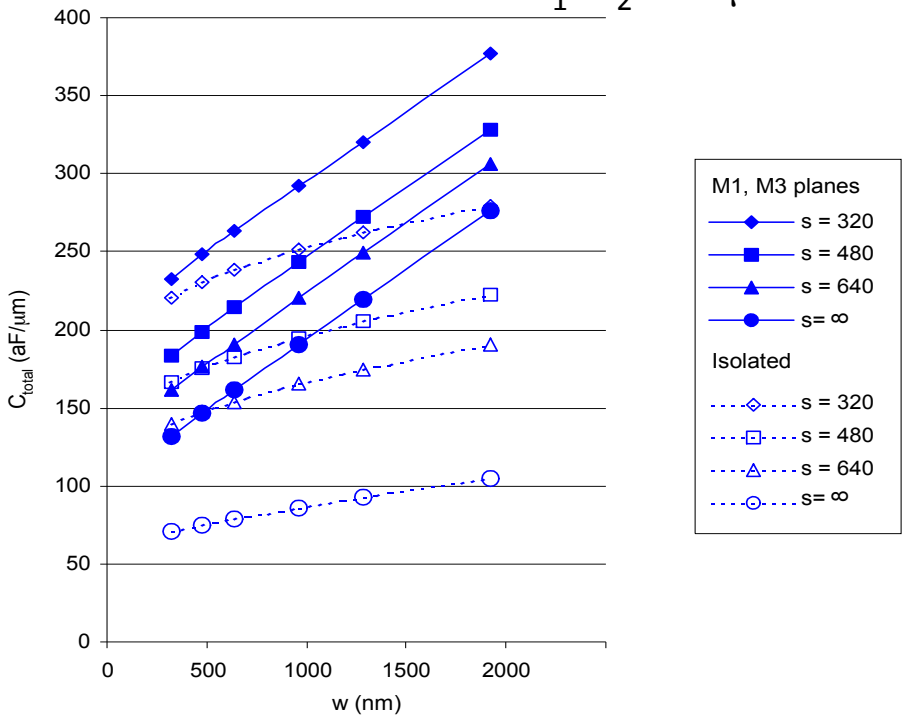
$$c_{wire} = c_{pp} + c_{fringe} = \frac{w\varepsilon_{di}}{t_{di}} + \frac{2\pi\varepsilon_{di}}{\log(t_{di}/H)}$$

Note: Cap is per unit length

# Metal2 Capacitance Data




$t=h_1=h_2=0.7\ \mu m$




Wire has capacitance *c* per unit length

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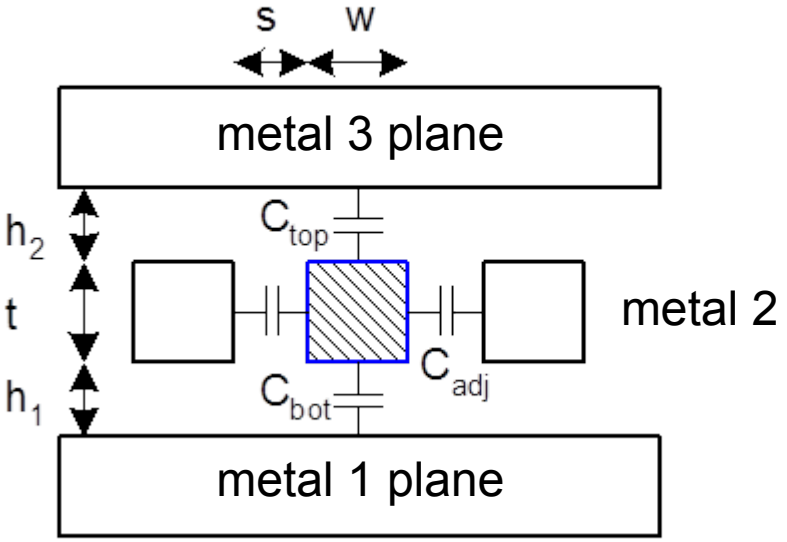


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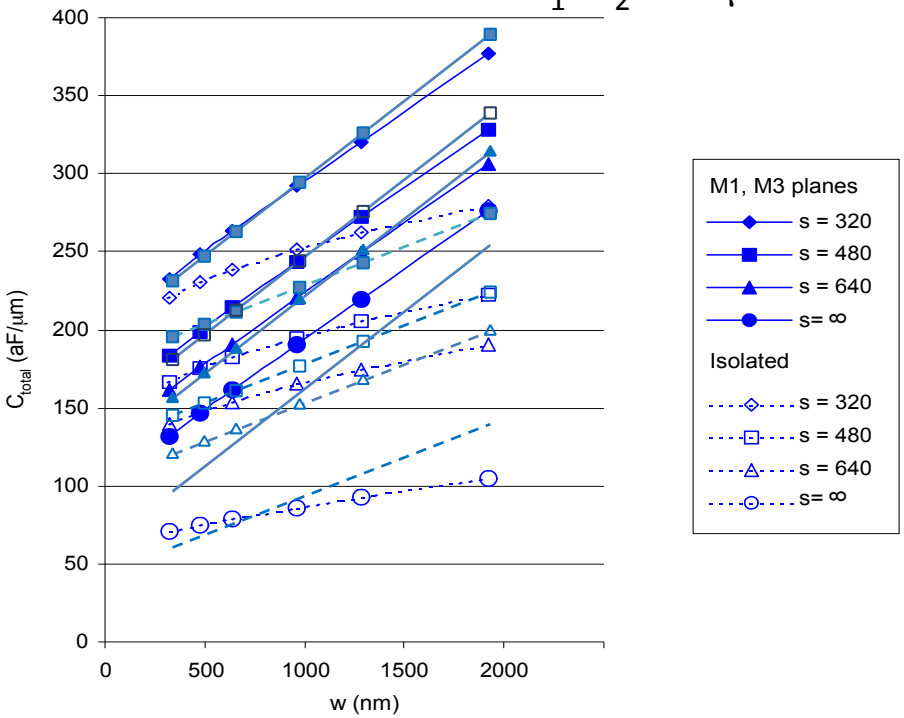


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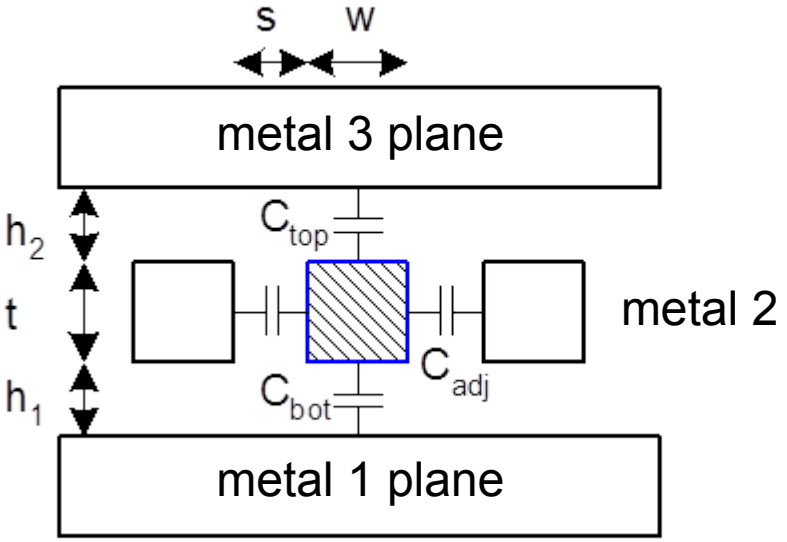


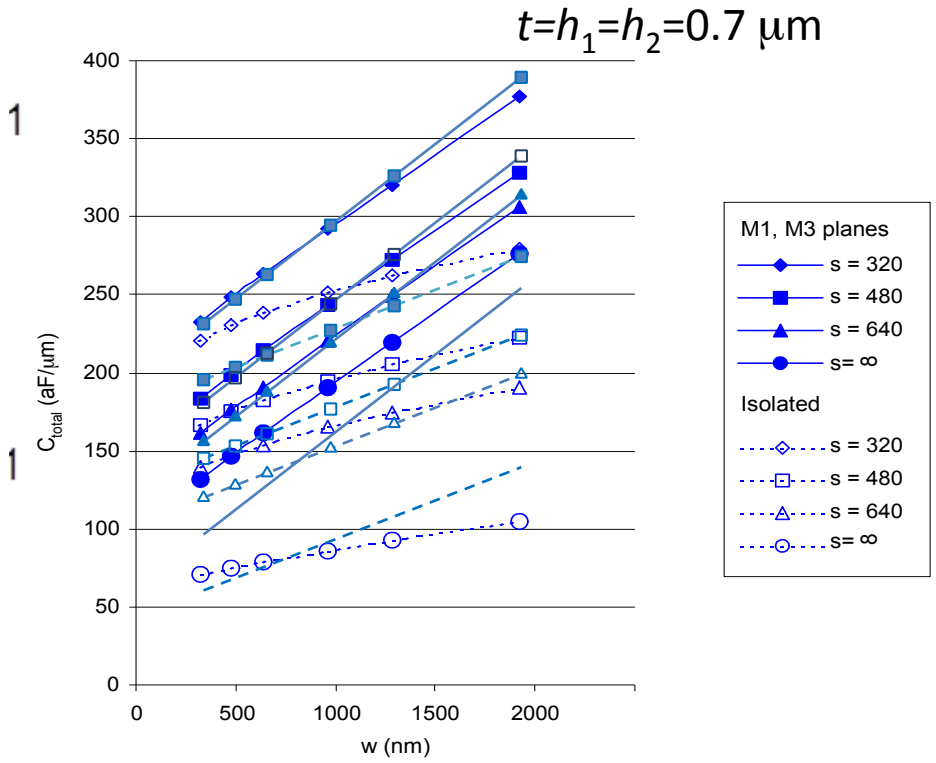


Wire has capacitance *c* per unit length

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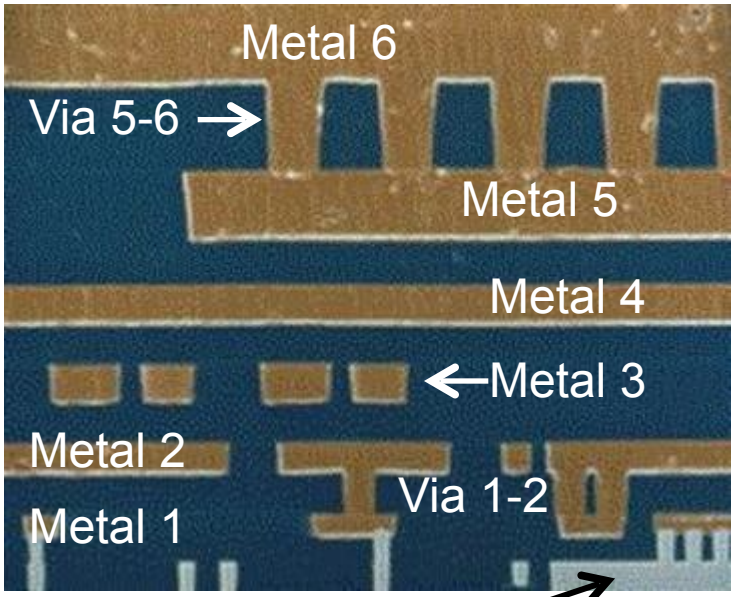
- Wires typically have capacitances about ~ 0.2 fF/μm, i. e. 200 fF/mm
- Compare with the 1.2 fF/μm for the MOSFET gate capacitances

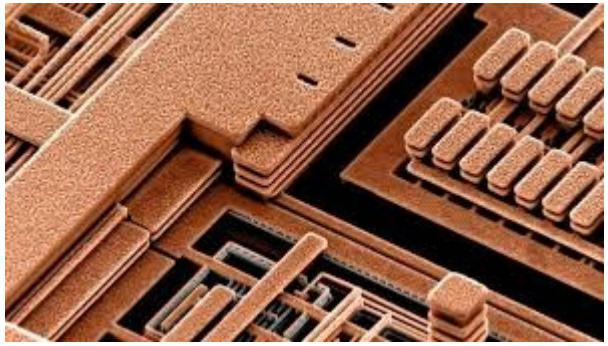
# Wire RC delay

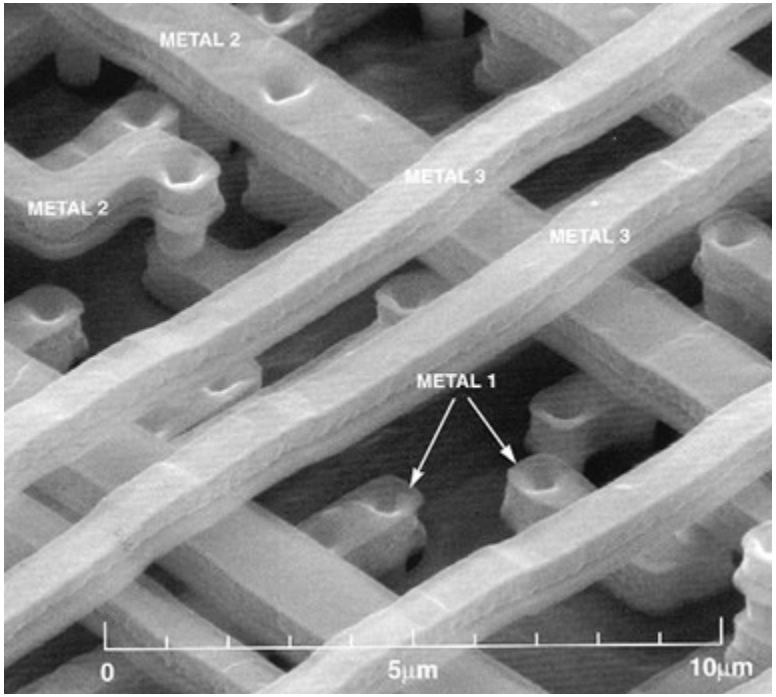
- Wire RC product increases as $L^2$ with wire length $L$
- For our 1 mm example wire, the *RC* product was 160 ps
  - *r* is wire resistance per unit length ~800 Ω/mm (0.8 kΩ /mm)
  - *c* is wire capacitance per unit length ~200 fF/mm
- In comparison, the *RC* time constant of an inverter with a FO4 was previously found to be 36 ps (5×7.2 ps)
  - FO4 delay = 0.7×36 = 25 ps

$$RC = rcL^2$$

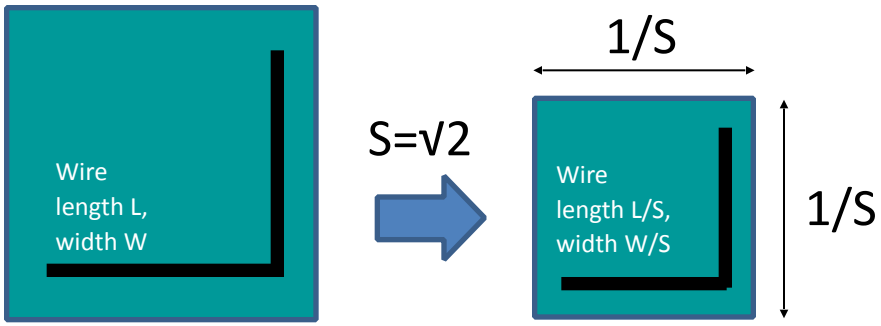
# Modern interconnect





# Wire delay scaling – Local wires




stays constant

$$R = R_S \frac{L/S}{W/S}, \quad R_S = \frac{\rho}{t}$$

- For local wires crossing the same amount of circuitry
  - Resistance stays roughly constant
    - Aspect ratio does not change
    - Sheet resistivity does not change if wire height stays large and/or change material to copper
  - Capacitance decreases by scaling factor
    - Cap/unit length stays constant, while length decreases

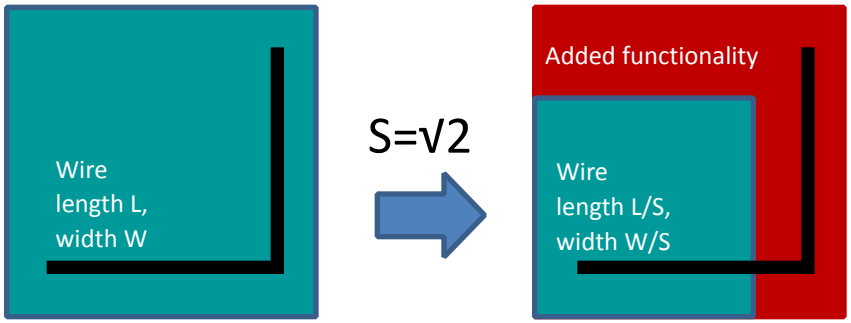
stays constant

$$C = (WC_{ox})L/S$$

- Hence, wire delay tracks gate delay ~1/S

From Mark Horowitz at Design Automation Conference 2000

# Wire delay scaling – Global wires




stays constant

$$R = R_S \frac{L}{W/S} \sim S$$

- For global wires crossing the whole chip
  - Resistance grows linearly (with scaling factor)
  - Capacitance stays fixed
    - Cap/unit length stays constant, as does wire length

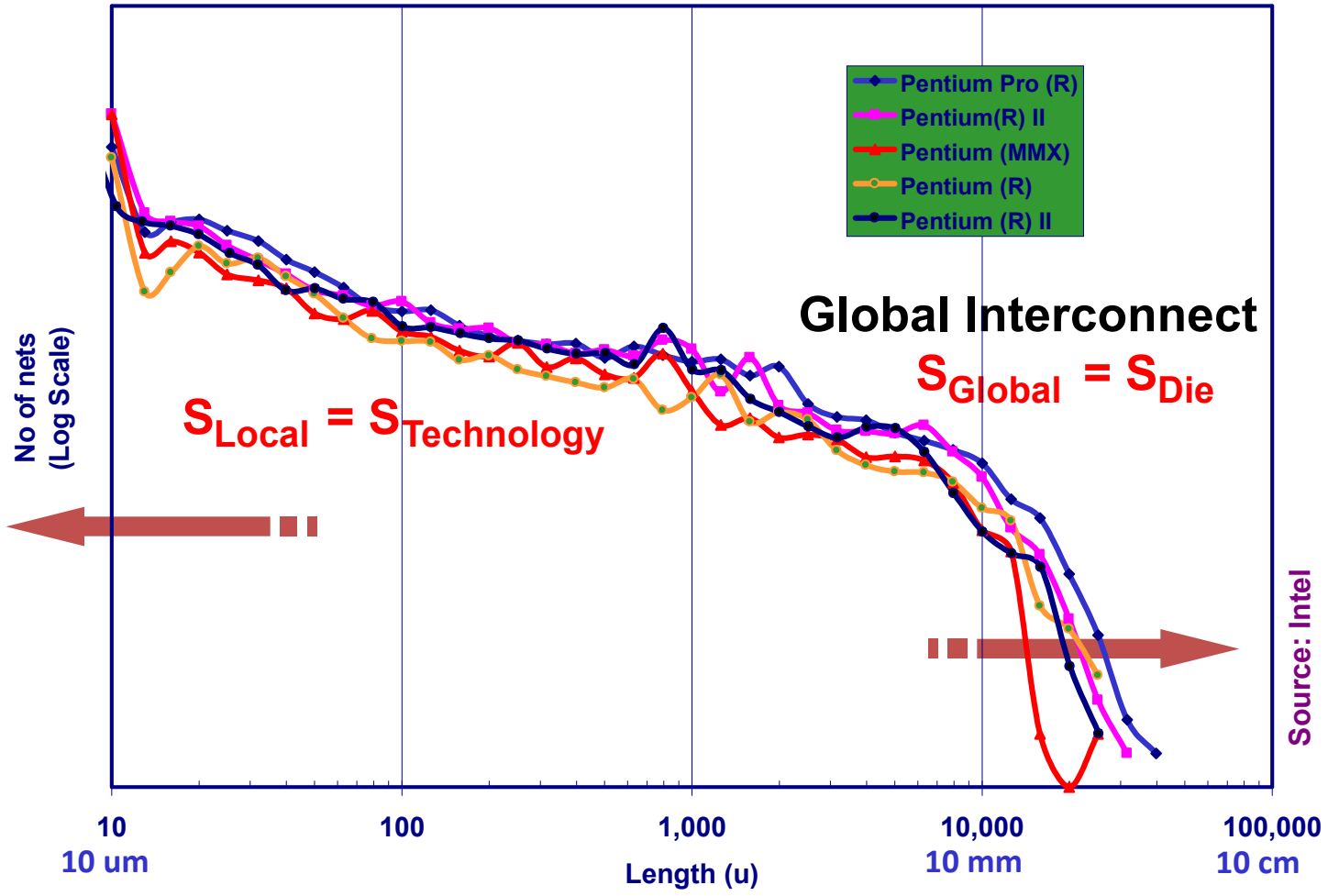
stays constant

$$C = (WC_{ox})L$$

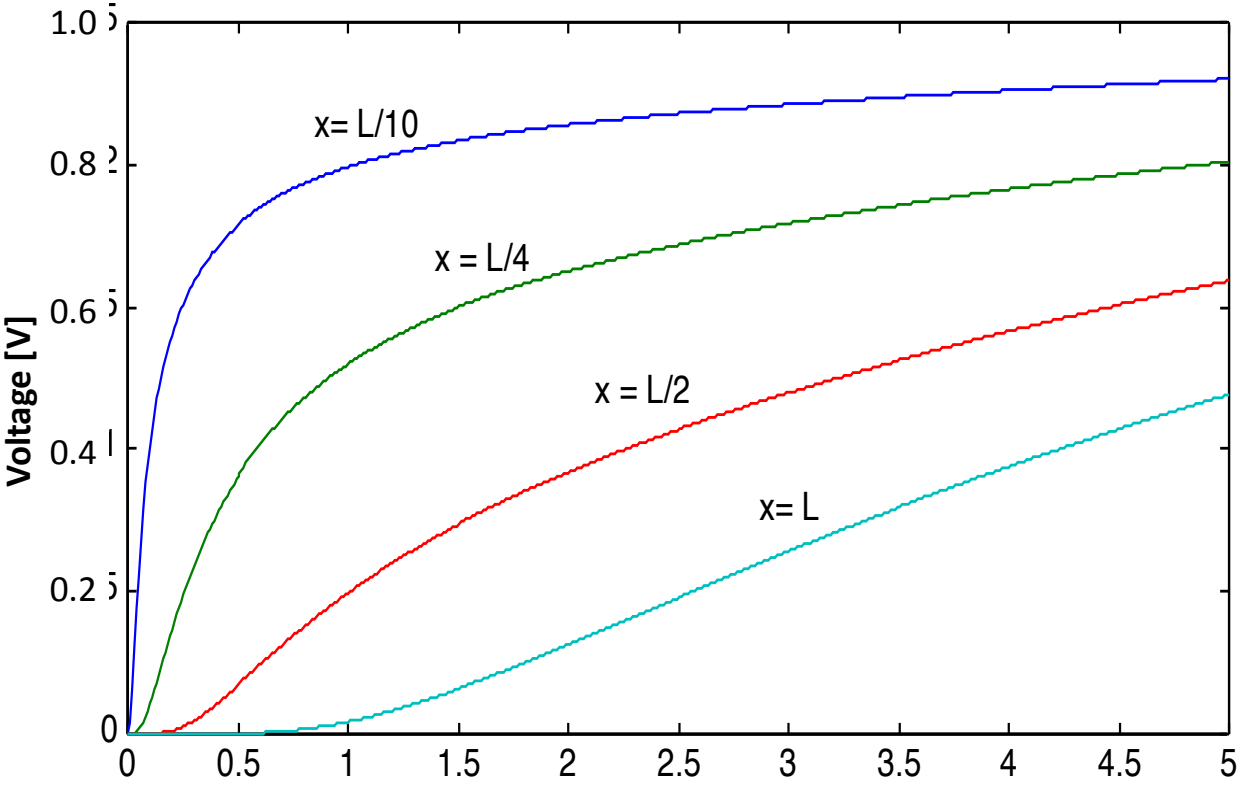
- Two opposite trends:
  - Wire delay increases (~S ) - gate delay decreases (~1/S)

From Mark Horowitz at Design Automation Conference 2000

# Modern Interconnect



# Step-response to a rising input voltage along an RC wire as a function of time and wire length



# Summary

We have

- discussed the importance of accurate wire modeling considering not only wire capacitance but also wire resistance as wires get longer and skinnier
- defined the concept of sheet resistance in ohms per square
- had a look at typical on-chip wire length distributions
- had a look at wire capacitance dependence on the surrounding wiring on top, below, and along sidewalls

# Introduction to on-chip interconnect

Wire delay modeling and repeater insertion

Lecture 7 continued

Tuesday October 2, 2018

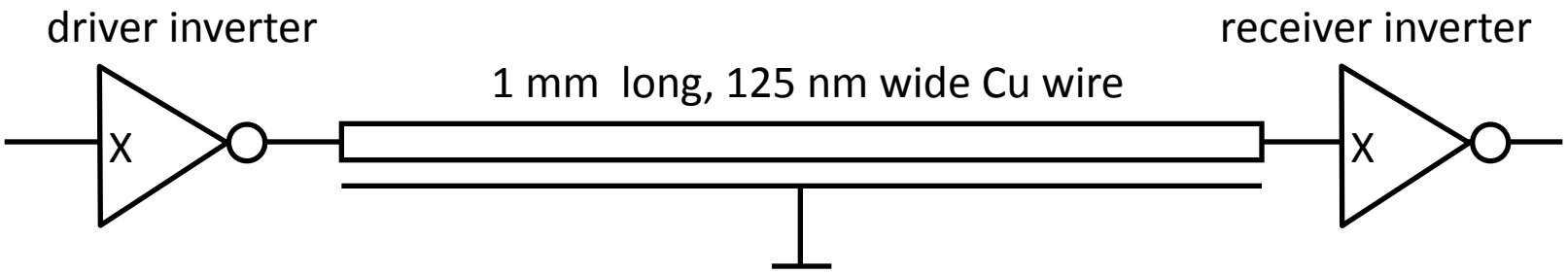
# Outline

- Introduction
- Introduce a distributed RC π-model for delay estimates
  - Wire resistance per unit length *L*, *r*
  - Wire capacitance per unit length *L*, *c*
  - Distributed wire delay ~ ½$rcL^2$
- For simplicity, assume the existence of a dominant RC time constant for describing the output signal at the wire end
- We will show how repeaters can be inserted to keep wire lengths short
  - Find the optimal number of repeaters for any wire length
  - Find the critical wire length for repeater insertion
- Introduce the concept of wire effort
- Conclusions

# Wire delay example

Estimate the delay of an inverter driving an identical inverter at the end of the 1 mm wire! $W_P=2W_N$.

Assume wire cap $c$= 200 fF/mm, $r$=800 Ω/mm (from previous examples)



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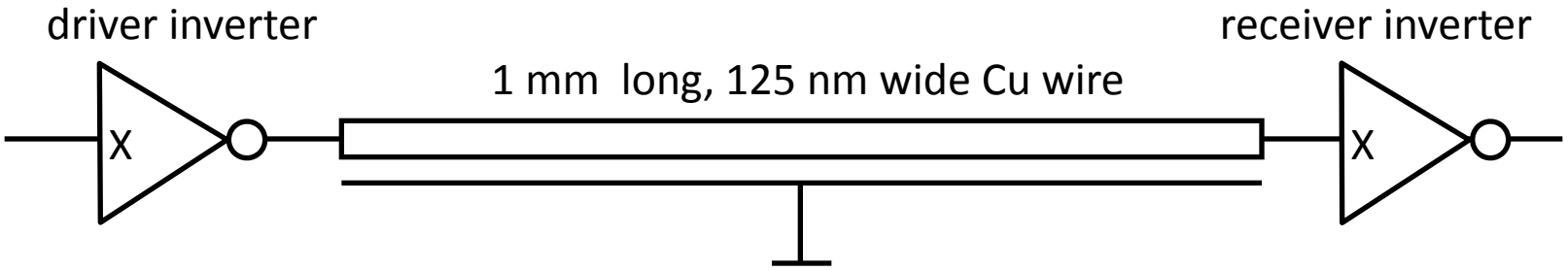

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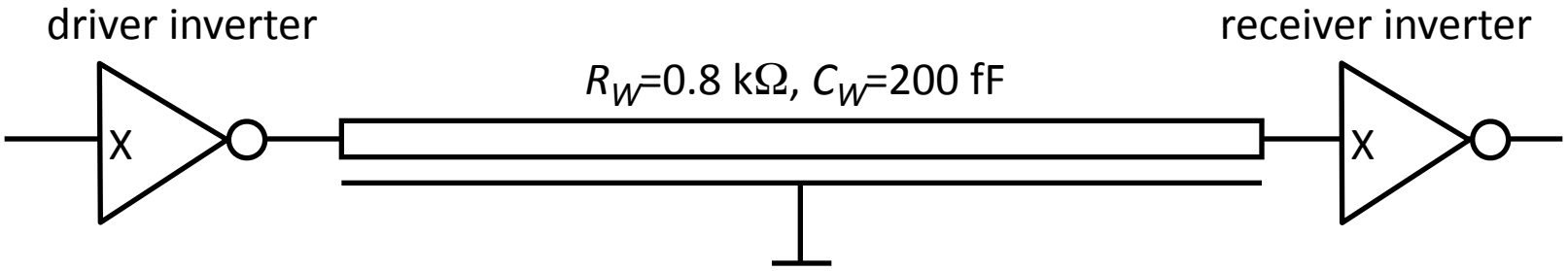


The given parameters yield a wire resistance of 800 Ω and a wire cap is 200 fF.

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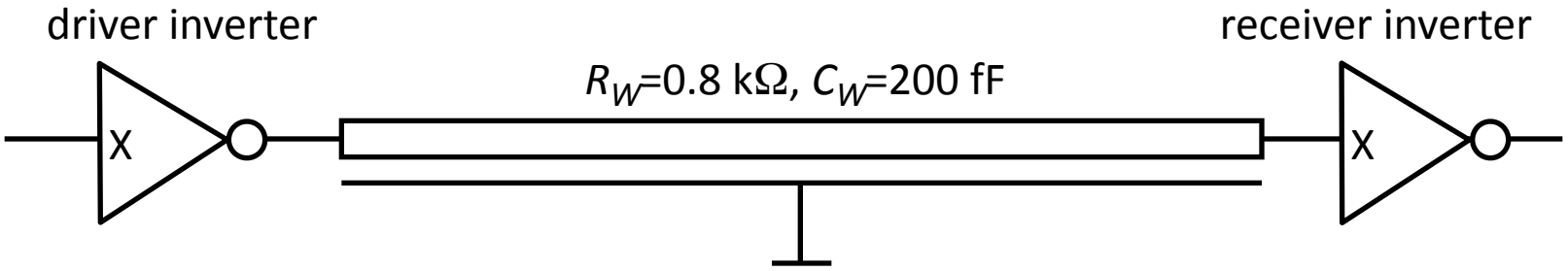


Hence, wire $R_WC_W$ product is 160 ps

The contribution to the system time constant from the distributed wire is ½$R_WC_W$= 80 ps

Increasing the time constant from the 14.4 ps with no or a short wire to almost 95 ps.

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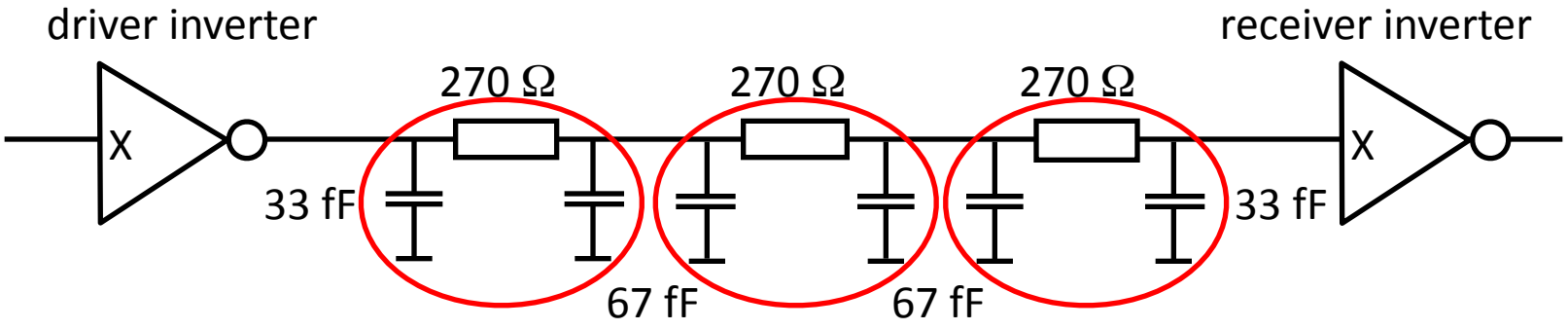


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In Spice circuit simulations a 3-segment π-model is accurate to within 3%

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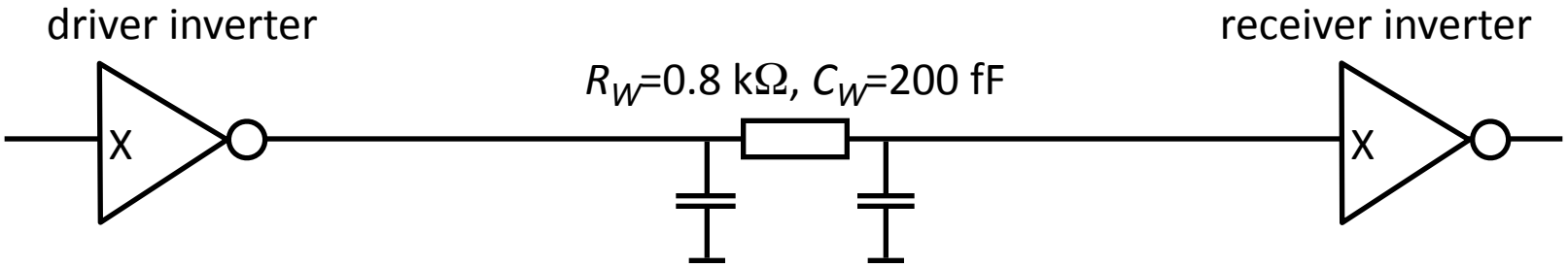


Wire resistance is distributed along the wire which must be modeled by segments
In Spice circuit simulations a 3-segment π-model is accurate to within 3%
However, for simple analytical estimate: use single segment π-model.

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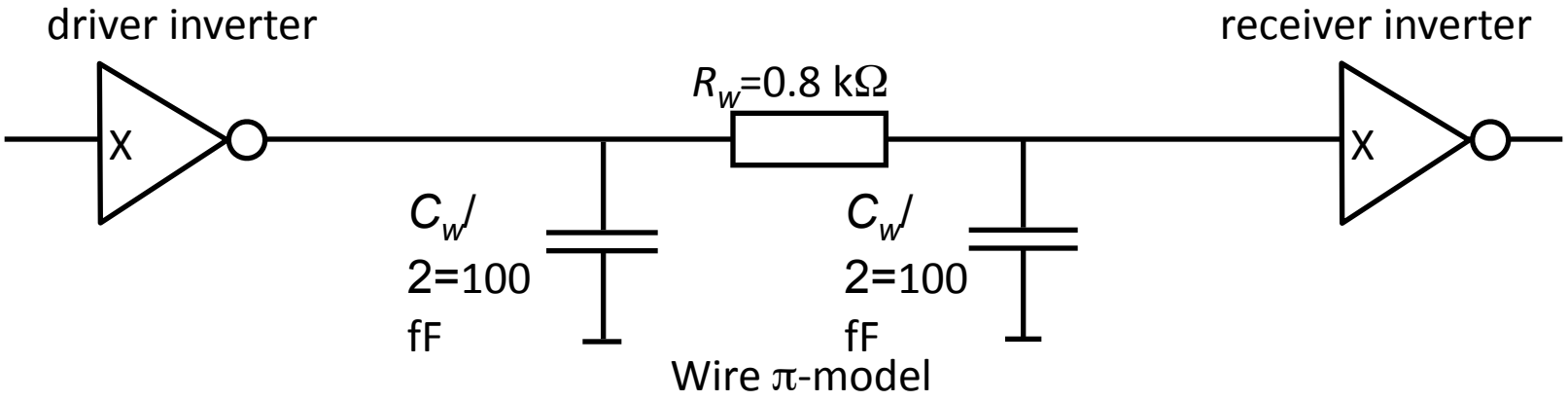

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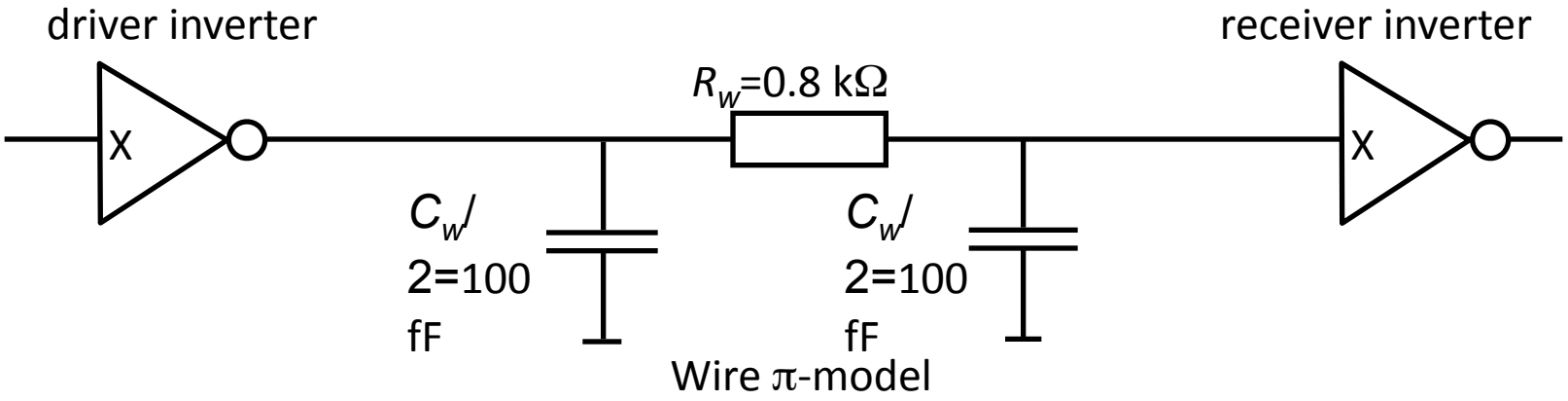


Wire π-model

Introduce electrical inverter models

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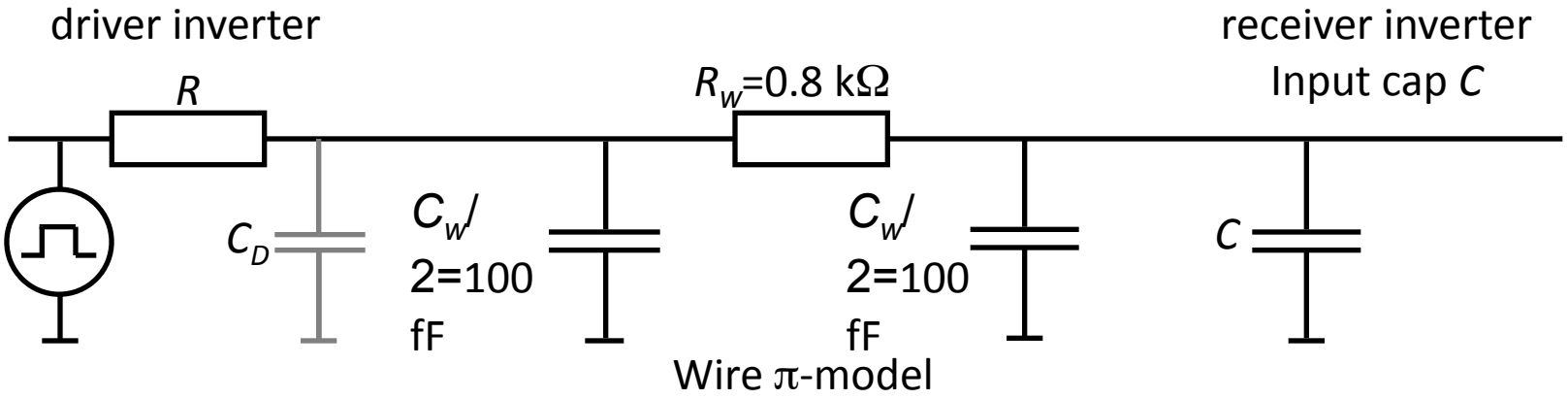


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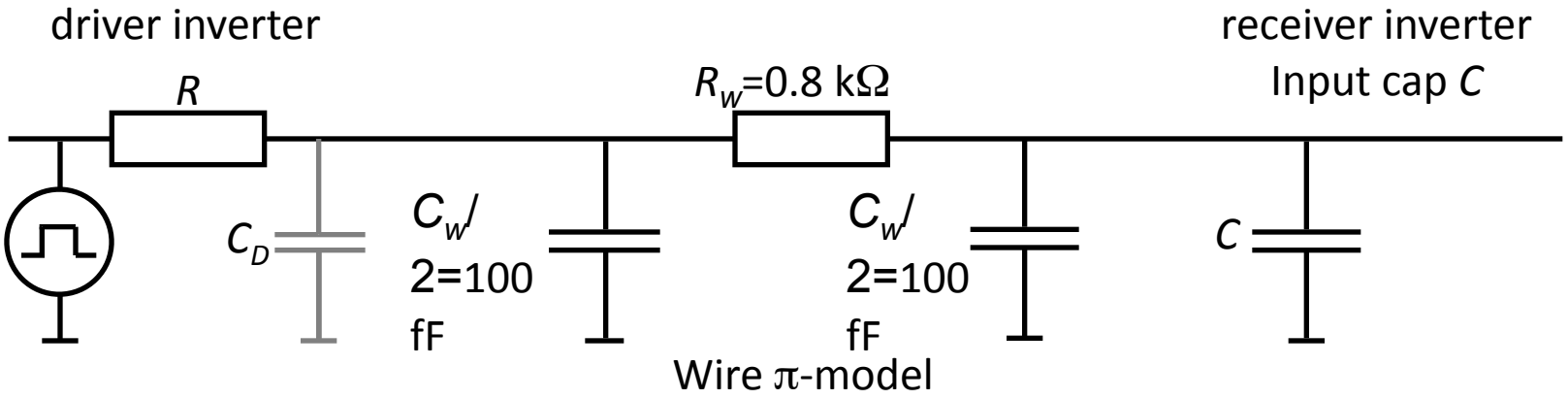



Wire π-model

Introduce electrical inverter models

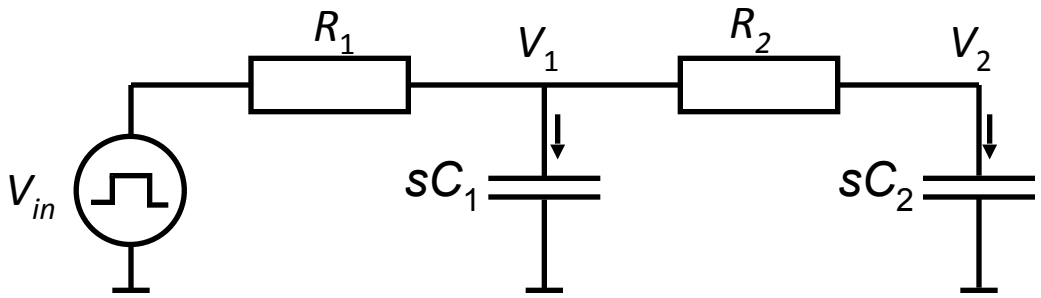
What is the delay of this two-stage RC circuit?

Can be found analytically from second-order differential equation!

# Simplify wire circuit to find solution

Redraw the wire circuit as a two-stage RC circuit, where

- Stage 1: resistance $R_1$ and capacitance $C_1$
- Stage 2: resistance $R_2$ and capacitance $C_2$



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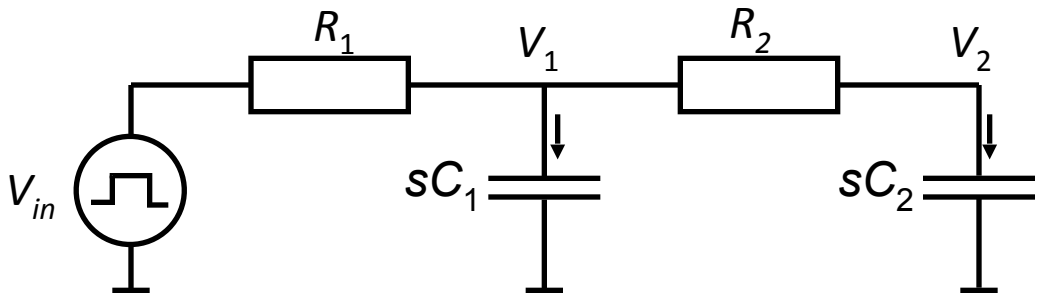
- Get transfer function, or 2nd order linear differential equation




$$H(s) = \frac{1}{R_1 R_2 C_1 C_2 s^2 + \left(R_1 (C_1 + C_2) + R_2 C_2\right) s + 1}$$

Second order linear differential equation

$$R_1 R_2 C_1 C_2 V_2^{(2)} + \left(R_1 (C_1 + C_2) + R_2 C_2\right) V_2' + V_2 = 0$$

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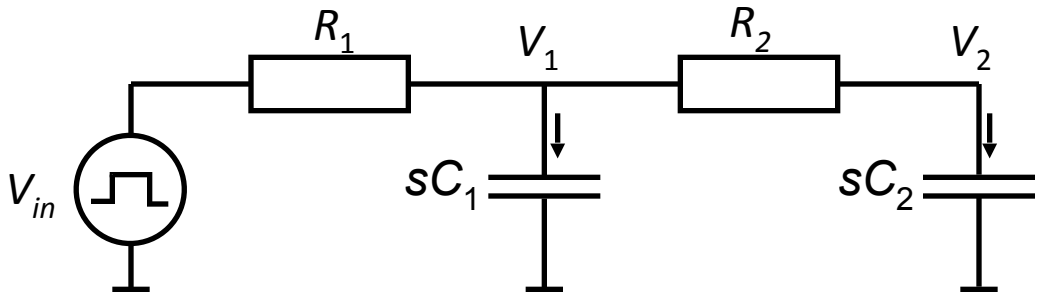


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Characteristic eq. yields exponential time constants

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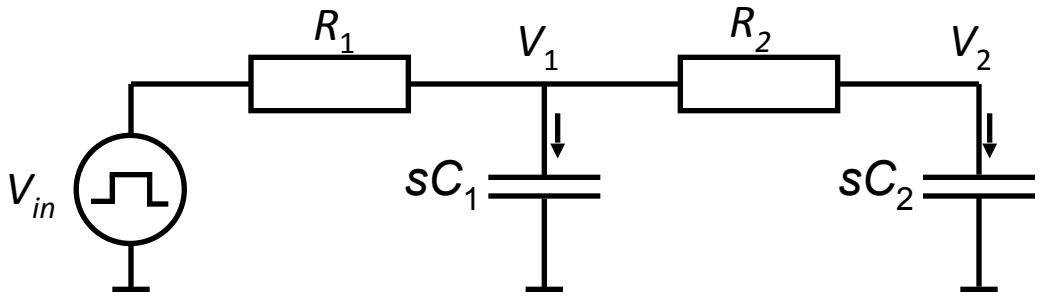


Let´s denote the two solutions to the characteristic equation $s_1$ and $s_2$, respectively.

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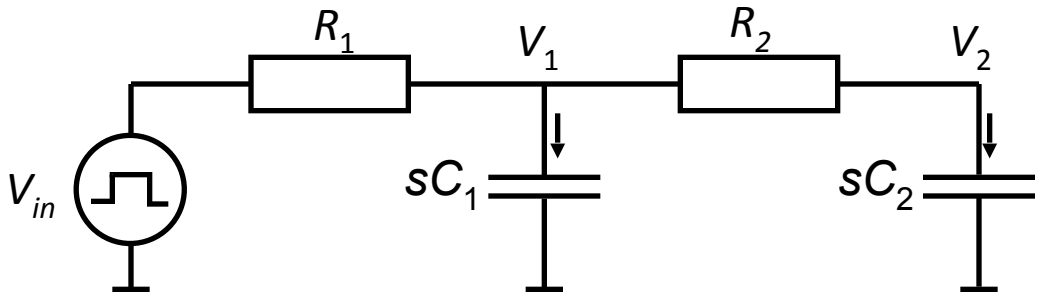


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For the case of a falling output the solution is:

$$V_2(t) = V_{21}e^{s_1 t} + V_{22}e^{s_2 t}$$

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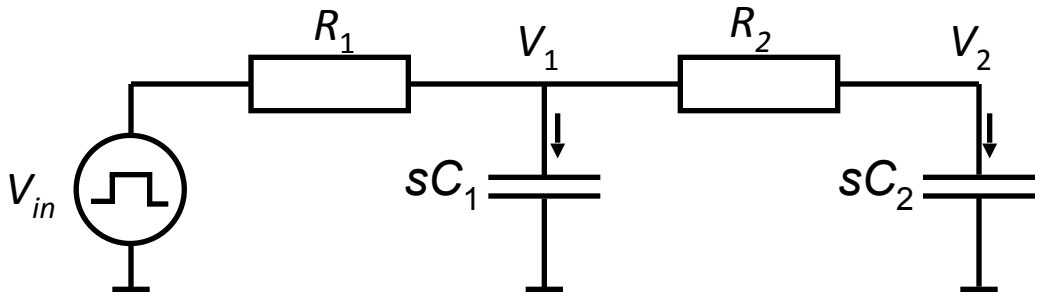


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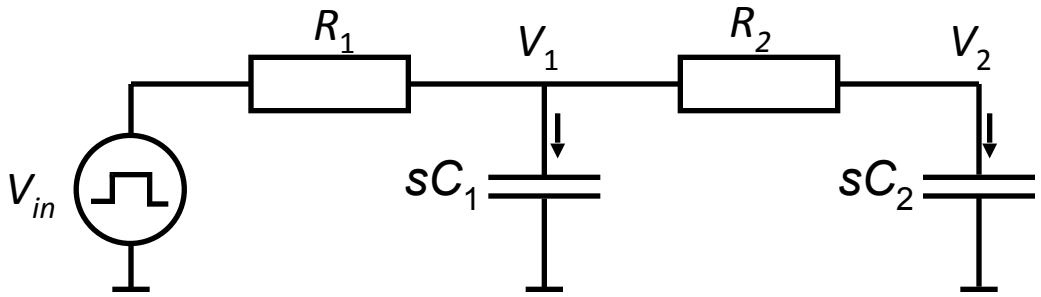


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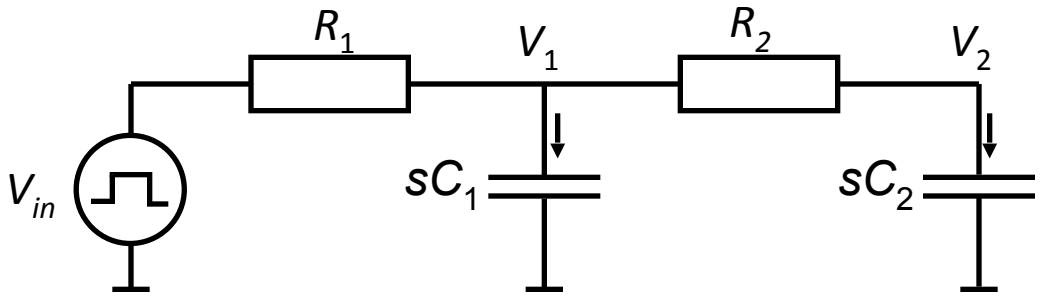


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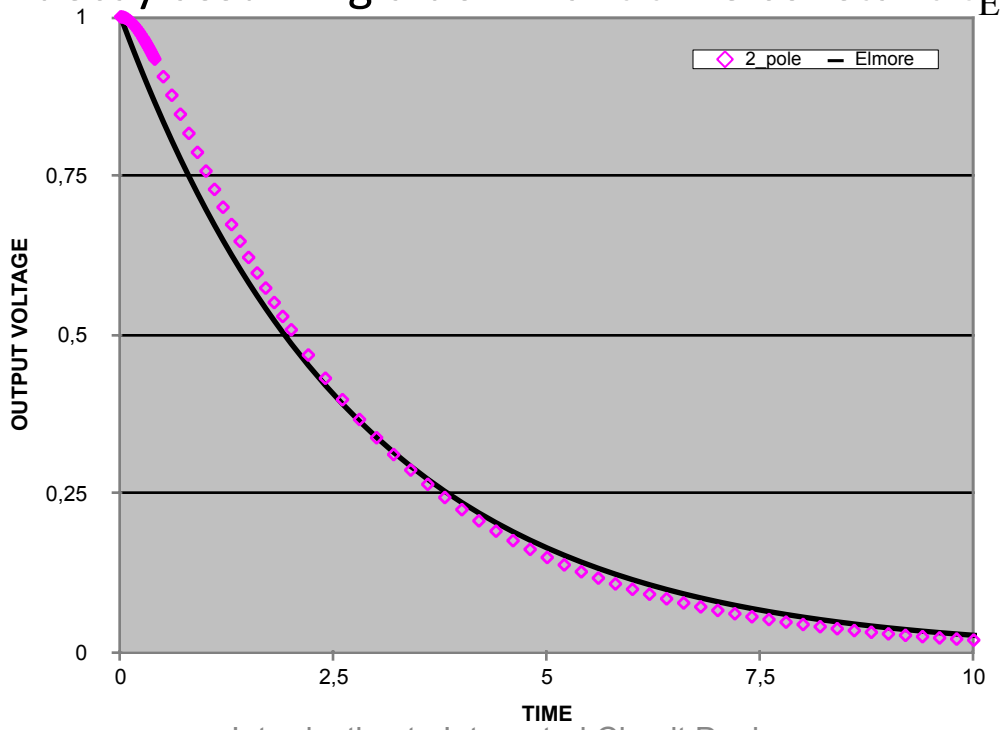
Propagation delay: $t_D = 0.7 \times \tau_E$

# Approximative solution

Let´s have a look at a circuit example where $R_1$=0.8$R_2$, $C_1$=1.2$C_2$

Already for these 20% differences between $R_1$ and $R_2$, $C_1$ and $C_2$, respectively, one of the time constants become dominant, i. e. $\tau_1$=2.45, $\tau_2$=0.3

This graph compares the exact two-pole solution with the approximative exponential decay assuming a dominant time constant $\tau_E=\tau_1+\tau_2=2.75$



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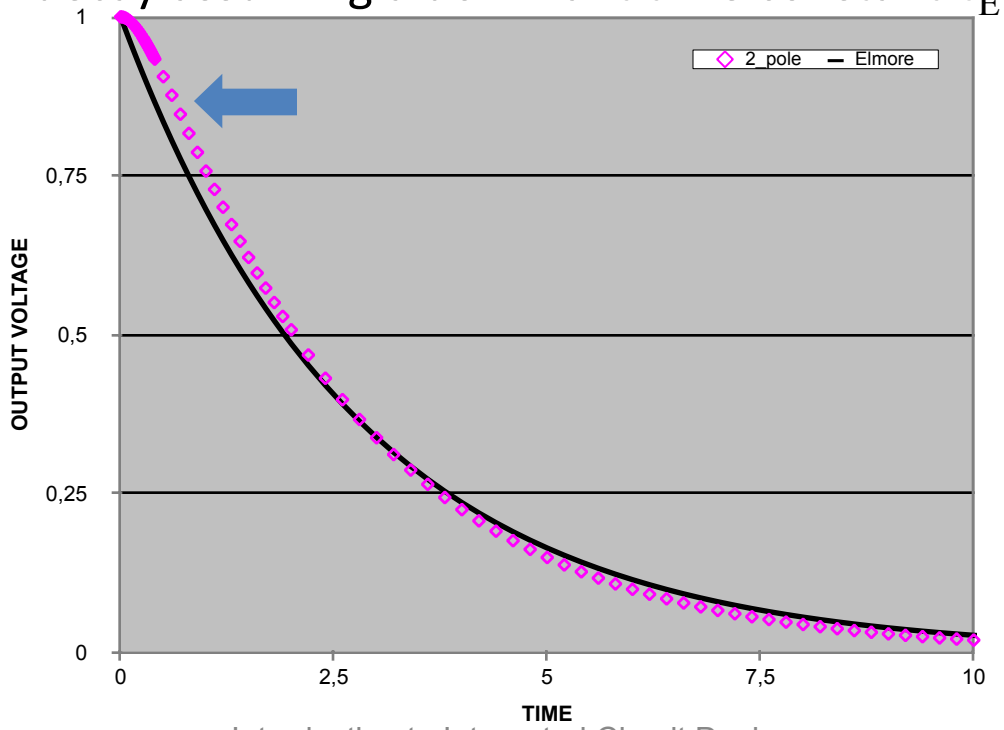

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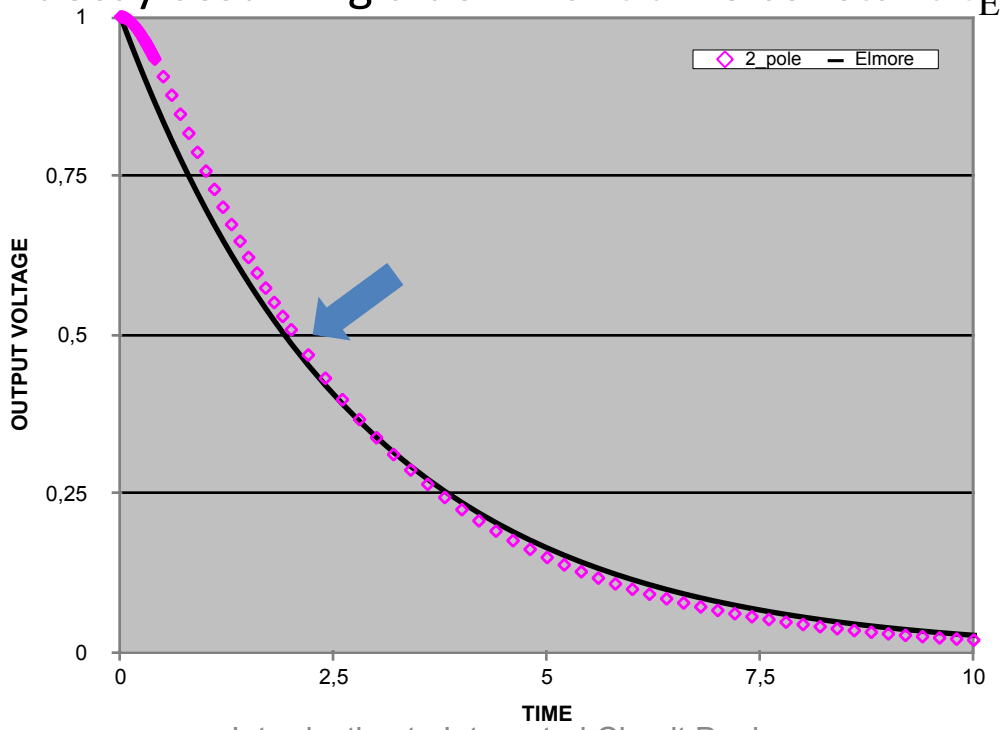

# How to remember delay formula?

Estimate the delay of an inverter driving an identical inverter at the end of the 1 mm wire! $W_P=2W_N$.

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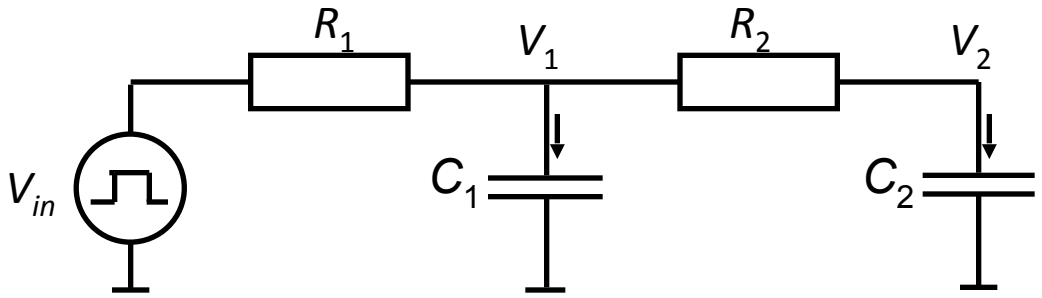
- Now, let us return to the simplified two-stage RC circuit
- How to remember how to get the dominant time constant?



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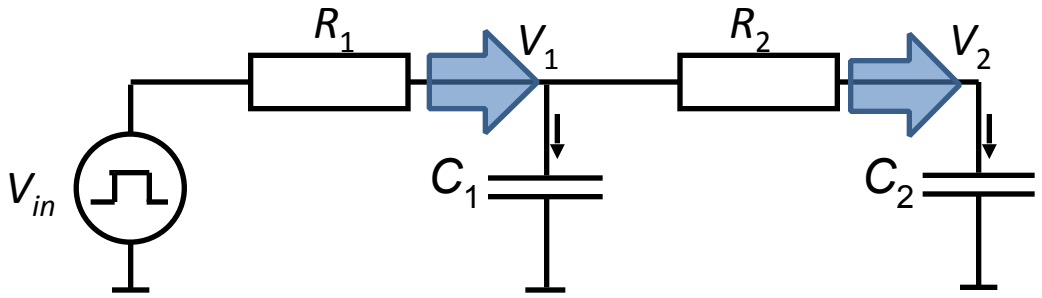


Each resistance is multiplied by its downstream capacitance!

$$T_E = R_1\left(C_1 + C_2\right) + R_2 C_2$$

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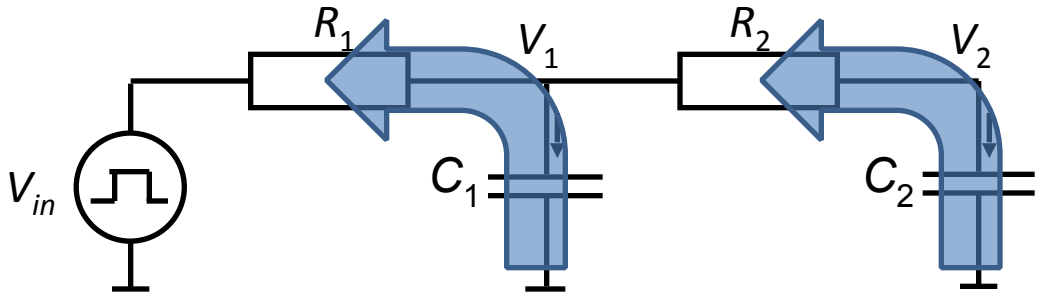
- Now, let us return to the simplified two-stage RC circuit
- How to remember how to get the dominant time constant?




Or: Each capacitance is multiplied by its upstream resistance!

$$T_E = R_1C_1 + (R_1 + R_2)C_2$$

# Return to wire delay example

Estimate the delay of an inverter driving an identical inverter at the end of the 1 mm wire! $W_P=2W_N$.

Assume wire cap $c$= 200 fF/mm, $r$=800 Ω/mm (from previous examples)

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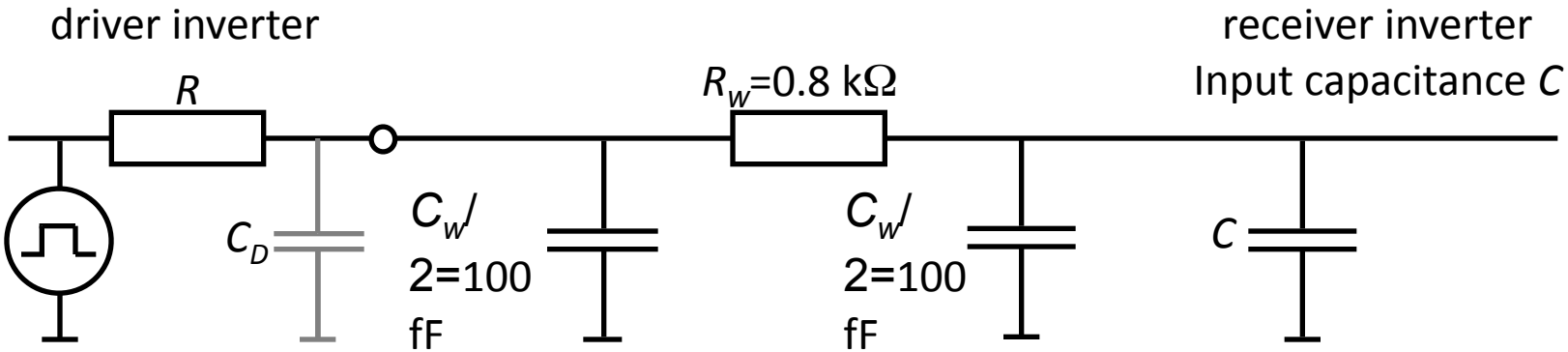
The wire will affect the propagation delay if wire RC product $R_WC_W$ is larger than the well-known inverter RC product $R_{eff}C_G$=2 kΩ × 3.6 fF = 7.2 ps.



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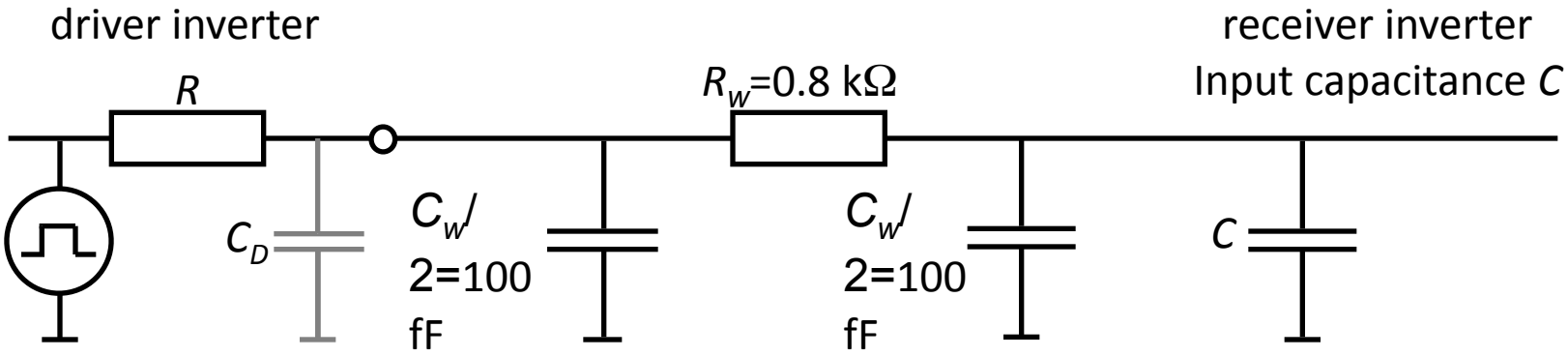


Dominating delay time constant becomes: $T_E = R\left(C_D + C + C_w\right) + R_w\left(C + \frac{C_w}{2}\right)$

# Return to wire delay example

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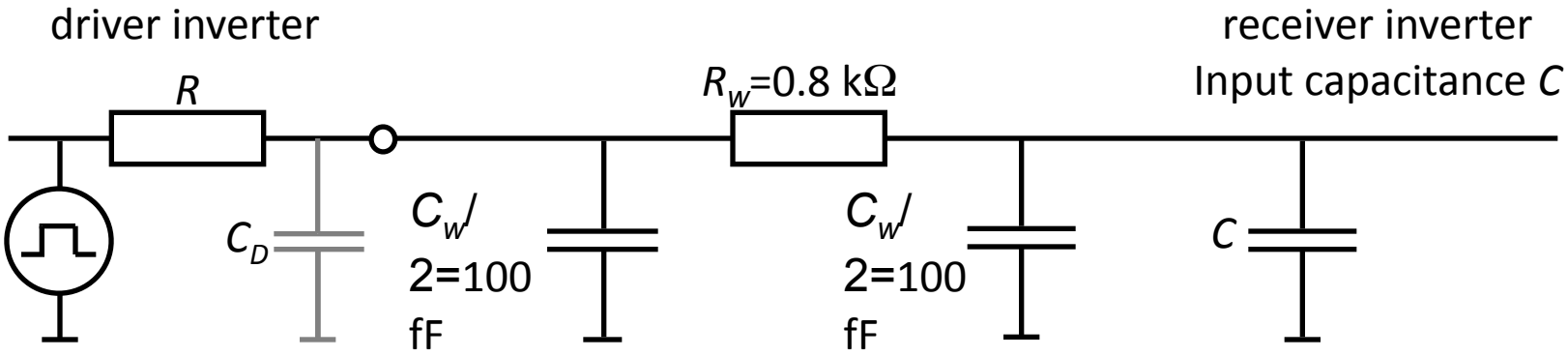


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$$T_E = \underbrace{R\left(C_D + C\right)}_{=2\times 7.2\text{ ps if } p_{inv}=1} + \underbrace{RC_w}_{R \text{ is unknown}} + \underbrace{R_w C}_{C \text{ is unknown}} + \underbrace{\frac{R_w C_w}{2}}_{80\text{ ps}} \geq 94.4\text{ ps}$$

# Return to wire delay example

Estimate the delay of an inverter driving an identical inverter at the end of the 1 mm wire! $W_P=2W_N$.

Assume wire cap $c$= 200 fF/mm, $r$=800 Ω/mm (from previous examples)

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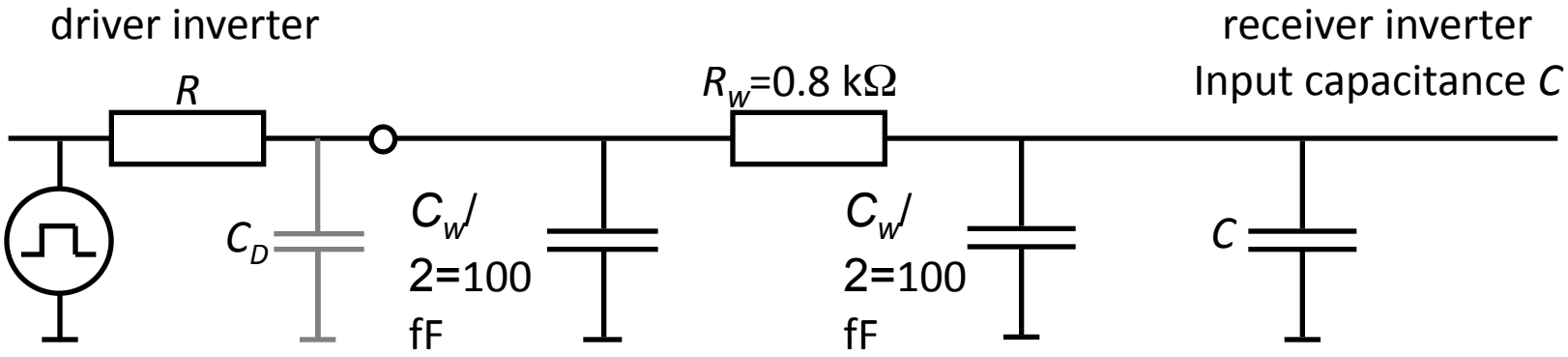


Dominating time constant $T_E$ can be normalized wrt technology time constant $RC$!

$$d = \frac{T_E}{\underbrace{RC}_{inverter}} = p_{inv} + 1 + \frac{R_WC_W}{RC}\frac{R}{R_W} + \frac{R_W}{R} + \frac{R_WC_W}{2RC}$$

# Return to wire delay example

Estimate the delay of an inverter driving an identical inverter at the end of the 1 mm wire! $W_P=2W_N$.

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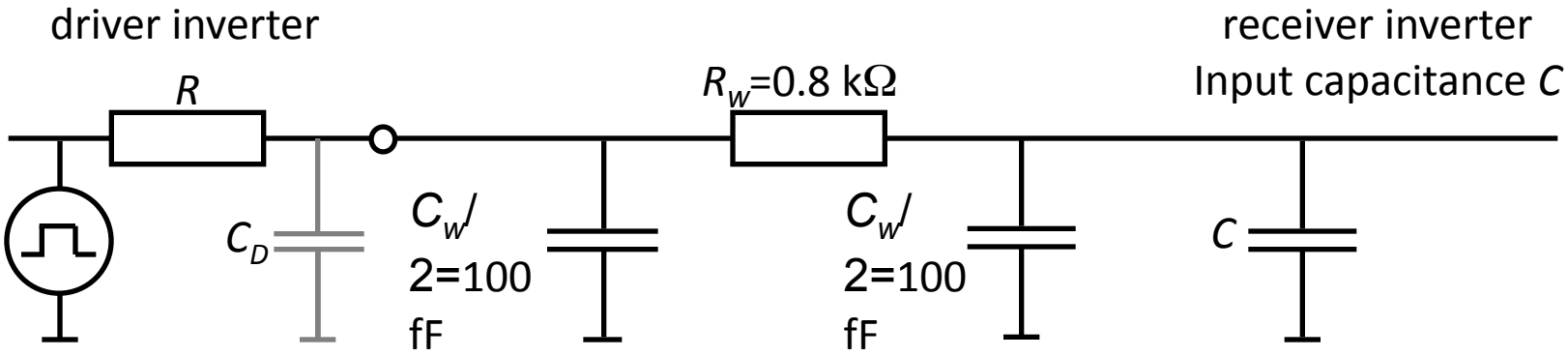


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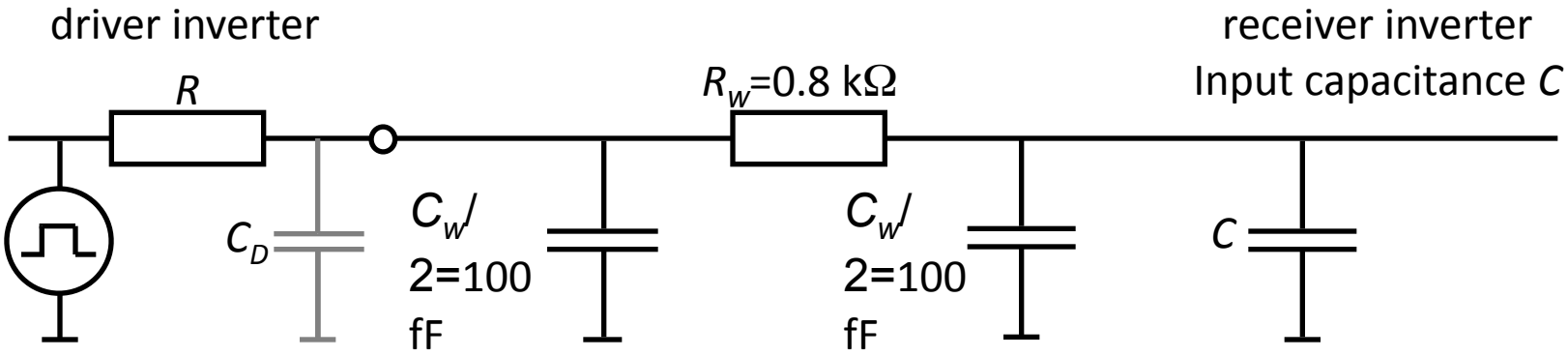


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In our example, $W_E$=160/7.2≈22

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Estimate the delay of an inverter driving an identical inverter at the end of the 1 mm wire! $W_P=2W_N$.

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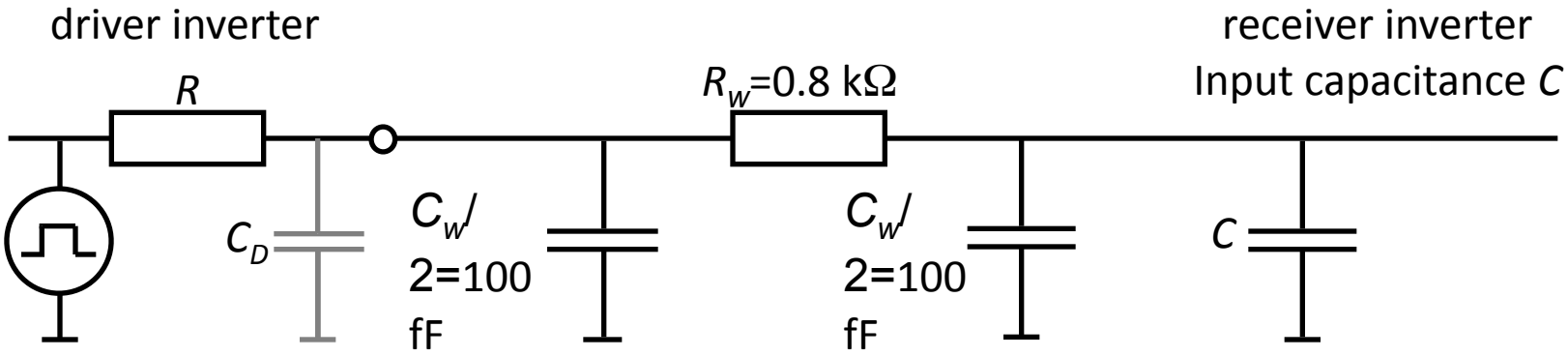


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and the normalized delay can be written $d = p_{inv} + 1 + W_E \frac{R}{R_W} + \frac{R_W}{R} + \frac{W_E}{2}$

# Return to wire delay example

Estimate the delay of an inverter driving an identical inverter at the end of the 1 mm wire! $W_P=2W_N$.

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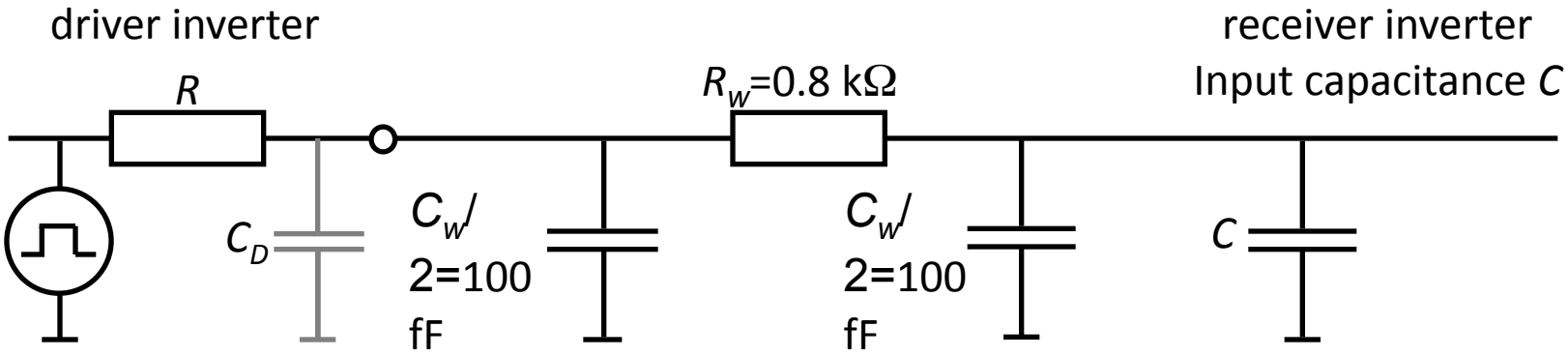


Having developed a delay model based on the assumption of a dominating time constant, let´s apply the model for finding the size of the inverter minimizing the delay!

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Estimate the delay of an inverter driving an identical inverter at the end of the 1 mm wire! $W_P=2W_N$.

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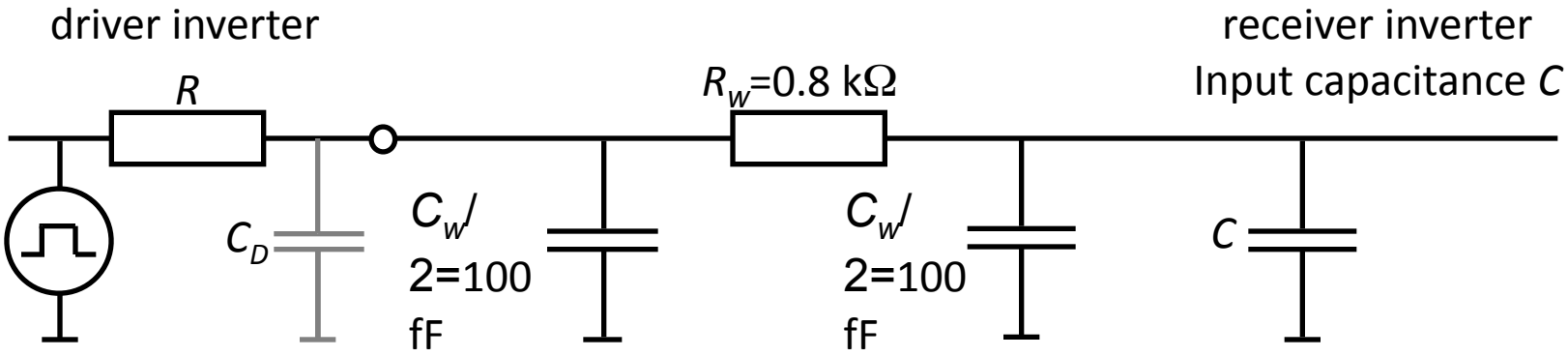


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$$\frac{\partial d}{\partial R}=\frac{W_E}{R_W}-\frac{R_W}{R^2}=0 \rightarrow R_{optimal}=\frac{R_W}{\sqrt{W_E}};\ R_W=0.8\ \text{k}\quad W_E= \quad \rightarrow R_{optimal}=$$

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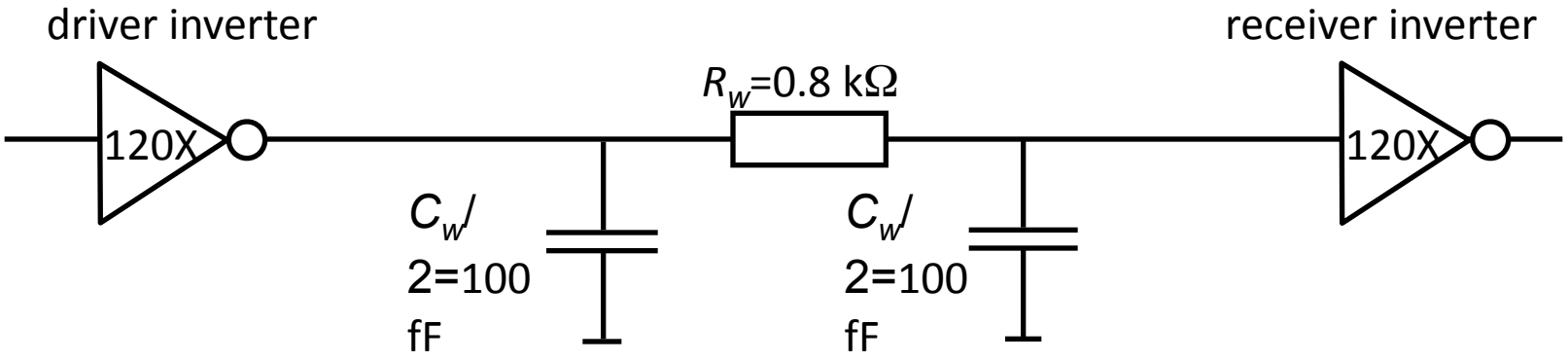


Having defined inverter size 10X for inverters with $R$=2 kΩ, 120X is the inverter size with $R_{eff}$=170 Ω minimizing the delay caused by the wire.

Assuming $p_{inv}=1$, and having $W_E$=22, we obtain $d_{\min}=\underbrace{2}_{p_{inv}=1}+2\sqrt{W_E}+\frac{W_E}{2}=22.5$

# Return to wire delay example

Estimate the delay of an inverter driving an identical inverter at the end of the 1 mm wire! $W_P=2W_N$.

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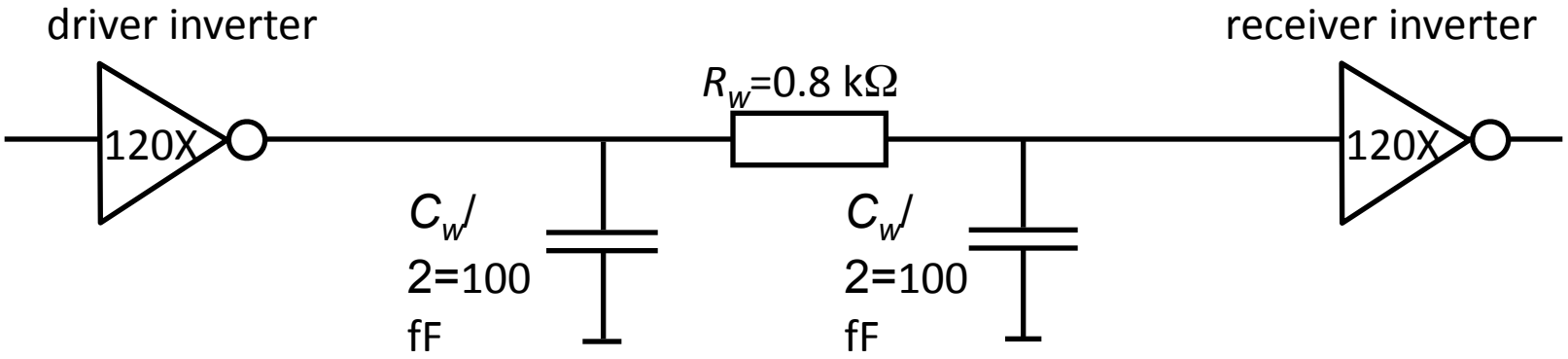


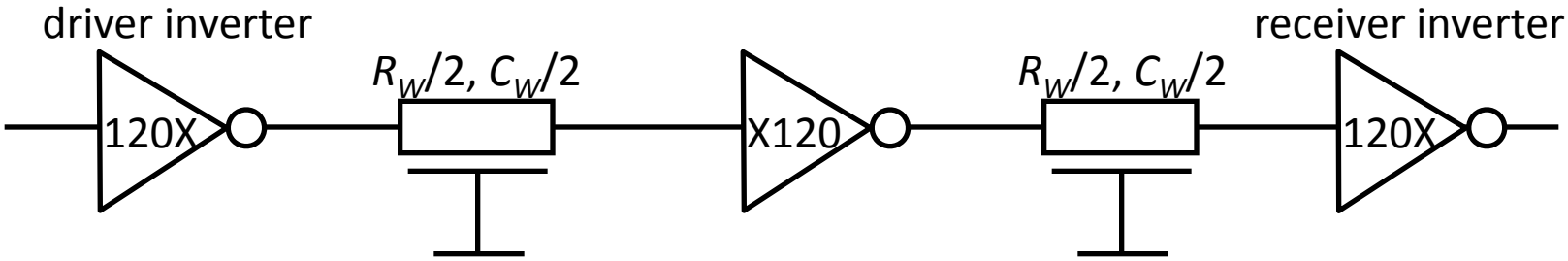

Having defined inverter size 10X for inverters with $R$=2 kΩ, 120X is the inverter size with $R_{eff}$=170 Ω minimizing the delay caused by the wire.

Total delay becomes 22.5 multiples of the basic 5 ps that we have defined for the 65 nm CMOS process, i.e. 112.5 ps, a value to be compared to the 10 ps with no wire.

# Keeping wires short using repeaters

For keeping wires short, what if we divide the wire in the example into 2 segments by inserting a repeater in the middle?

A repeater is just an identical inverter that we call repeater!
To estimate the propagation delay, just add the two segment delays!



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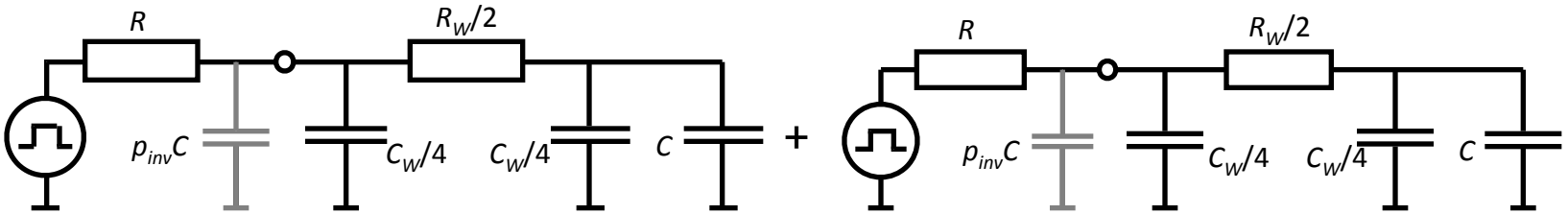

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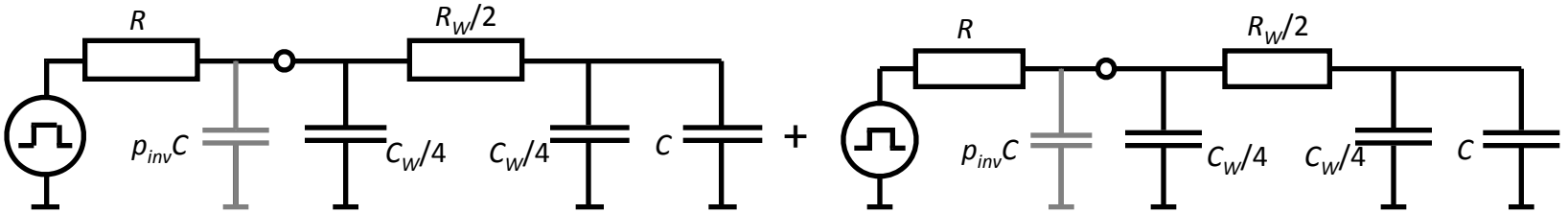


If we keep the total wire effort $W_E$=22, the sum of the two stage delays is

$$d = 2 \times \left( \underbrace{p_{inv} + 1}_{} + \frac{W_E}{4} \frac{R}{R_W/2} + \frac{R_W/2}{R} + \frac{W_E/4}{2} \right)$$ (Using delay Eq. on slide 27)

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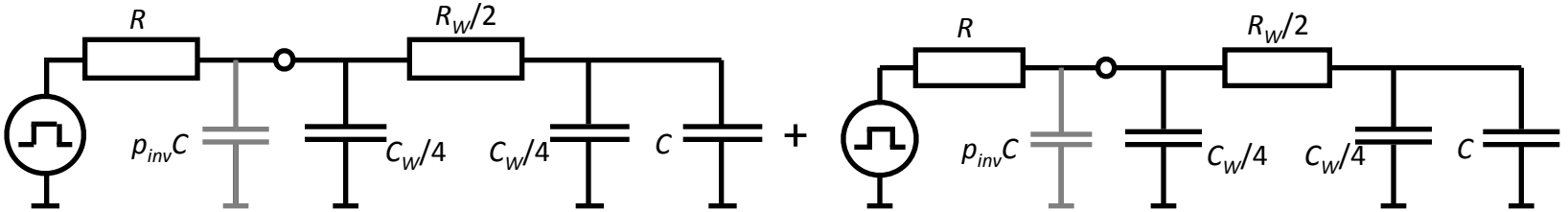


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Keeping $R_{eff} = R_{opt} = \frac{R_W}{\sqrt{W_E}}$ ➡ $d_{\min} = 2\times\left(2+\sqrt{W_E}+\frac{W_E}{8}\right) = 2\times(2+2.35+2.35+2.8) = 19$

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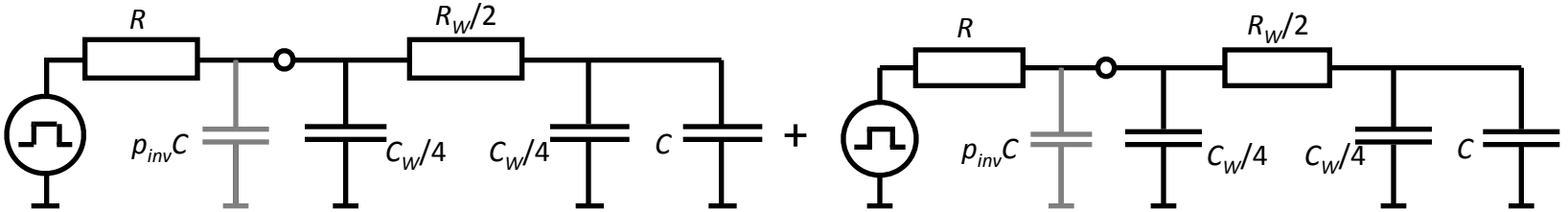


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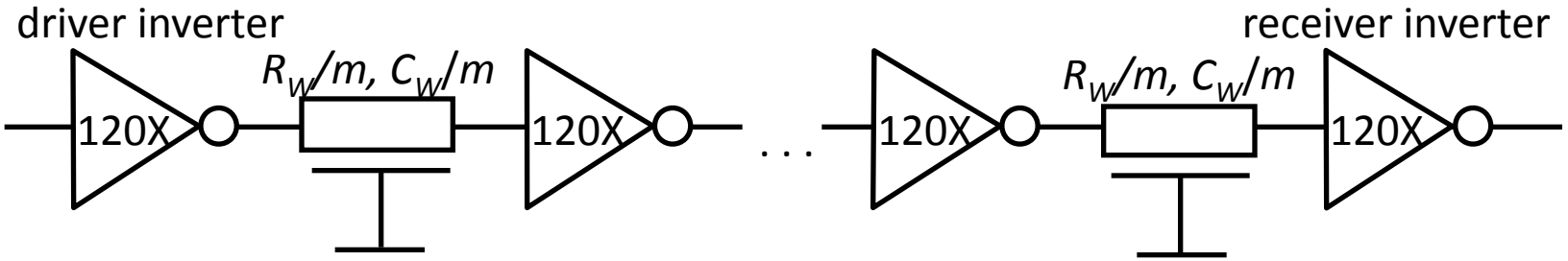
Just a small decrease of the wire delay (from 22.5 to 19)! But still . . .

# Keeping wires short using repeaters

But what if the wire is much longer, say 10-15 mm?

What would be the optimal number of segments, *m,* into which the wire should be split by inserting *m*-1 identical repeaters for minimizing the delay?



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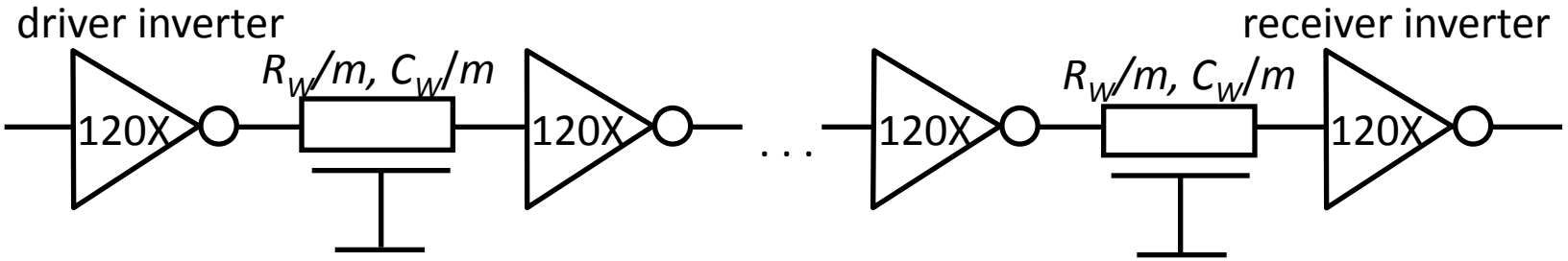


If we keep $W_E$ as the total wire effort, the delay can be written

$$d = m \times \left( \underbrace{p_{inv} + 1}_{} + \frac{W_E}{m^2} \frac{R}{R_W/m} + \frac{R_W/m}{R} + \frac{W_E}{2m^2} \right) \Rightarrow m_{opt} = \sqrt{\frac{W_E}{2\left(p_{inv}+1\right)}} = \underbrace{\frac{\sqrt{W_E}}{2}}_{p_{inv}=1}$$

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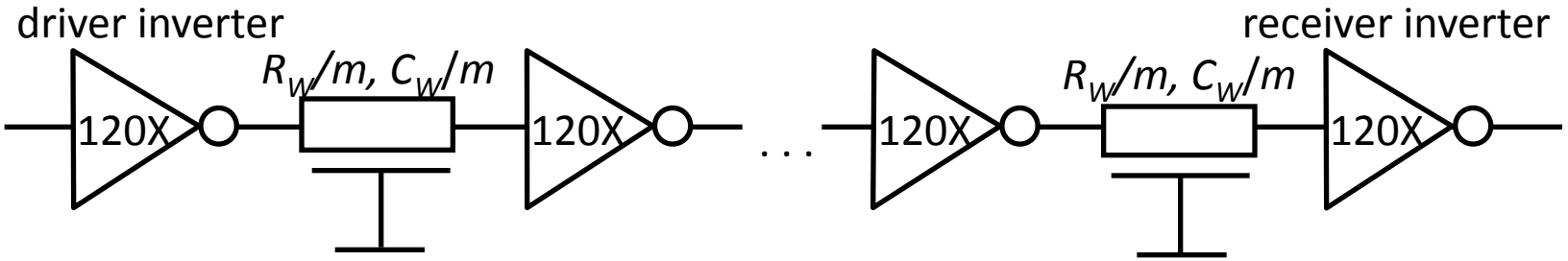


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The previous inverter sizing is still optimal, since the two middle terms yielding the relationship between $R$ and $R_w$ are independent of $m$!

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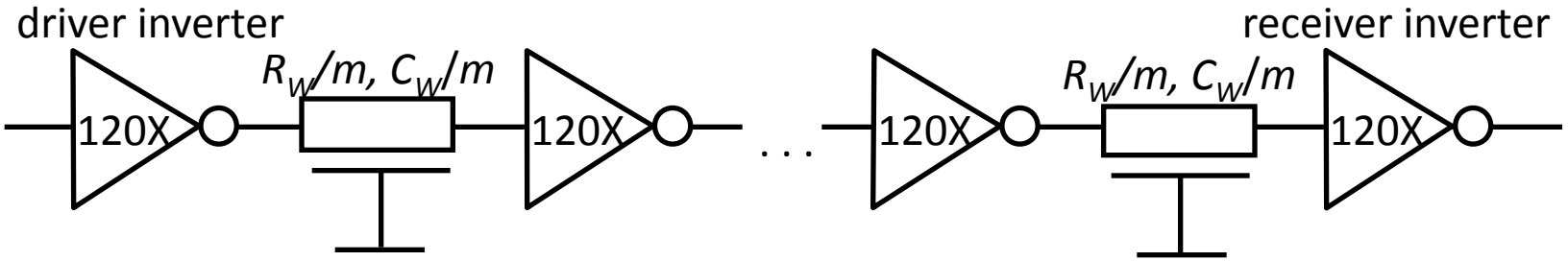


What is the critical wire length for considering repeater insertion?

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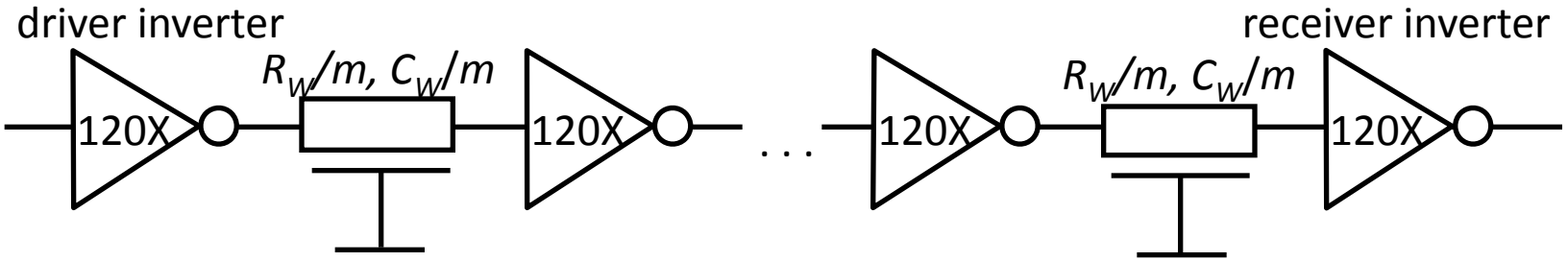


What is the critical wire length for considering repeater insertion?

$$L_{crit} = \frac{L}{m_{opt}} = \frac{2L}{\sqrt{W_E}} = 2\sqrt{\frac{RC}{rc}} = 2\sqrt{\frac{7.2}{160}} = 0.42 \text{ mm}$$

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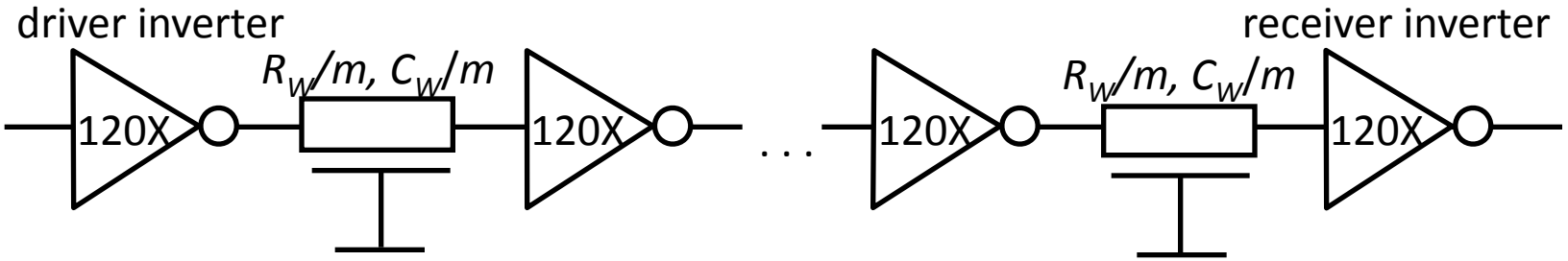


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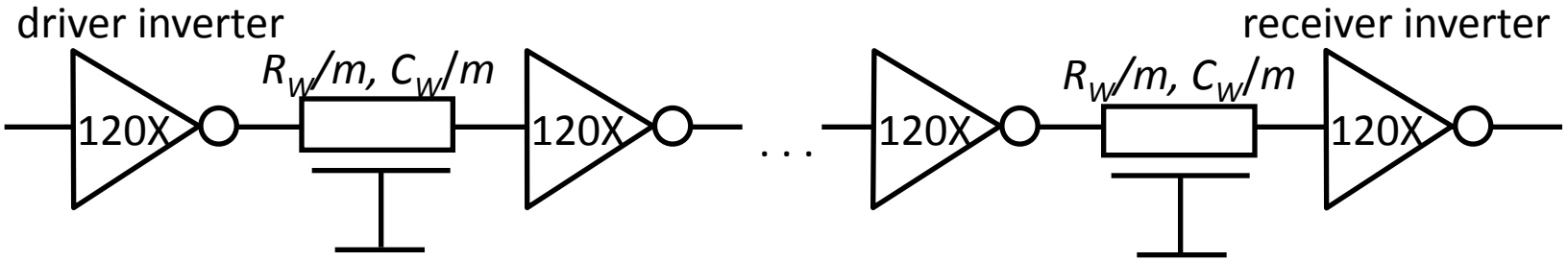
Hence, in the case of our 1 mm wire example, it´s optimal to divide wire in two segments. However, the gain was small and the signal became inverted

# Example: 10 mm wire

But what if the wire is much longer, say 10 mm?

The critical length being 0.42 mm suggests insertion of 22 repeaters, i.e. that we should divide the wire into 23 segments.




The wire effort is now $W_E$=16000/7.2 ≈ 2200

Hence, minimum normalized delay is 4√$W_E$=188≈190.

Summarizing the 23 stage delays gives the same result:

$$d = 23 \times 2 + 2\sqrt{W_E} + \frac{W_E}{46} = 46 + 2 \times 47 + 48 = 188 \approx 190$$

Important comment: An even number of repeaters does not invert the signal!

# Conclusion

- Introduced a distributed wire RC model, the π-model
- Discussed the relevance of a delay model assuming the existence of a dominant time constant
- Understood that wires should be kept short since wire delay or flight time, increases with the wire length squared!

$$W_E = \frac{rcL^2}{RC} \sim L^2 \text{ ! Therefore, keep wires short!}$$

- For long wires, delay can be minimized by inserting repeaters
- We have derived expressions for the optimal number of segments, $m_{opt}$, and for the critical wire length $L_{crit}$
- $$L_{crit} = \frac{L}{m_{opt}} = 2\sqrt{\frac{(RC)_{inverter}}{(rc)_{wire}}}$$

# Introduction to on-chip interconnect

Elmore delay model

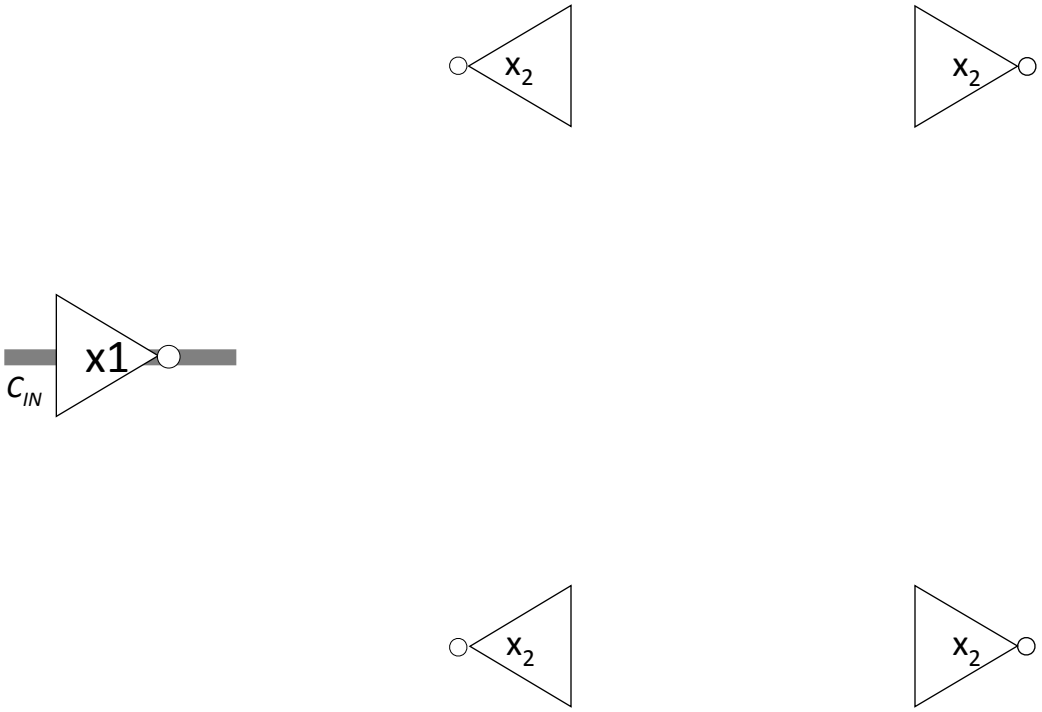
Lecture 7 continued

Tuesday October 2, 2018

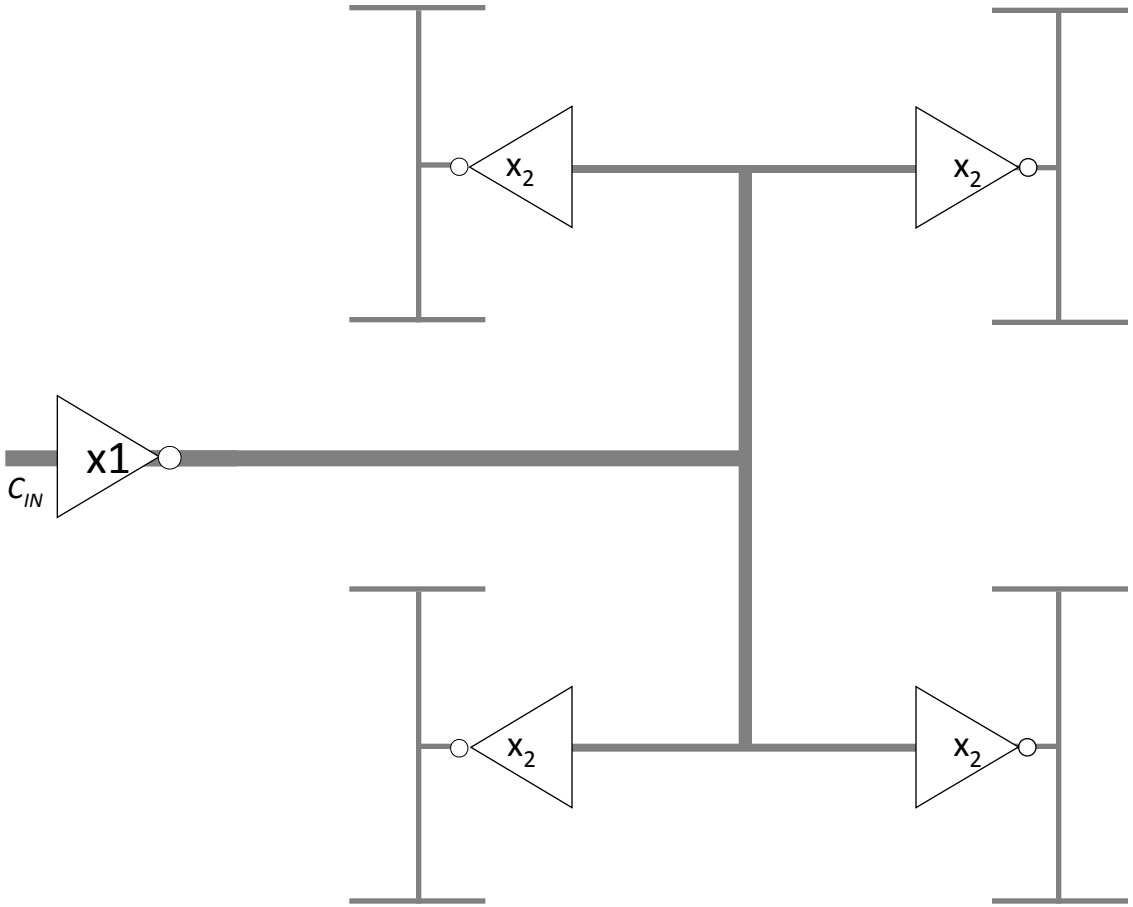
# Outline

- Elmore delay model – a generalized model
- How to handle wire branches
- Conclusions

# H-tree clock distribution



# H-tree clock distribution



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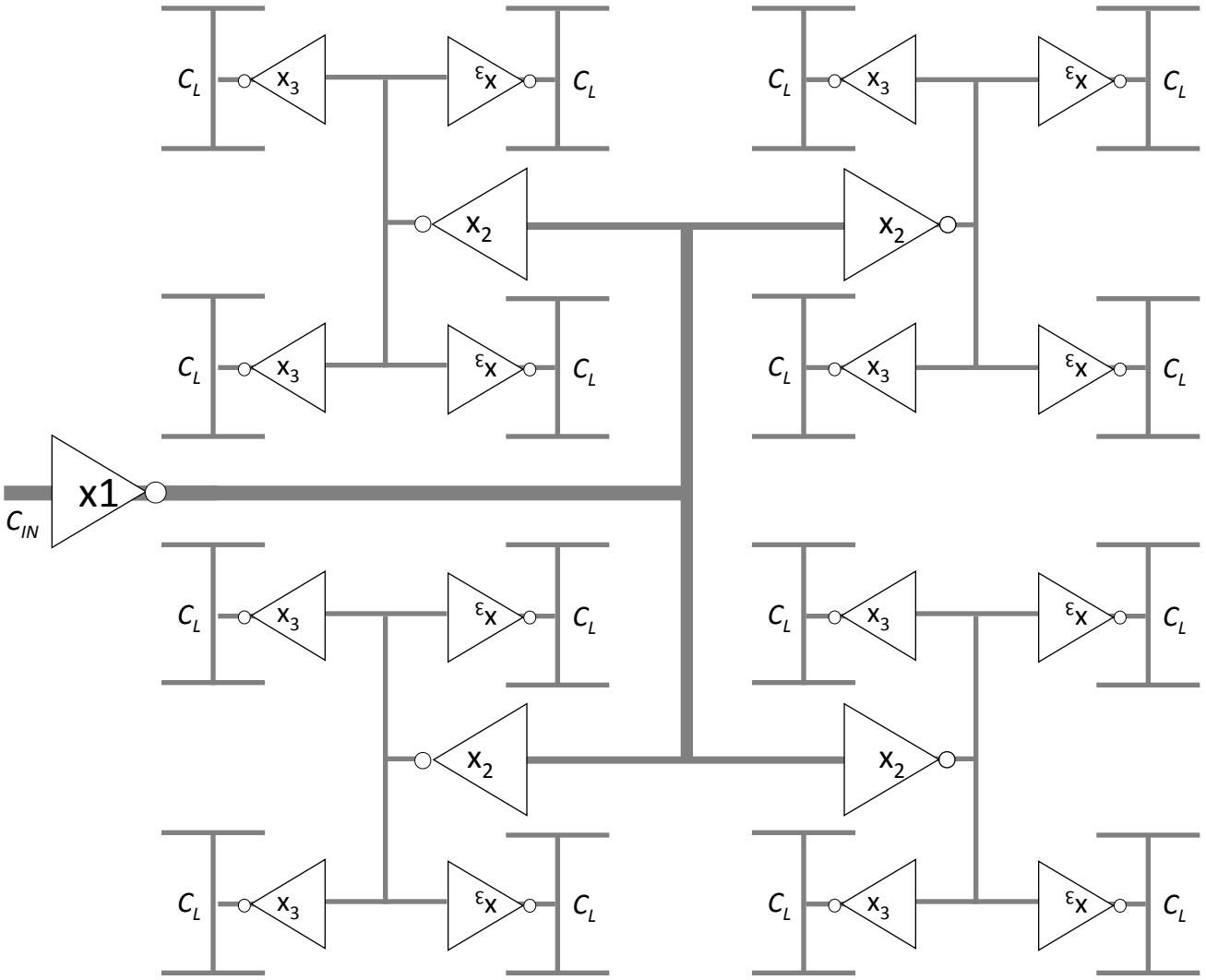
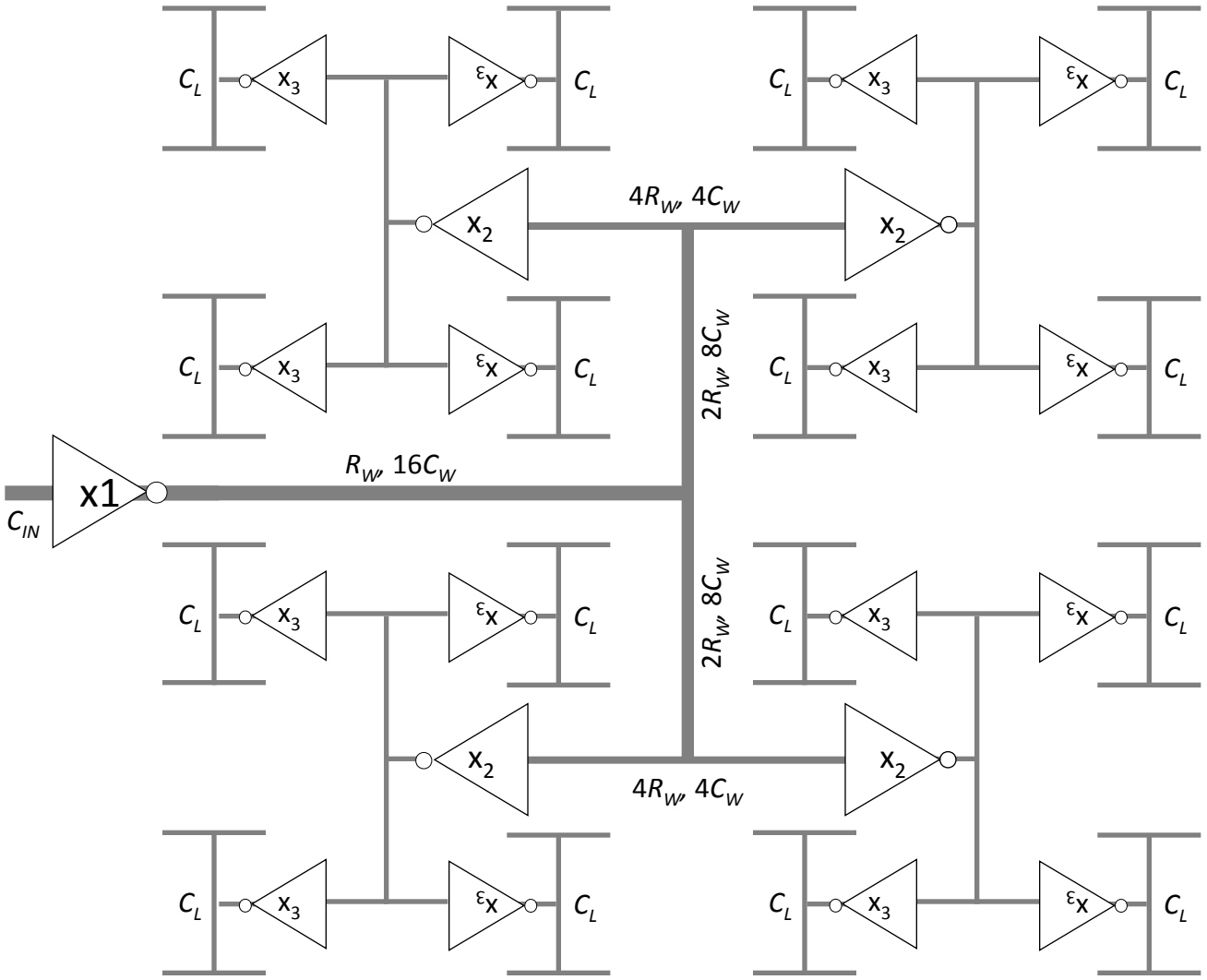


# H-tree clock distribution



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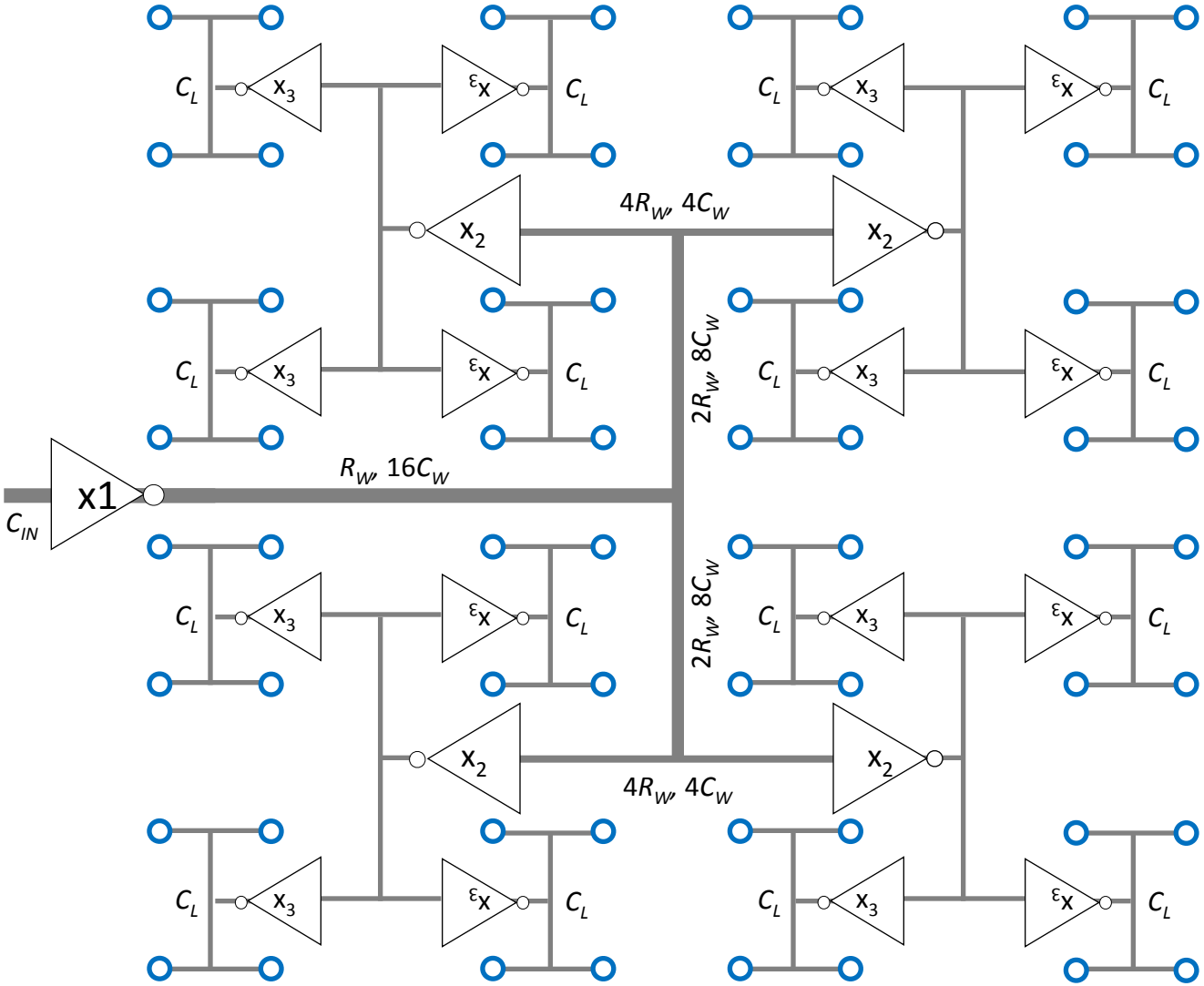
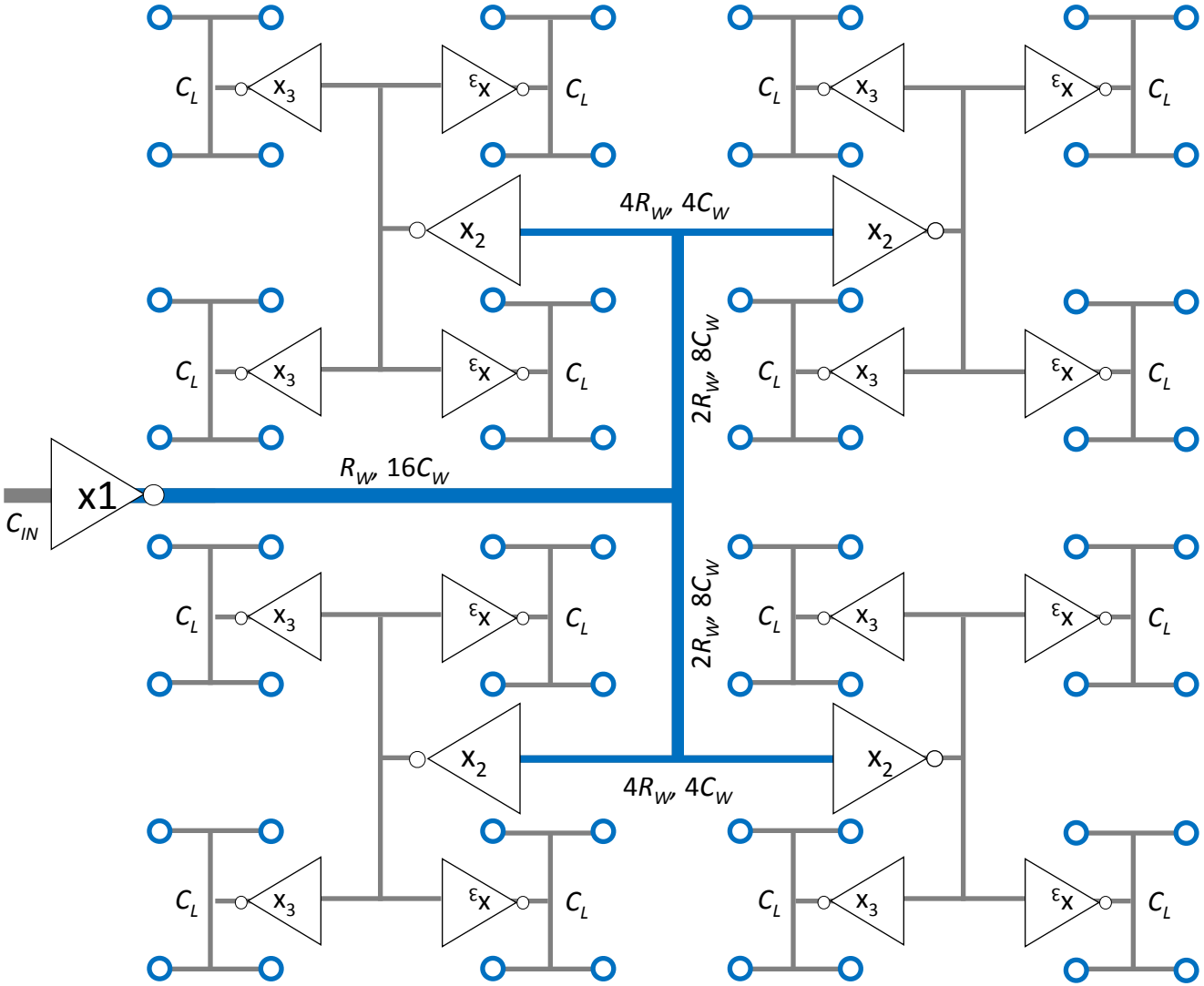


# Identify the critical timing path



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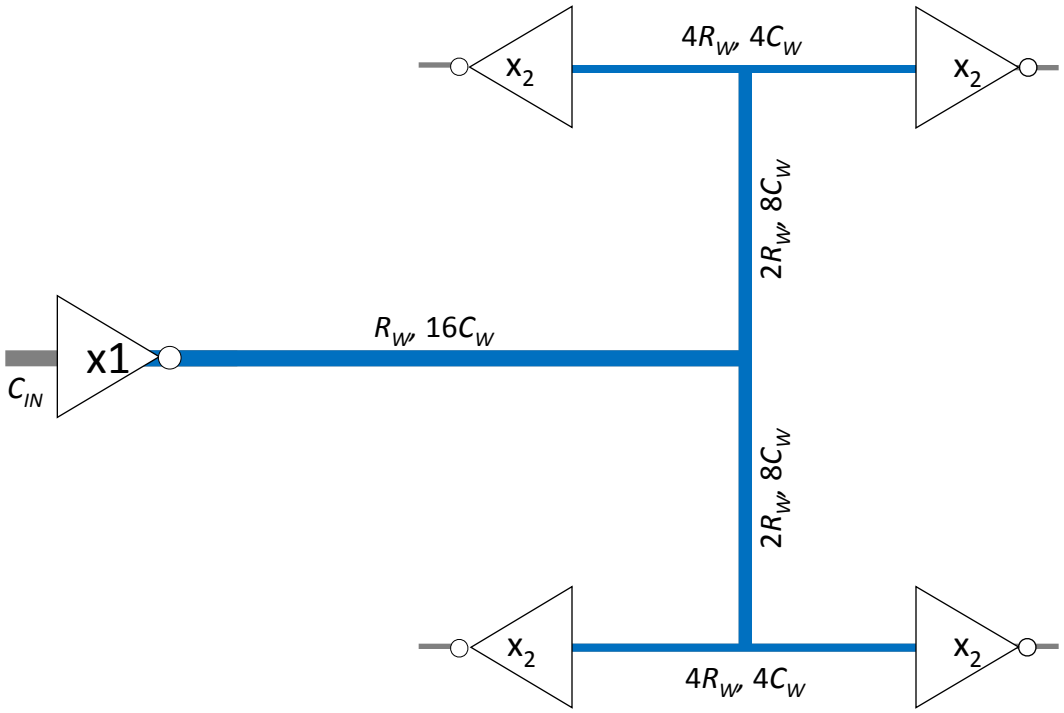

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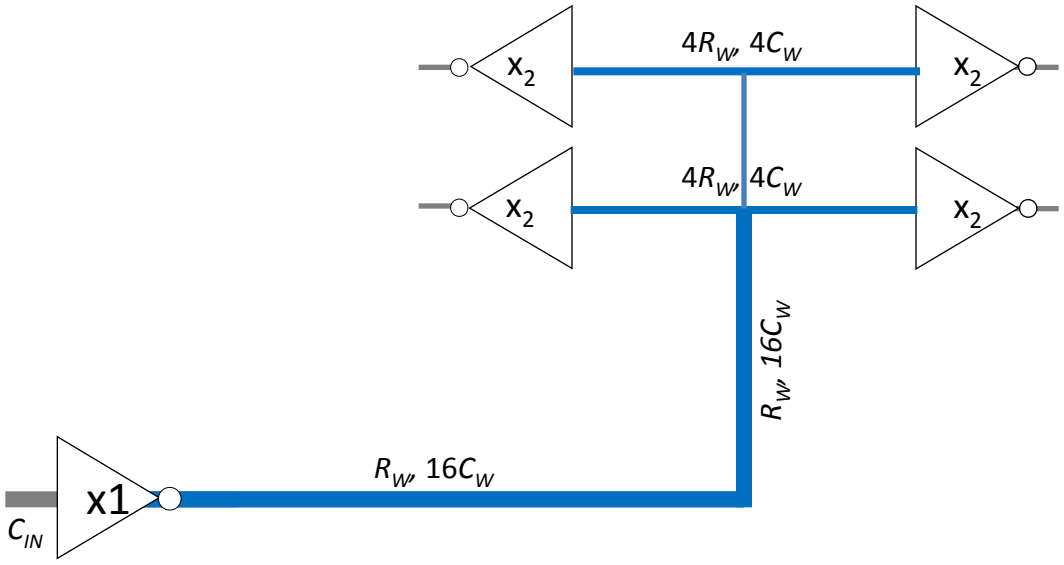

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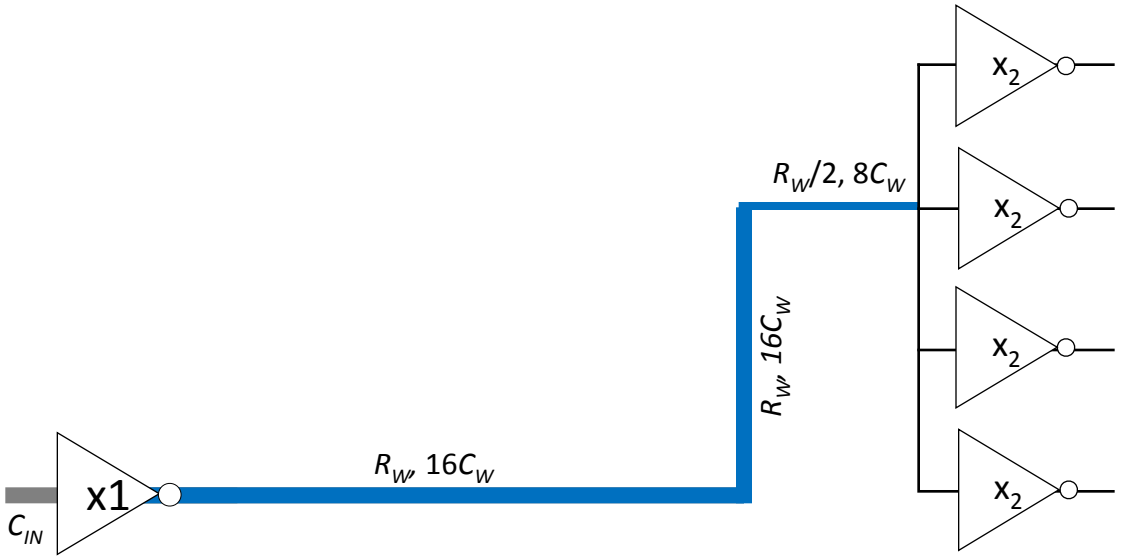

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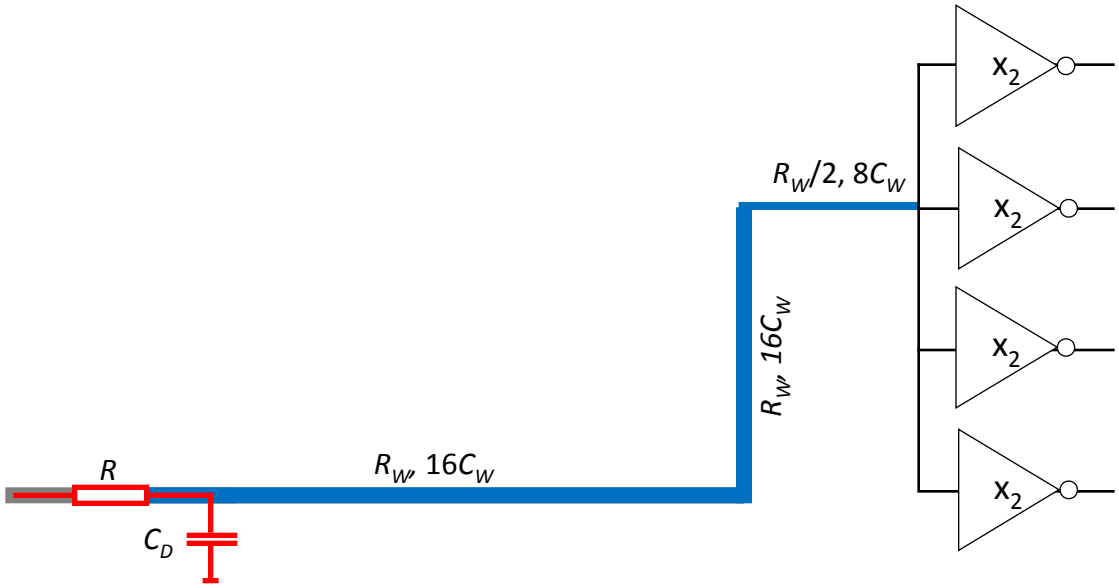

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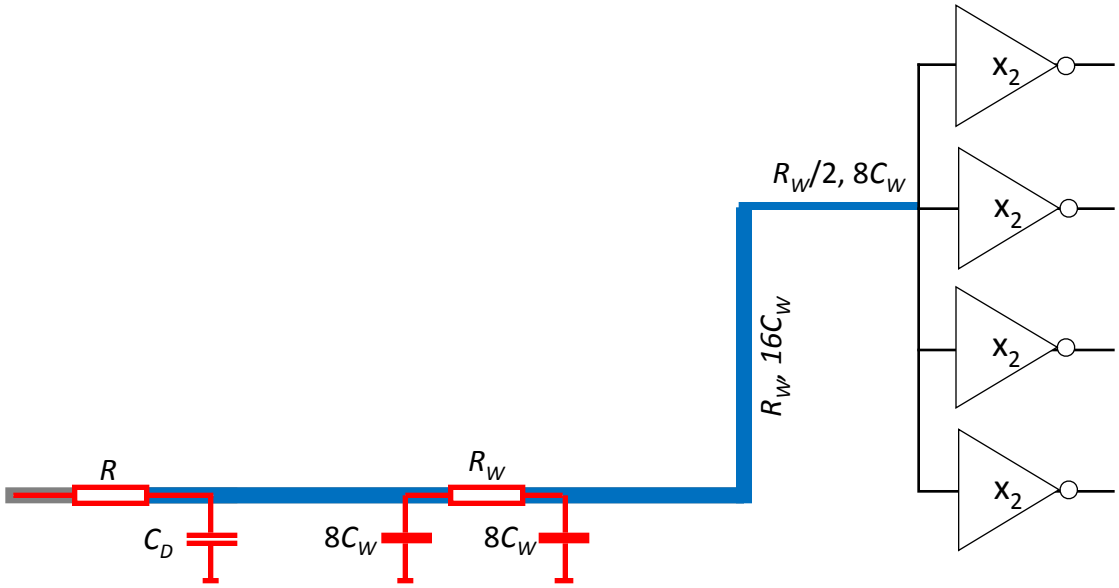

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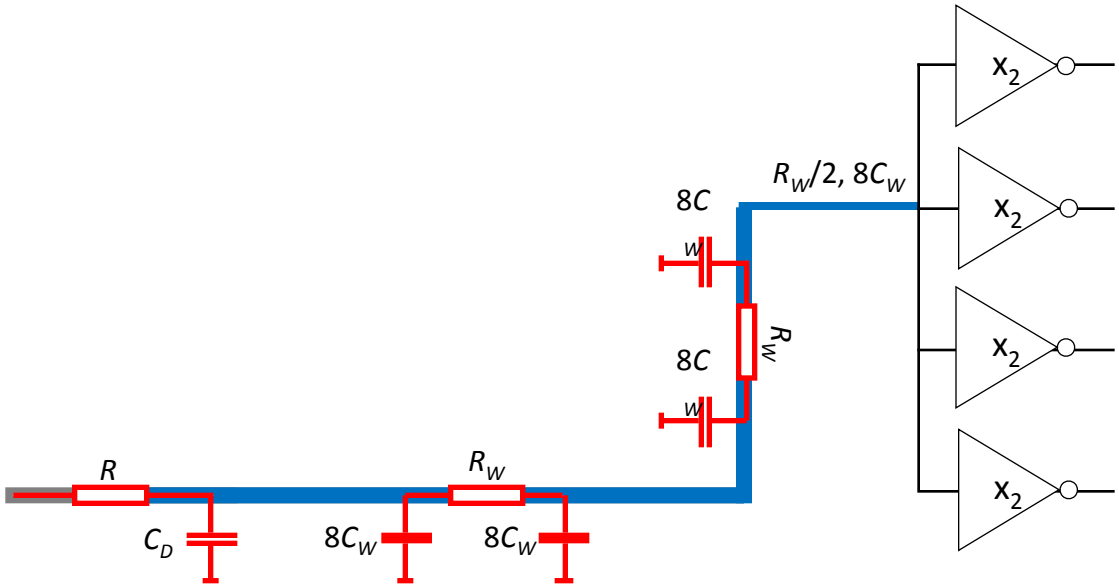

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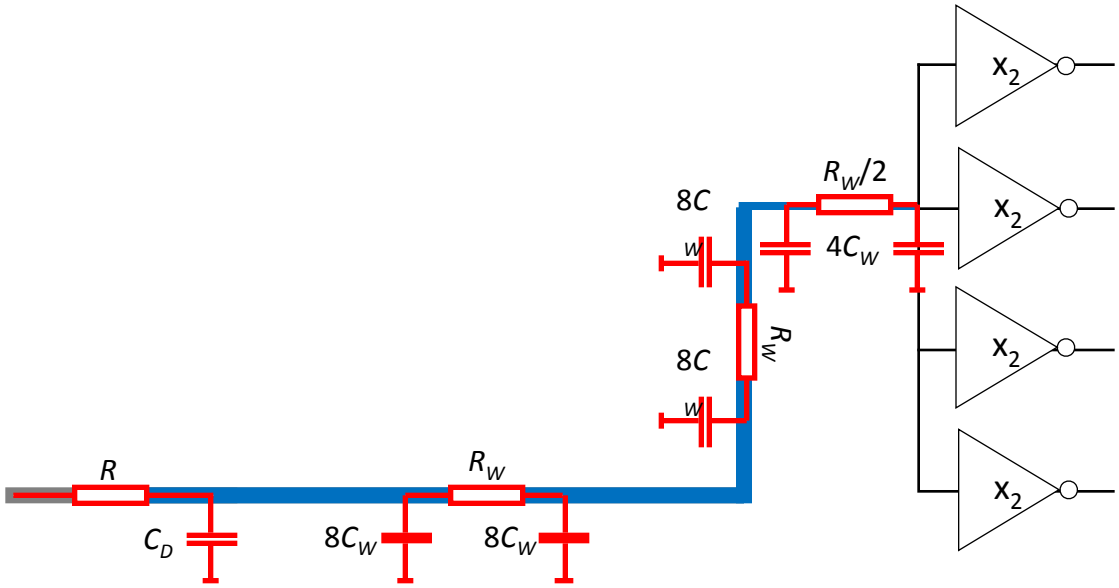

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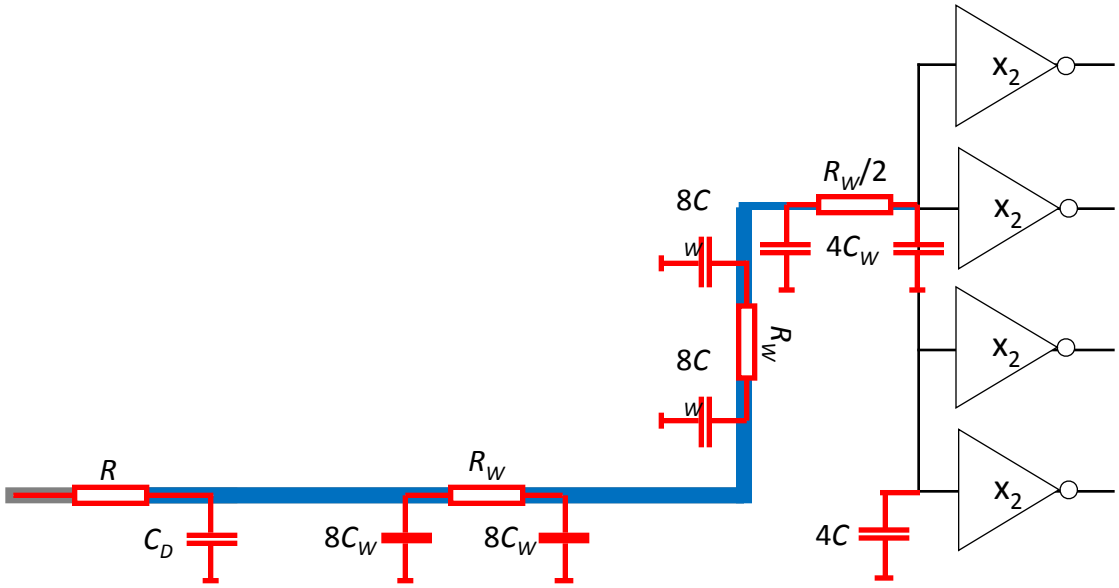

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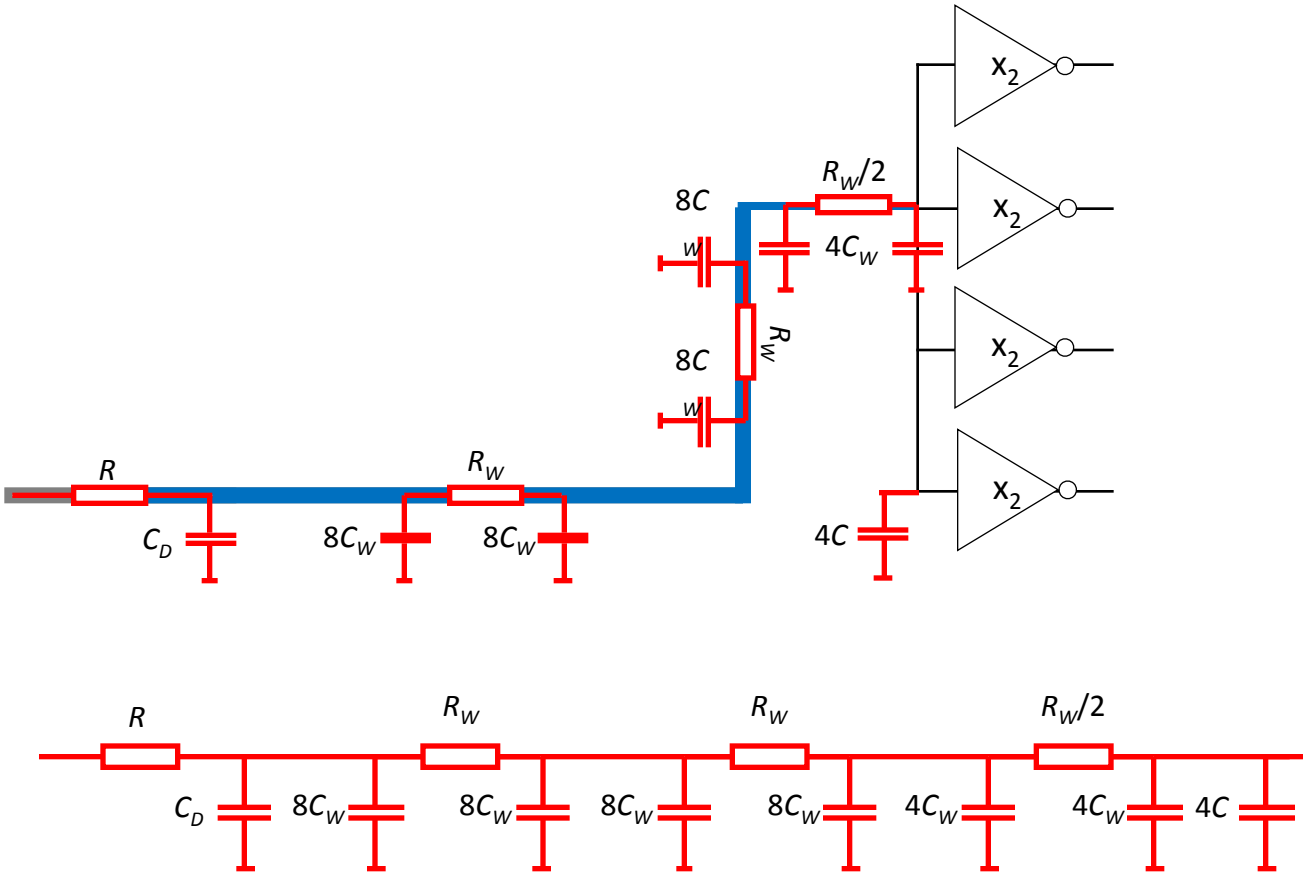

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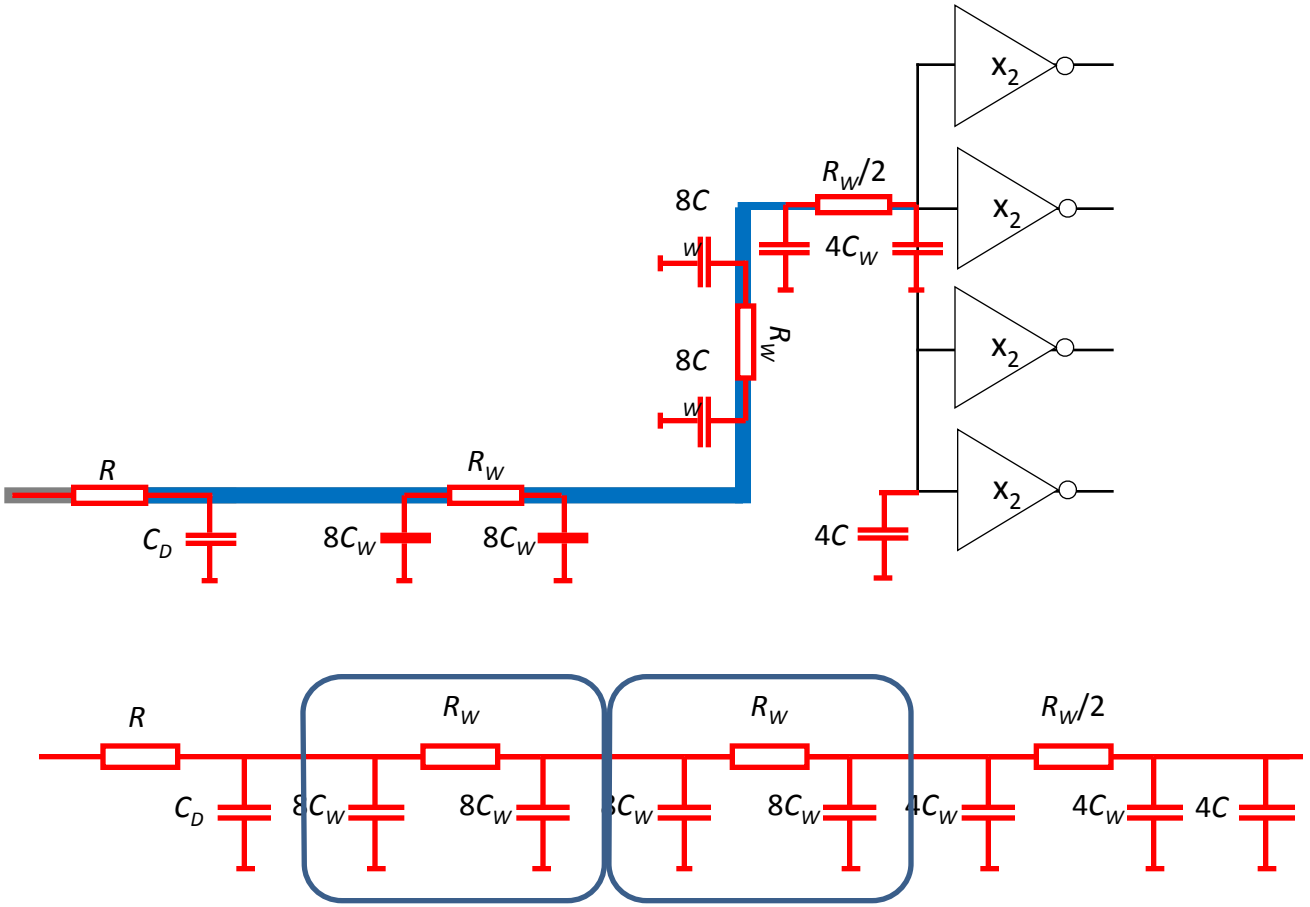

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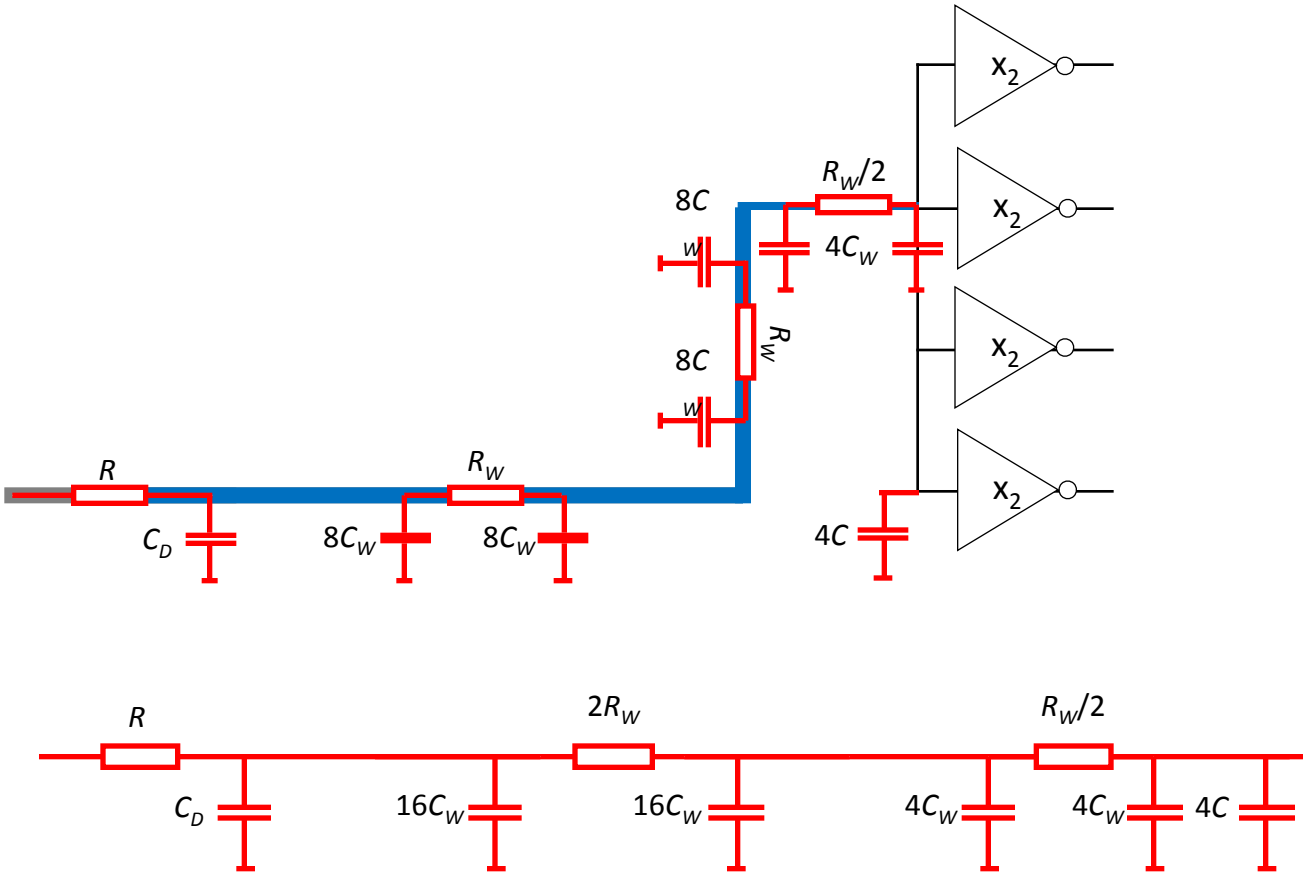
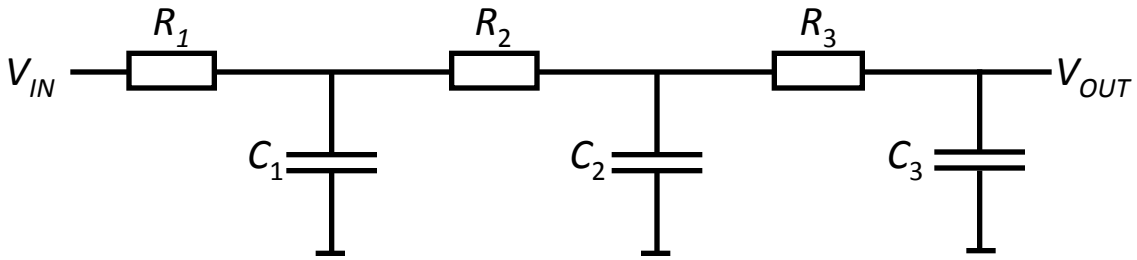
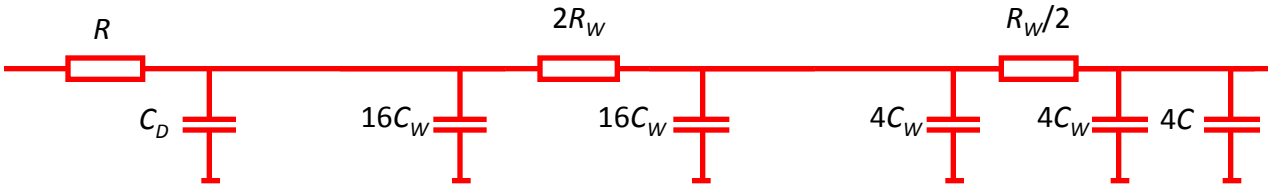


# General solution



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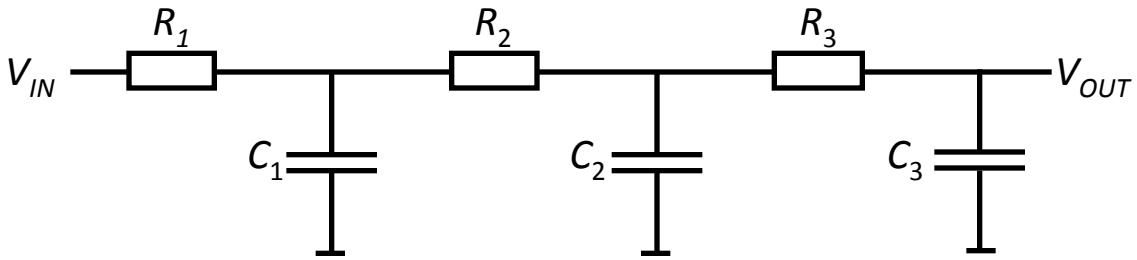


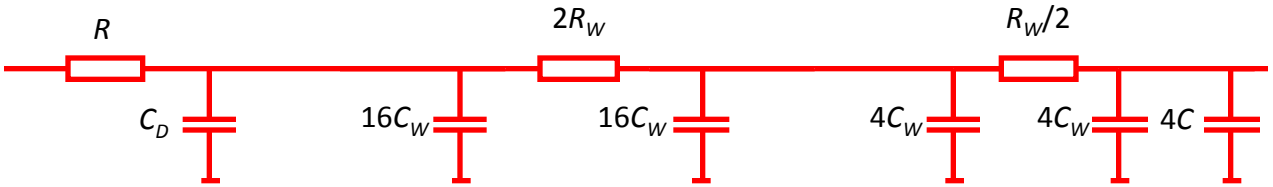

Transfer function

$$H(s) = \frac{1}{as^3 + bs^2 + cs + 1}$$

$$a = R_1R_2R_3C_1C_2C_3$$

$$b = R_1R_2C_1C_2 + R_1R_2C_1C_3 + R_1R_3C_2C_3 + R_2R_3C_2C_3$$

$$c = R_1(C_1 + C_2 + C_3) + R_2(C_2 + C_3) + R_3C_3$$



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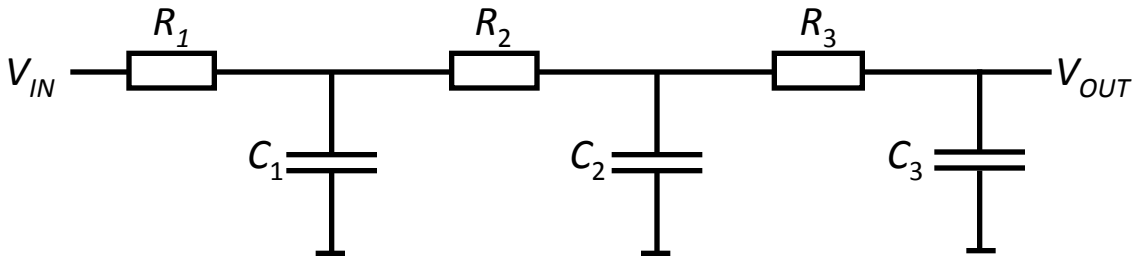


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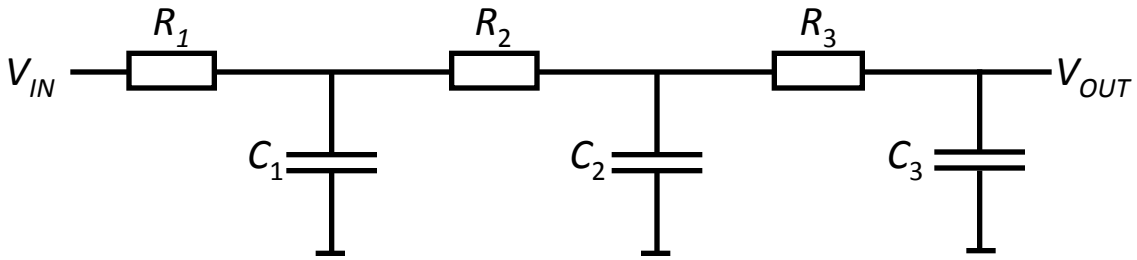
$$c = R_1(C_1 + C_2 + C_3) + R_2(C_2 + C_3) + R_3C_3$$

This transfer function corresponds to a third order linear differential equation
The solution is a sum of three exponentials with three different time constants
We cannot solve this analytically.
But if we assume that there is a dominant time constant $T_E$ it is given by $c$

# General solution

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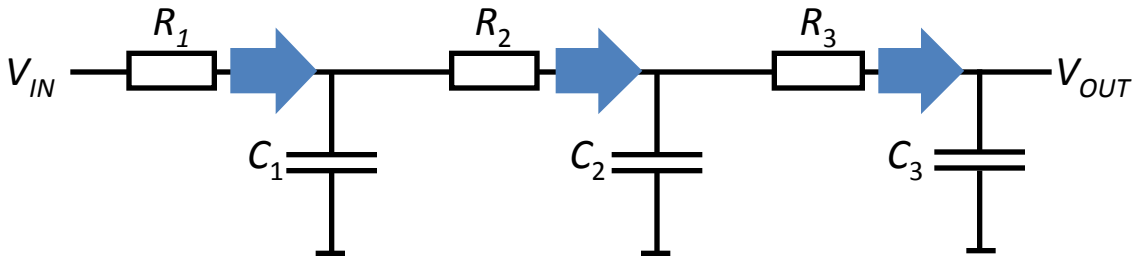
# General solution

Each resistance is multiplied by its downstream capacitance!

$$T_E = R_1\left(C_1 + C_2 + C_3\right) + R_2\left(C_2 + C_3\right) + R_3C_3$$

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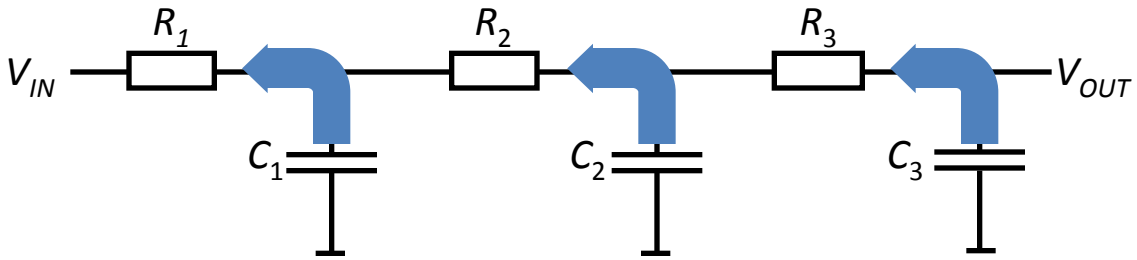
$$T_E = R_1\left(C_1 + C_2 + C_3\right) + R_2\left(C_2 + C_3\right) + R_3C_3$$

# General solution

Each capacitance is multiplied by its upstream resistance!

$$T_E = C_3\left(R_1 + R_2 + R_3\right) + C_2\left(R_1 + R_2\right) + C_1R_1$$

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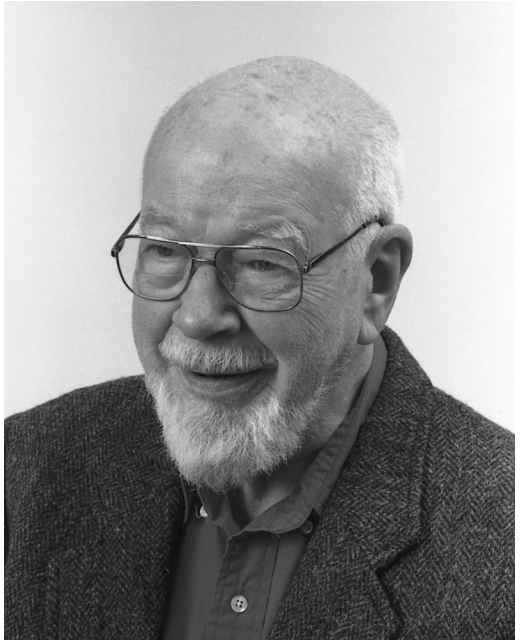
# The man behind Elmore delay

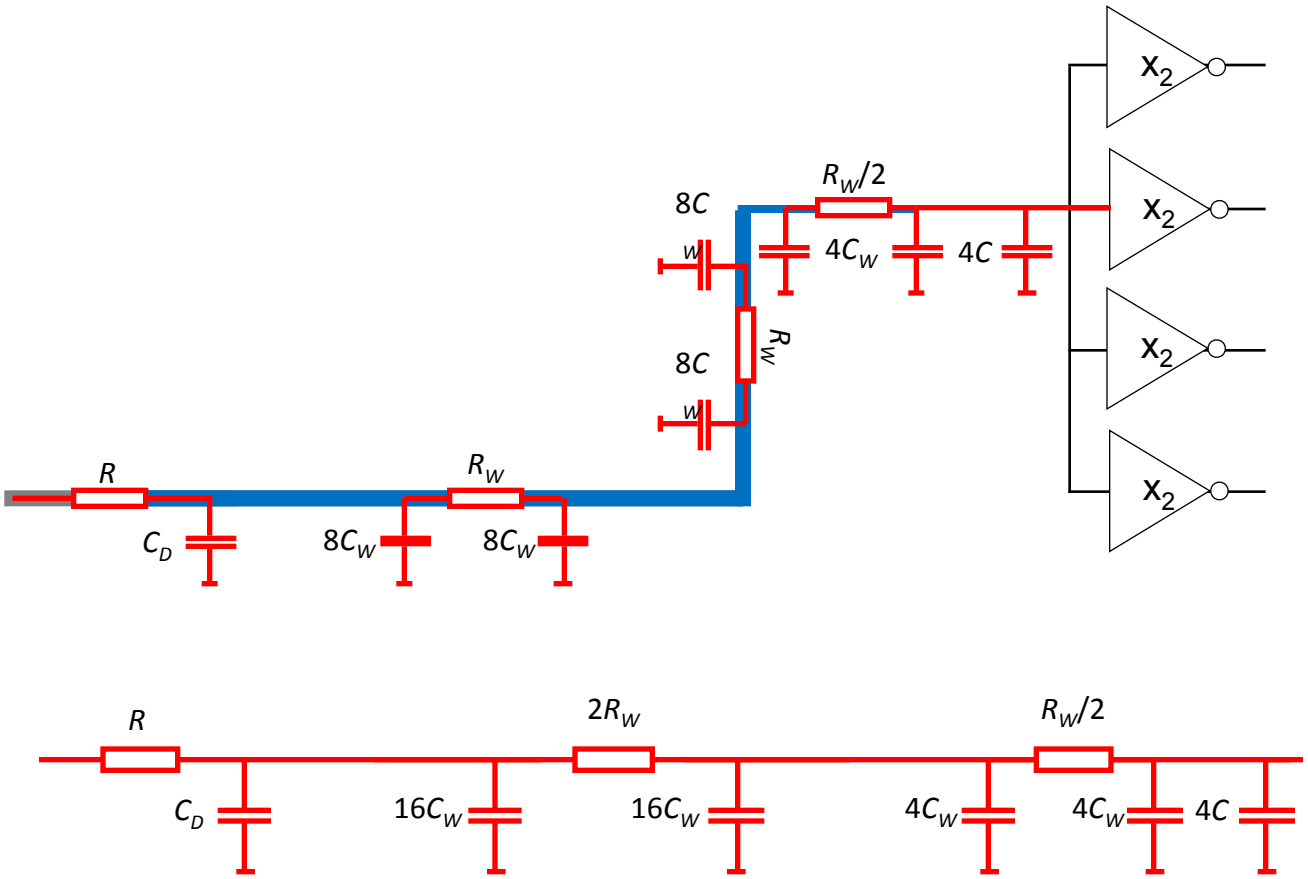
- William Cronk Elmore (1909 - 2003) was an American physicist, educator, and author.
- He is best known for his work on and related to the Manhattan project during World War II.
- Professor of Physics at Swarthmore College, Pennsylvania, from 1938 to 1974.
- Authored two influential books during his life,
  - Electronics-Experimental Techniques with M. Sands
  - Physics of Waves with Mark Heald.
- He is also known for deriving a simple approximation for the delay through an RC network, known as the Elmore delay.
- Despite his clear potential for advancing theoretical and experimental physics, Elmore was known for developing (and publishing) laboratory experiments that effectively taught students the fundamentals of physics.



W. C. Elmore

W.C. Elmore. The Transient Analysis of Damped Linear Networks with Particular Regard to Wideband Amplifiers, J. Applied Physics, vol. 19(1), 1948

# Identify the critical timing path



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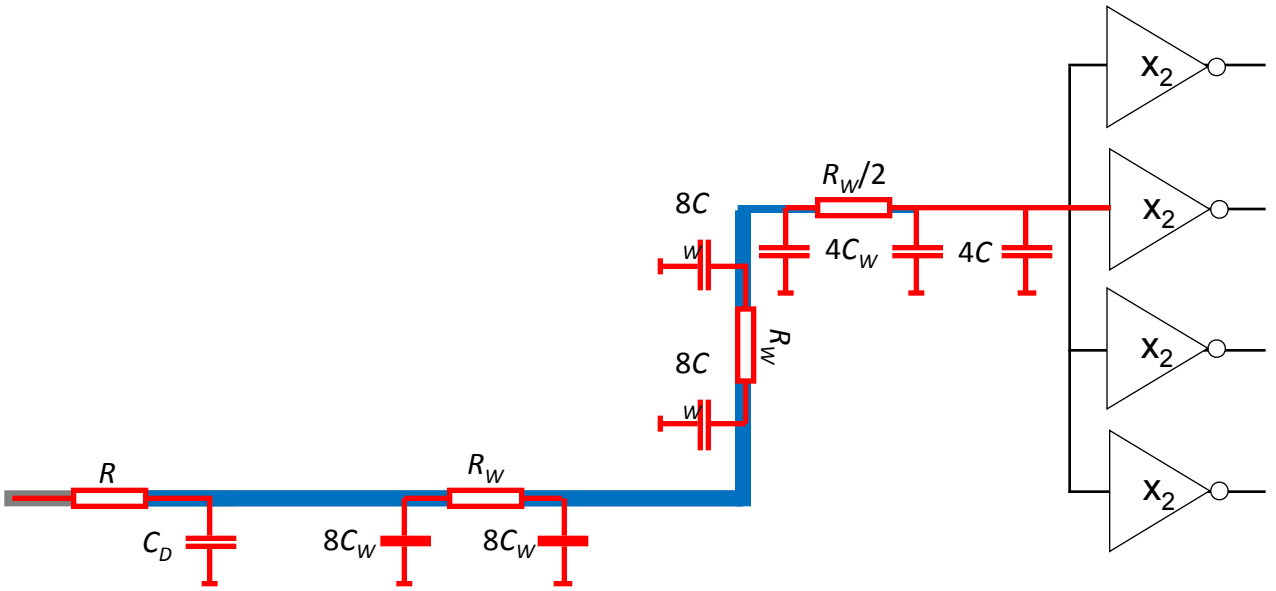


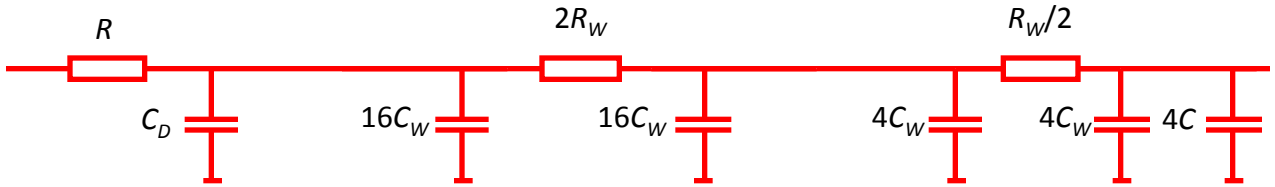


$$T_E = R\left(C_D + 4C\right) + R \times 40C_W + 2R_W\left(4C + 24C_W\right) + \frac{R_W}{2}\left(4C + 4C_W\right)$$

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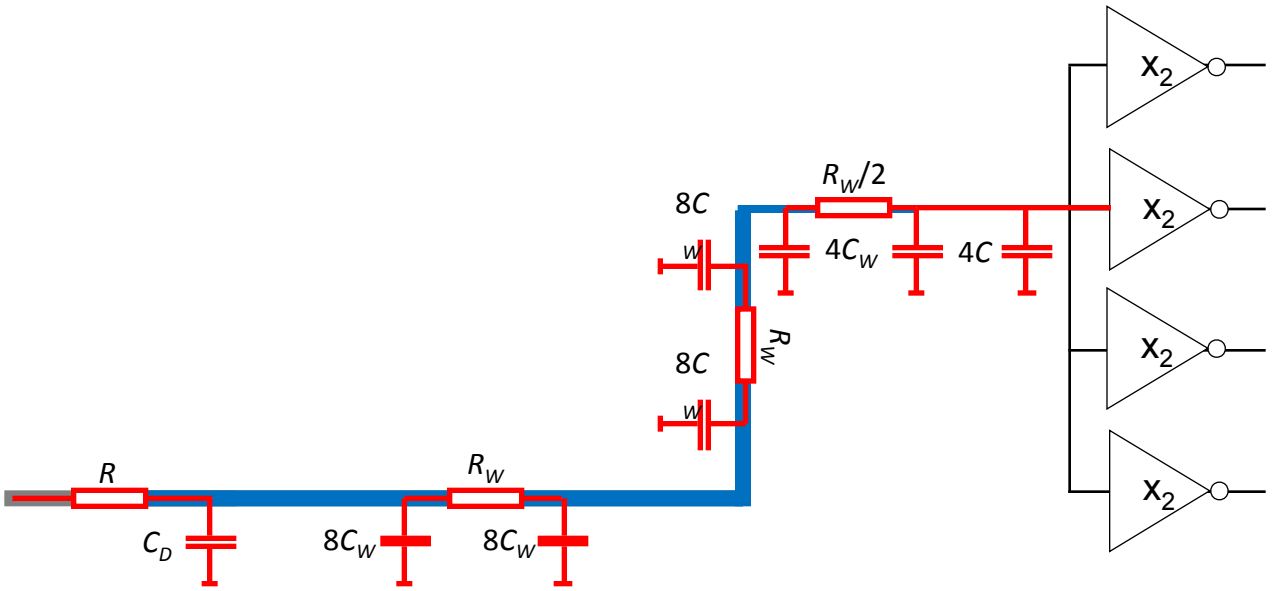


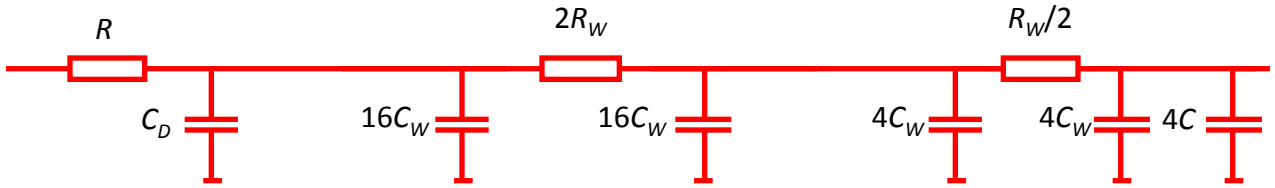


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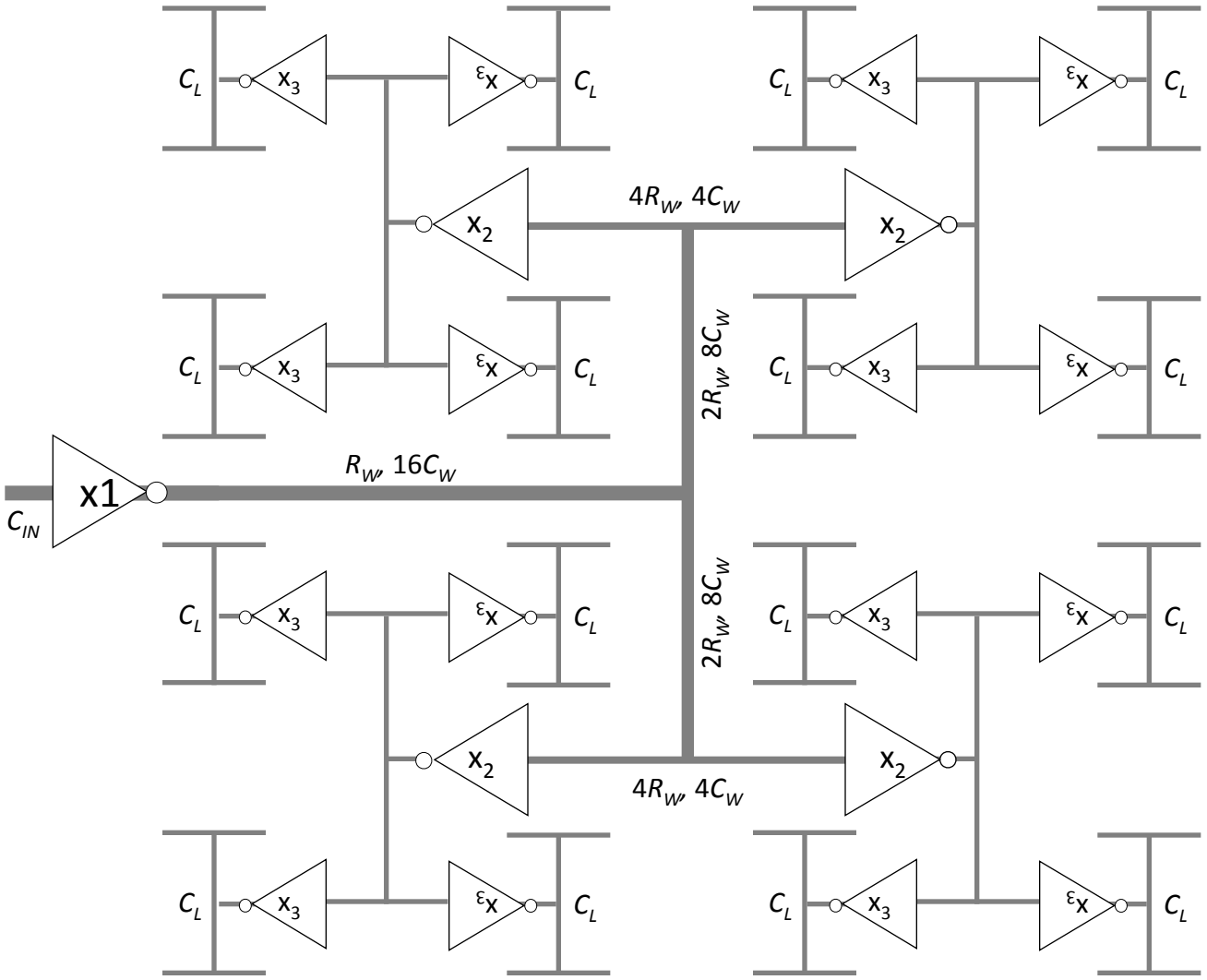
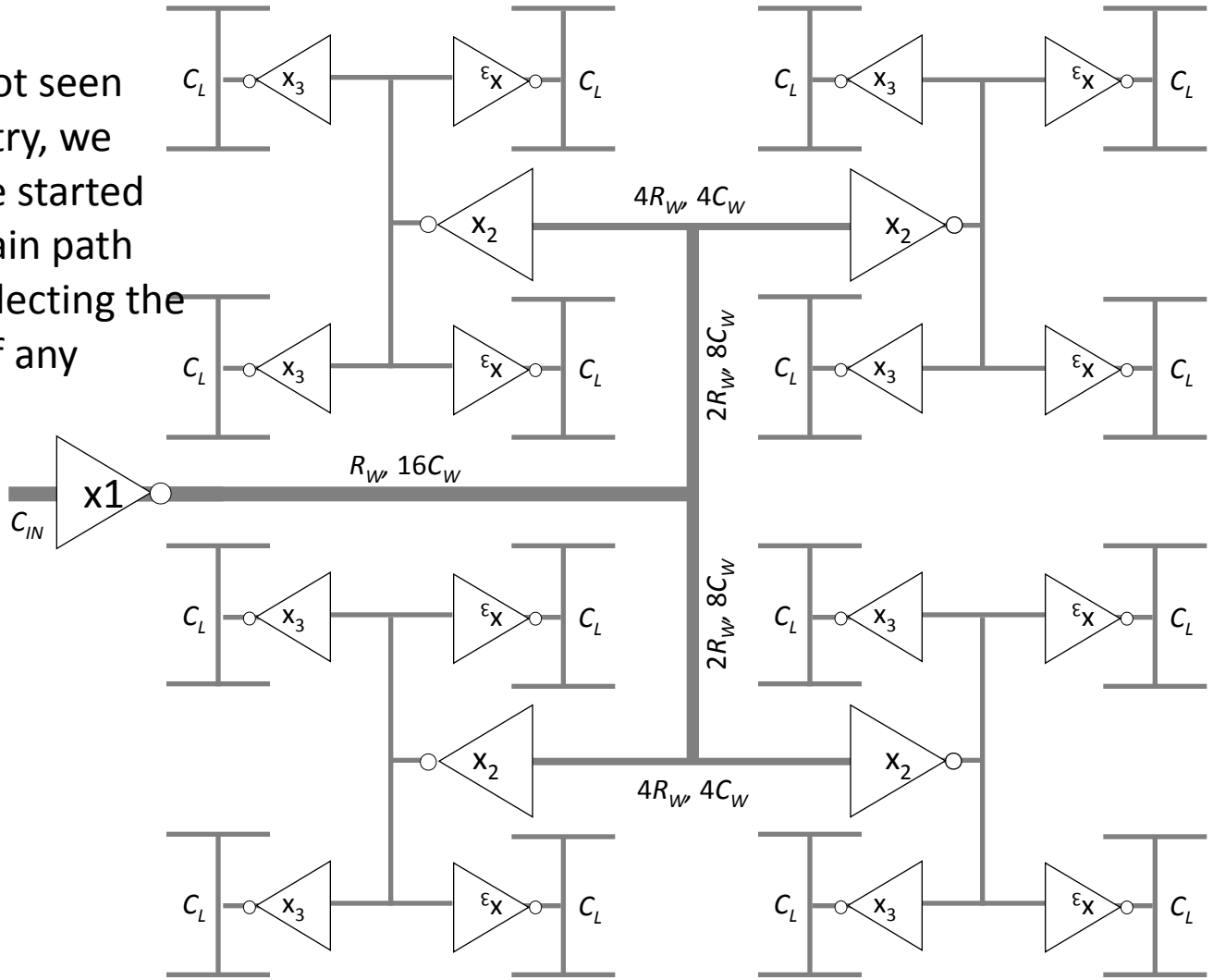
$$T_E = R\left(C_D + 4C\right) + 40RC_W + 10R_W C + 50R_W C_W$$

# H-tree clock distribution



# H-tree clock distribution

If we had not seen the symmetry, we should have started with the main path delay – neglecting the influence of any branches



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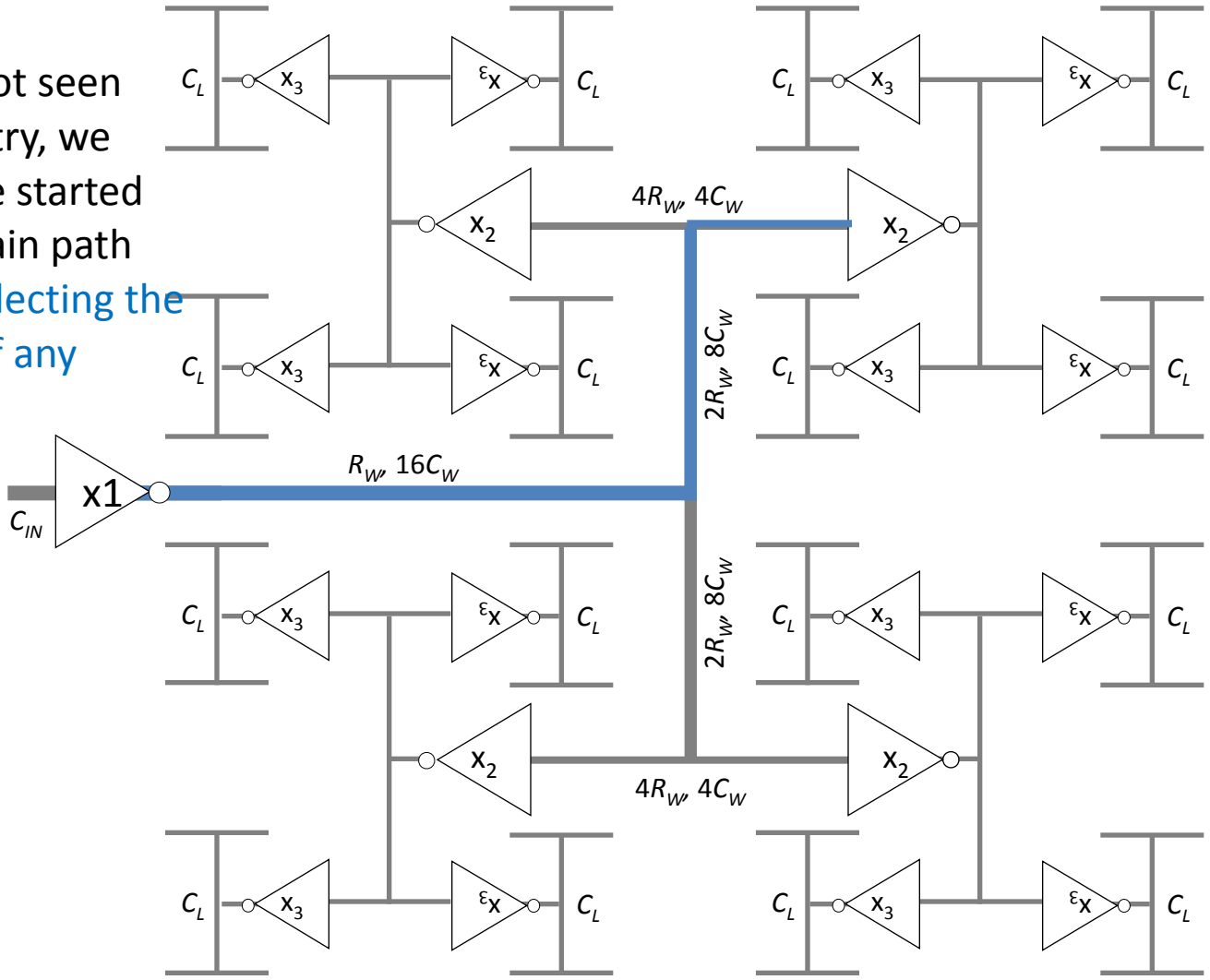

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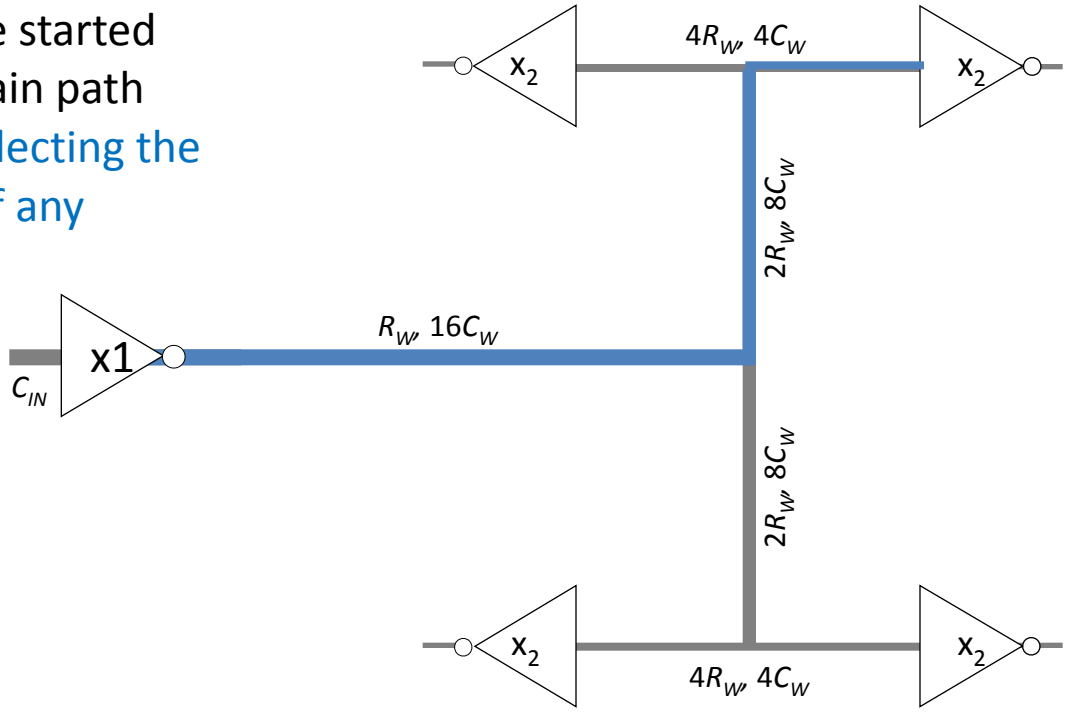

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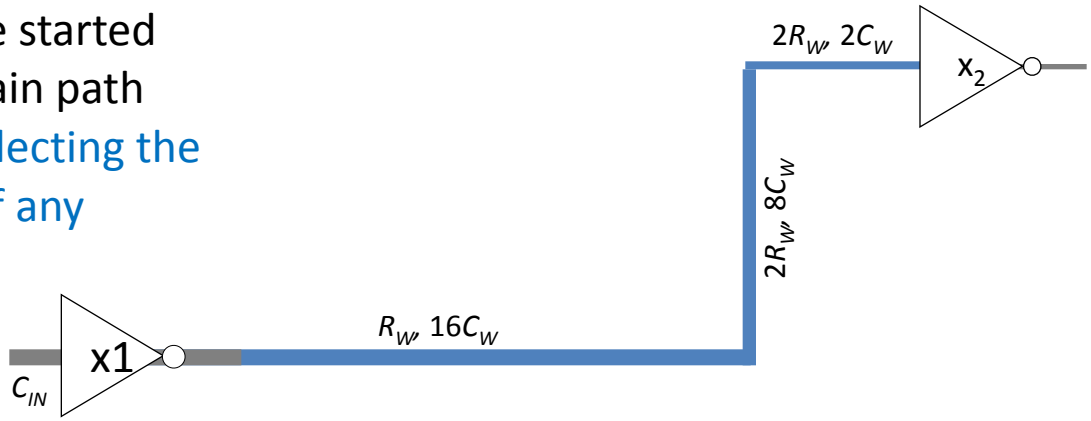

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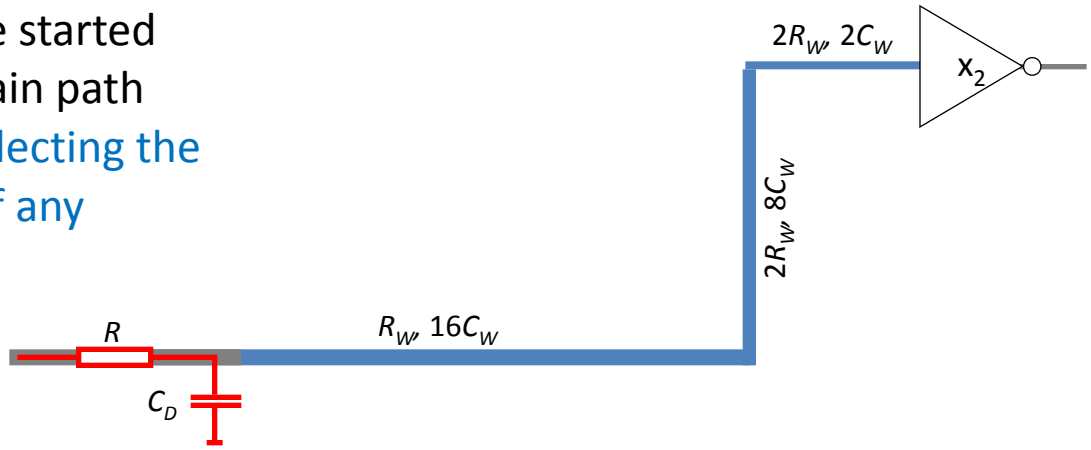

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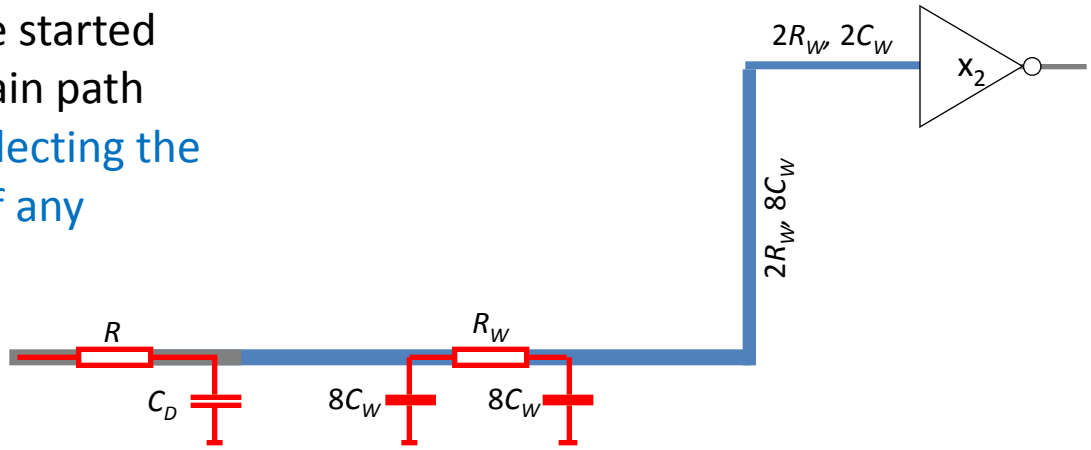

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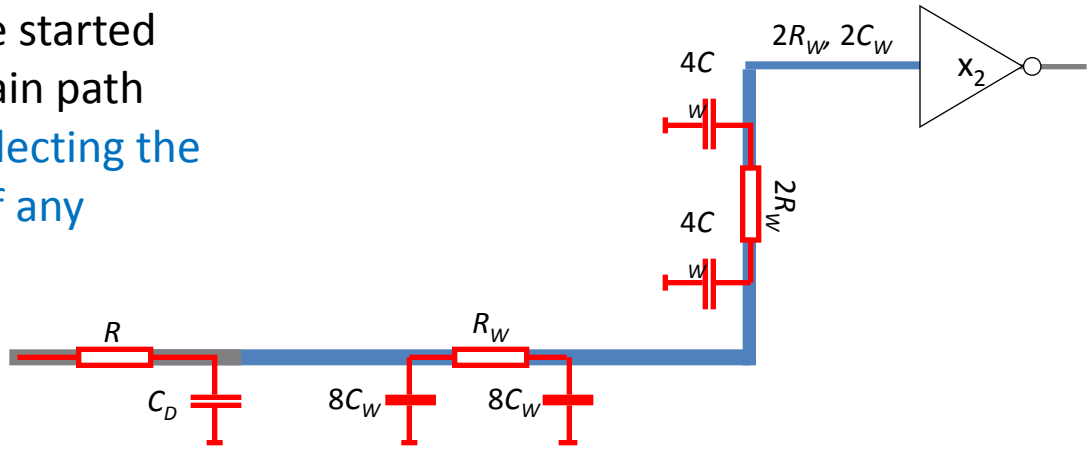

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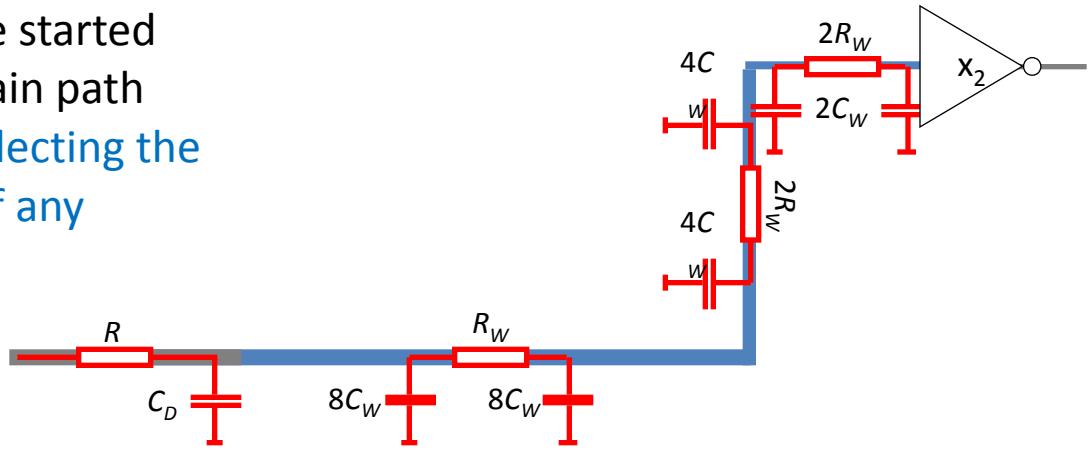

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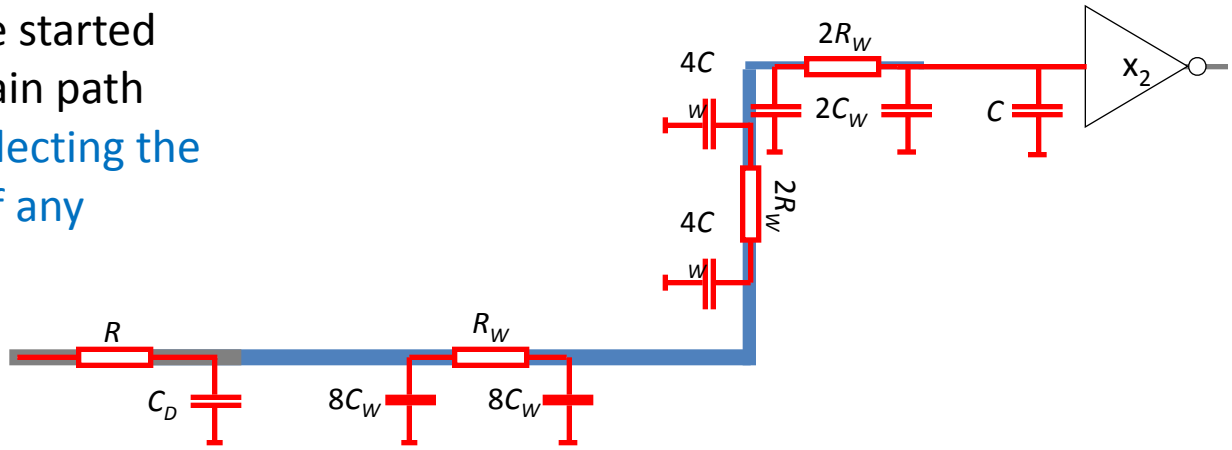

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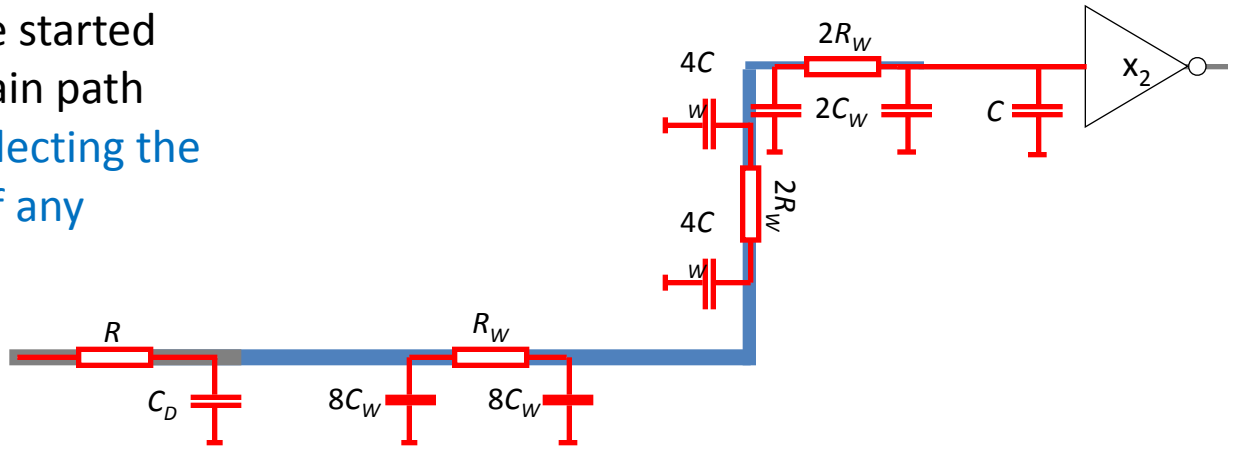
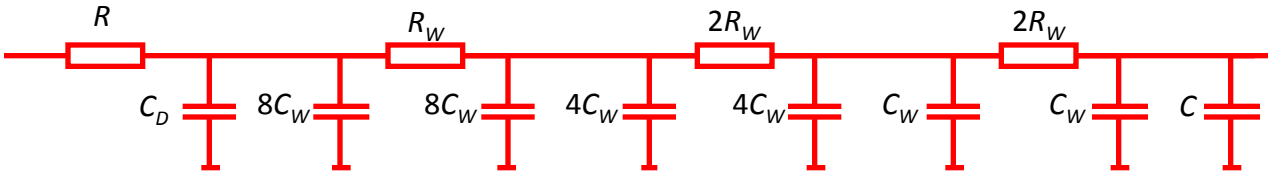



Electrical RC wire model (neglecting branches)



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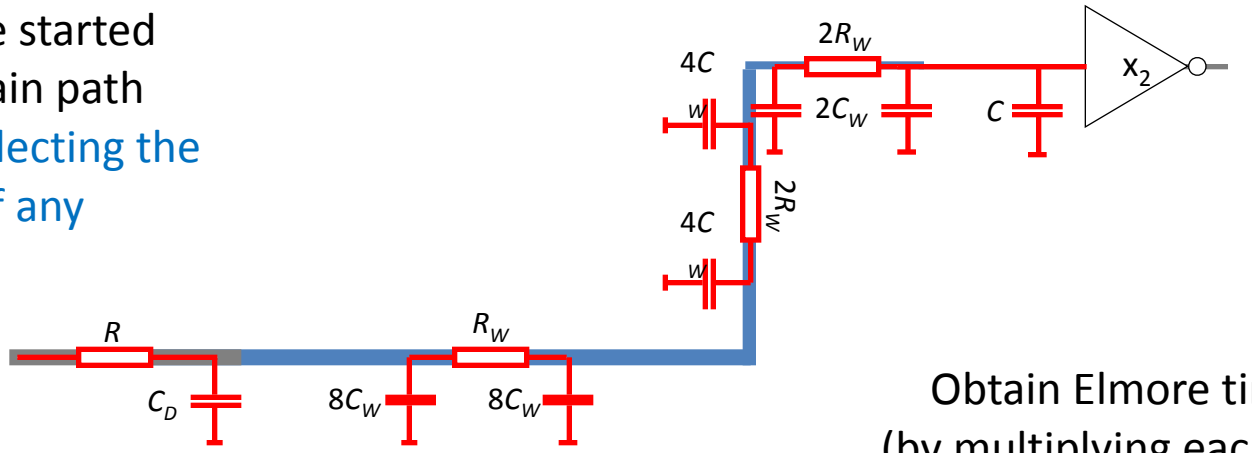


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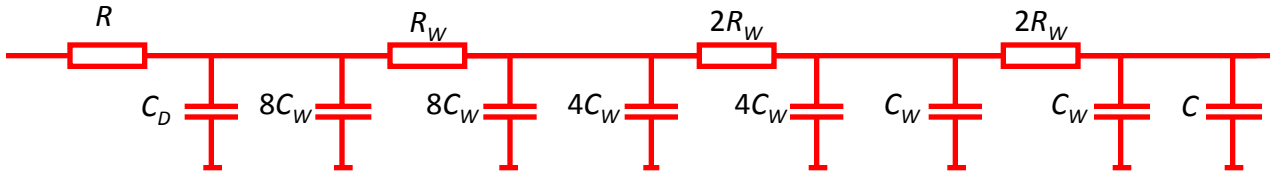
Obtain Elmore time constant (by multiplying each resistance by all downstream capacitances)



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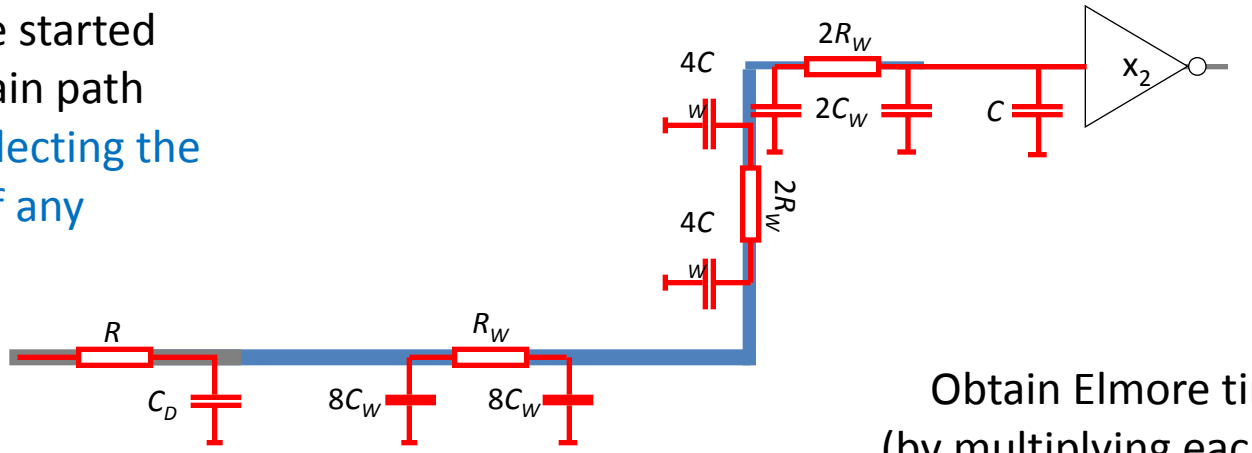


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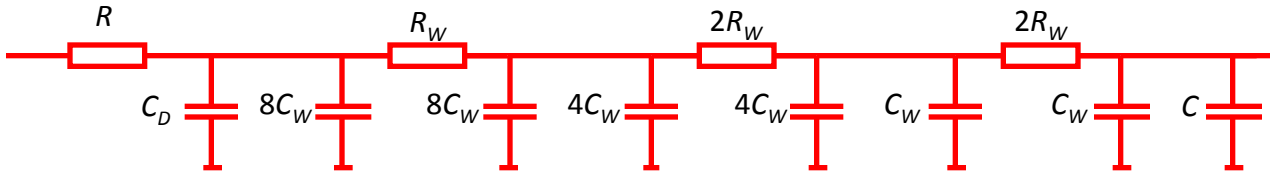


$$T_{E,main} = R\left(C_D + C\right) + R \times 26C_W + R_W\left(C + 18C_W\right) + 2R_W\left(C + 6C_W\right) + 2R_W\left(C + C_W\right)$$

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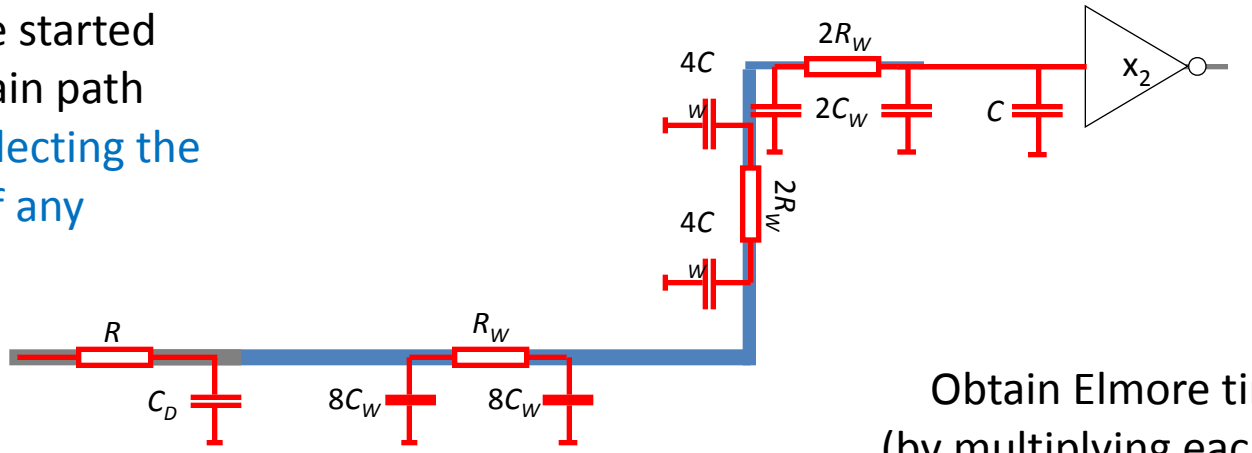


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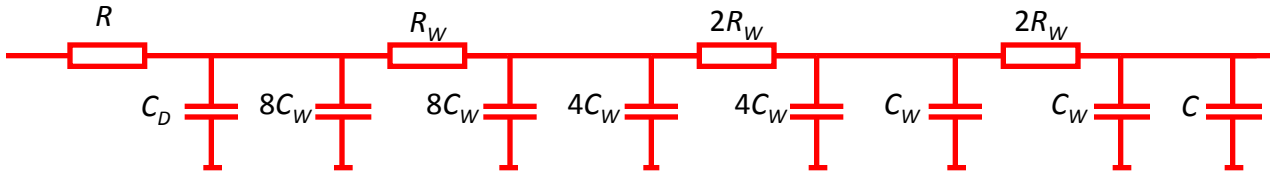


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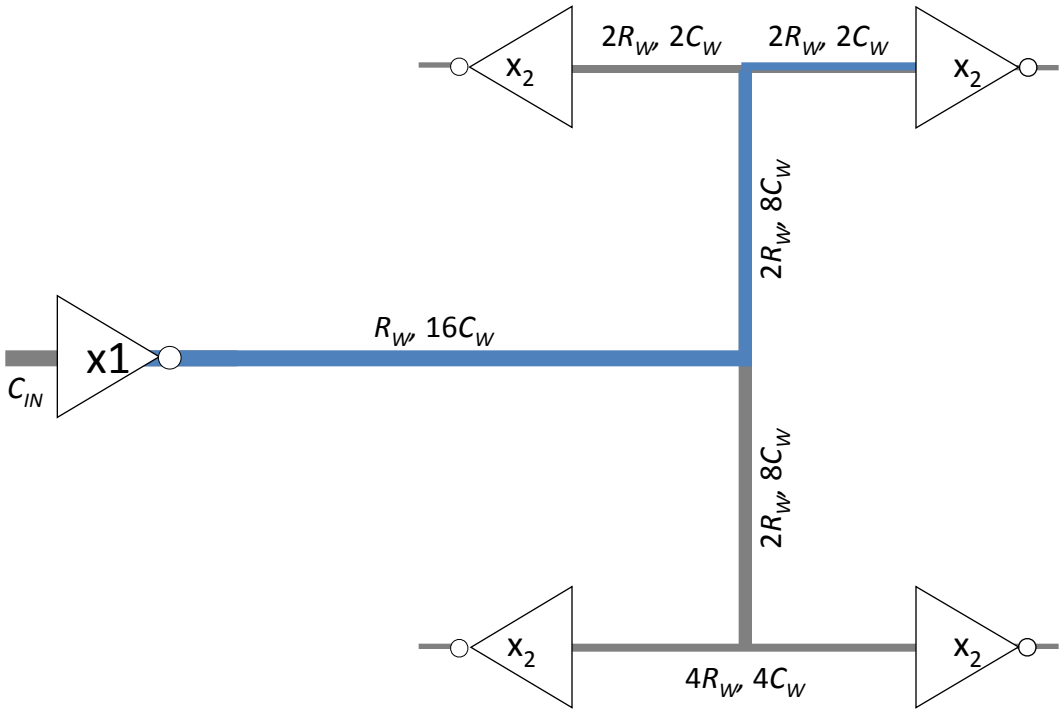
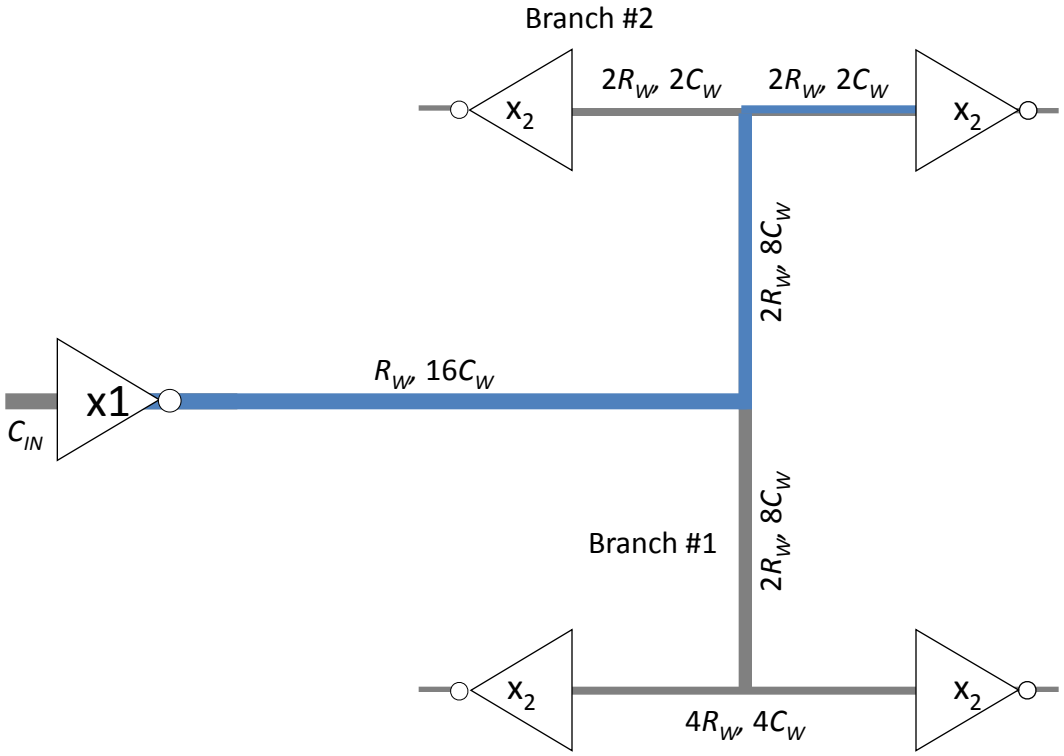
# Then consider neglected branches



# Then consider neglected branches

We have two neglected branches: #1 and #2



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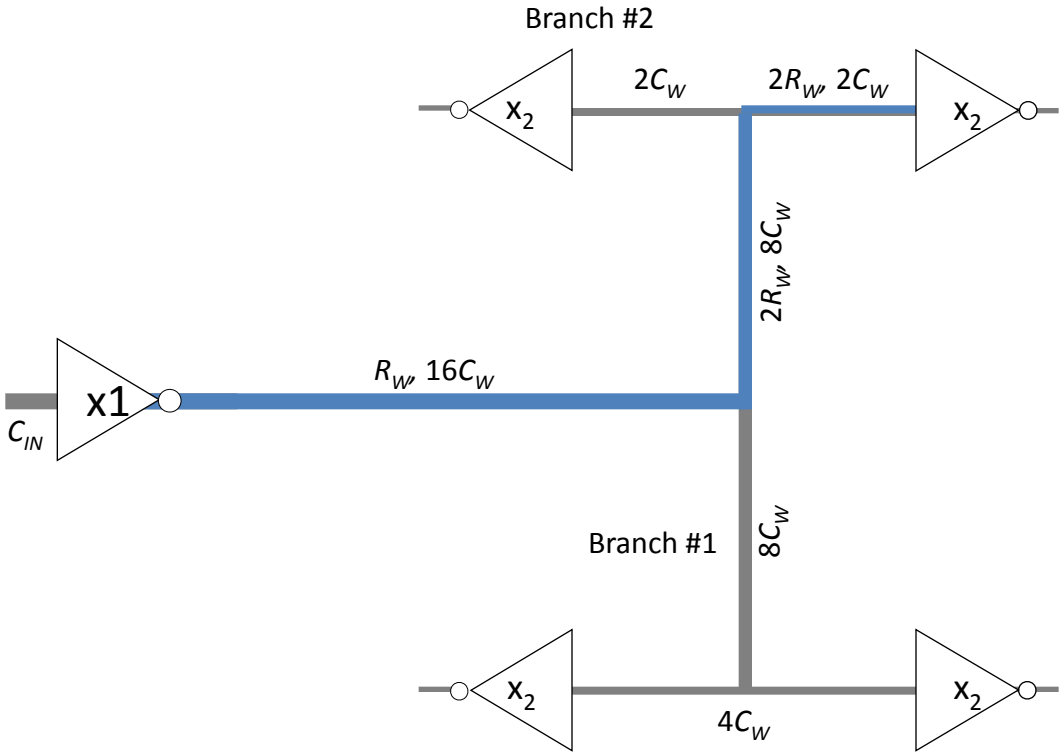

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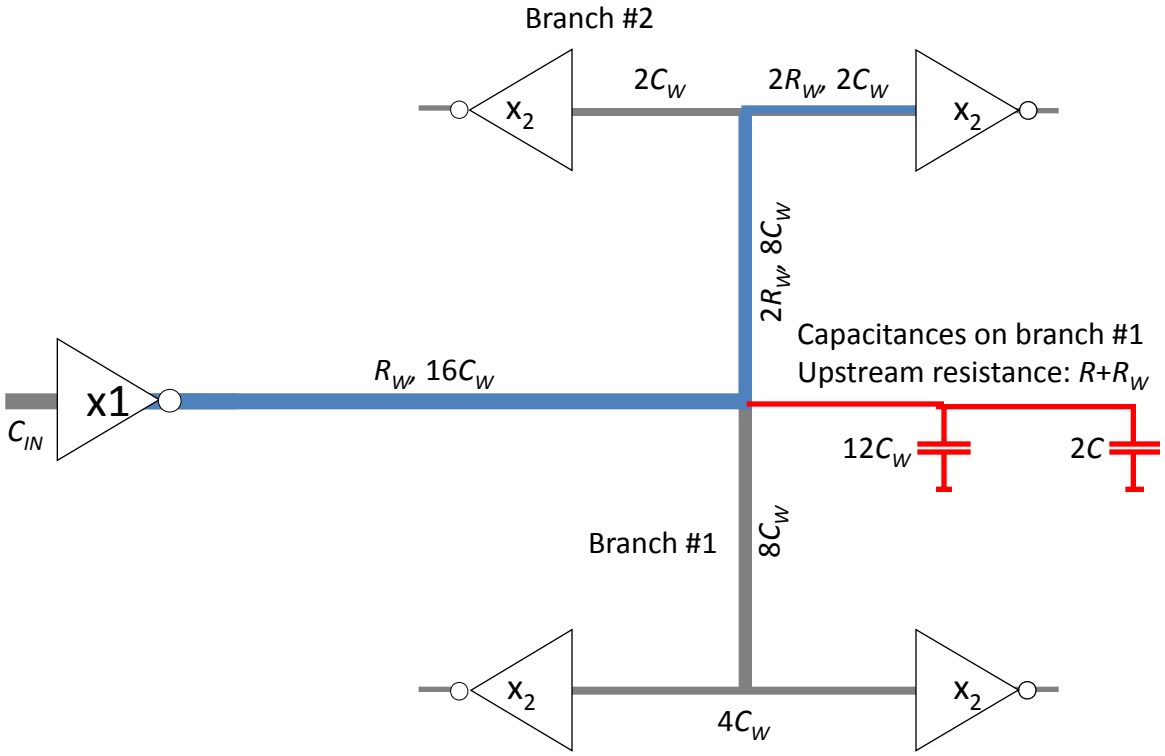

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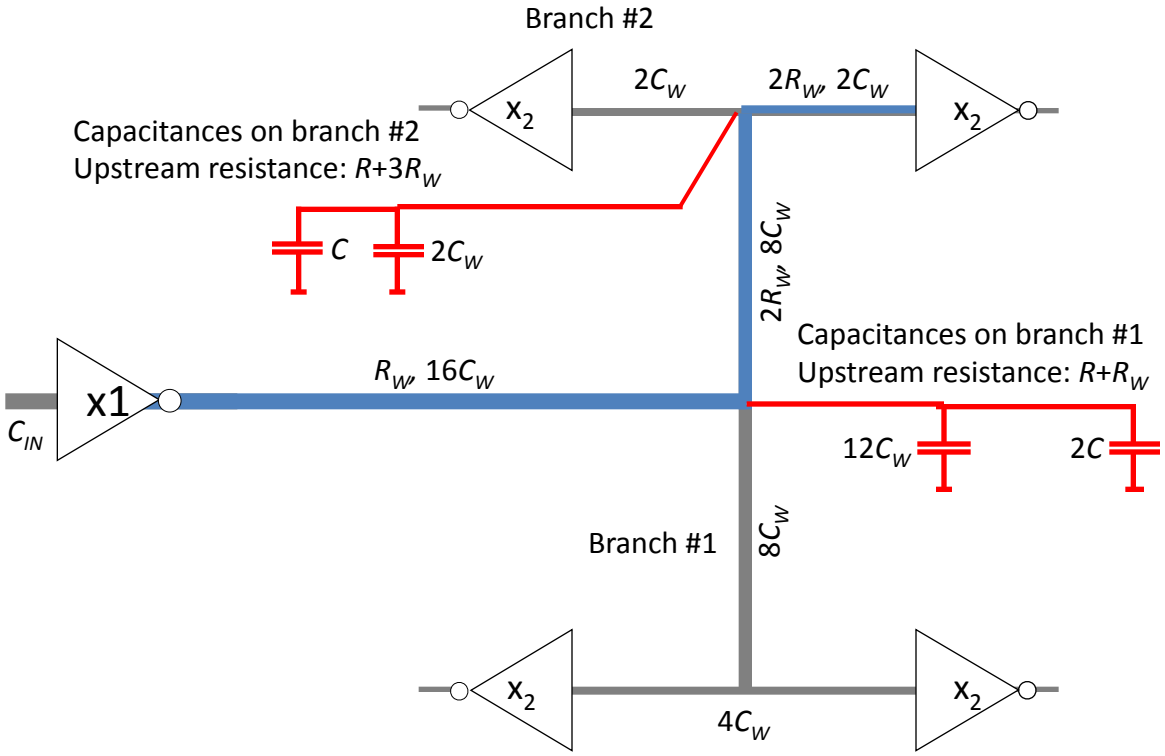

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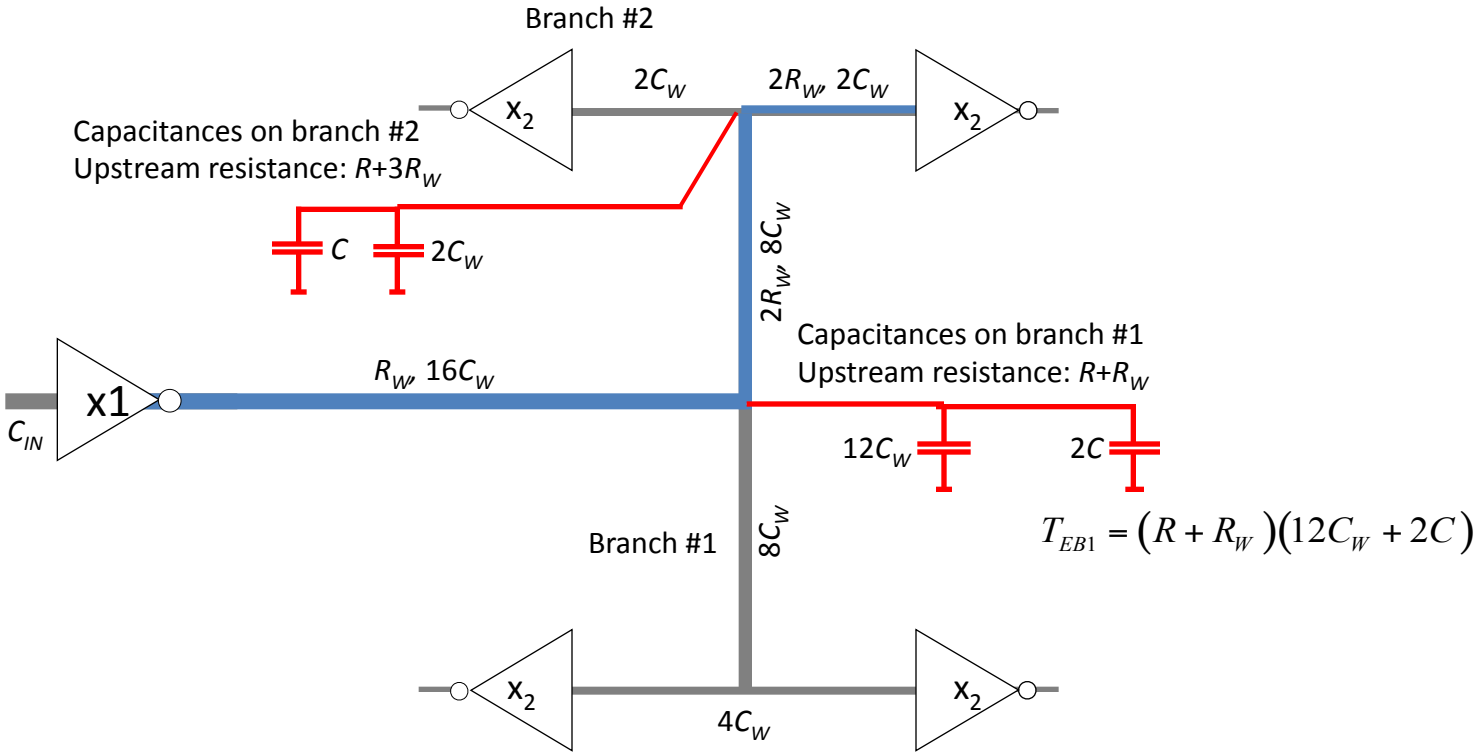

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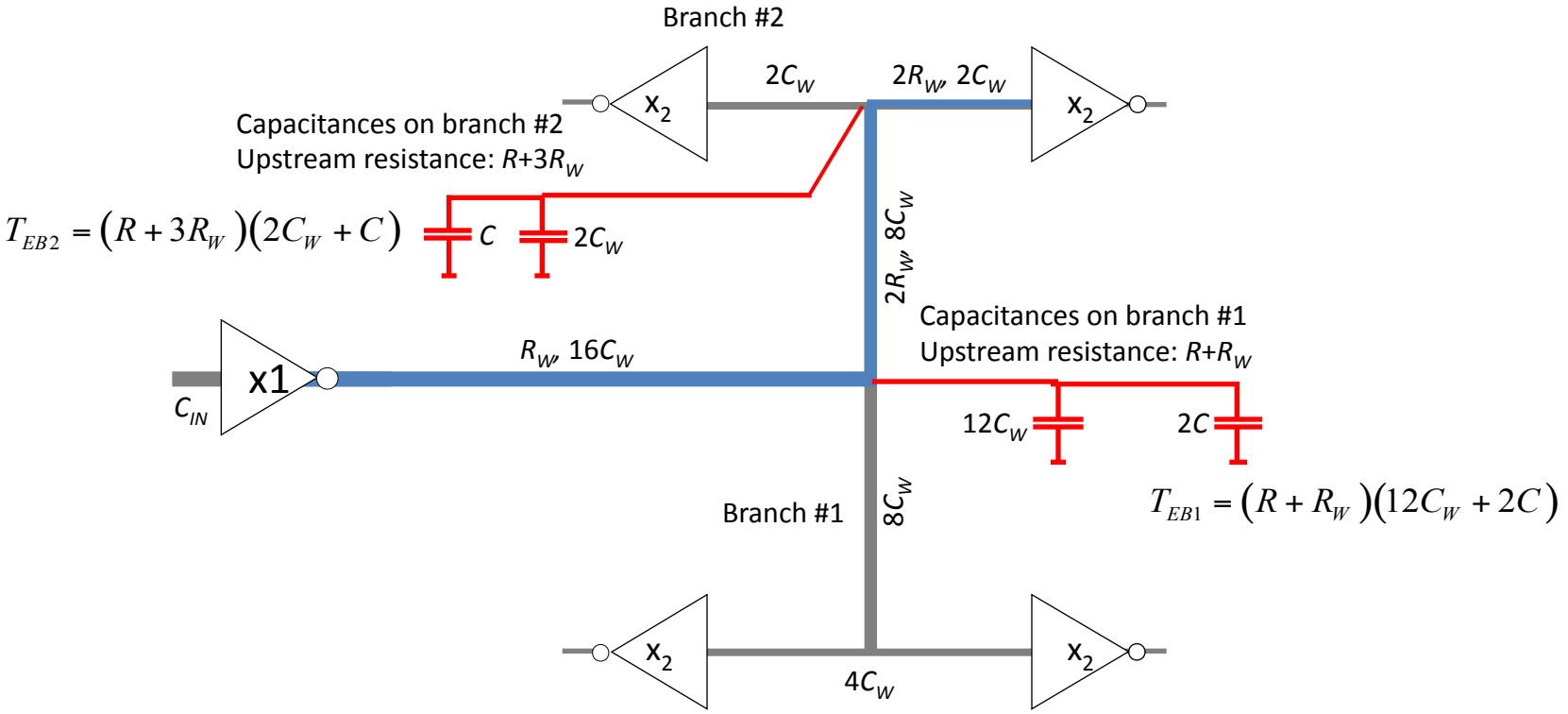

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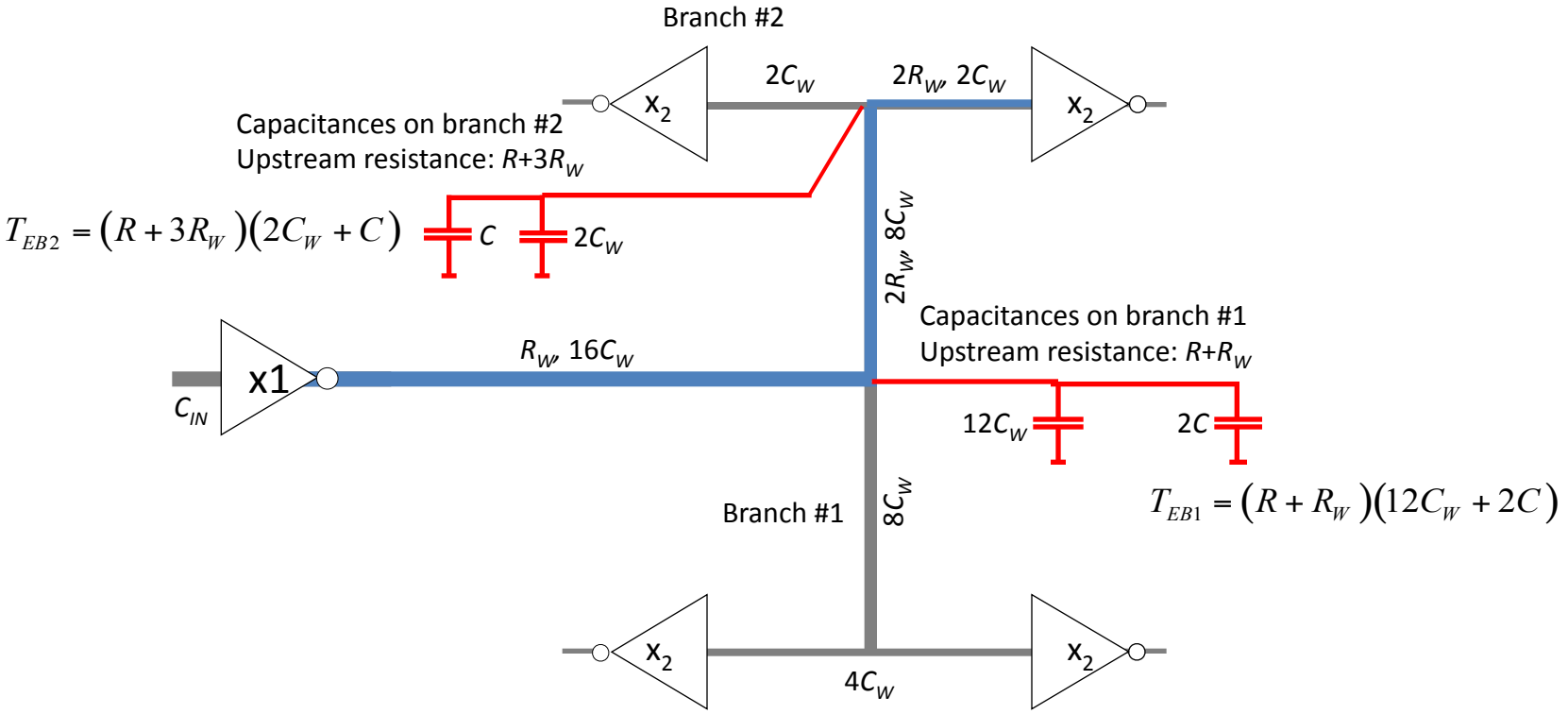


Branch contribution to Elmore time constant: $T_{E,branches} = 3RC + 14RC_W + 5R_WC + 18R_WC_W$

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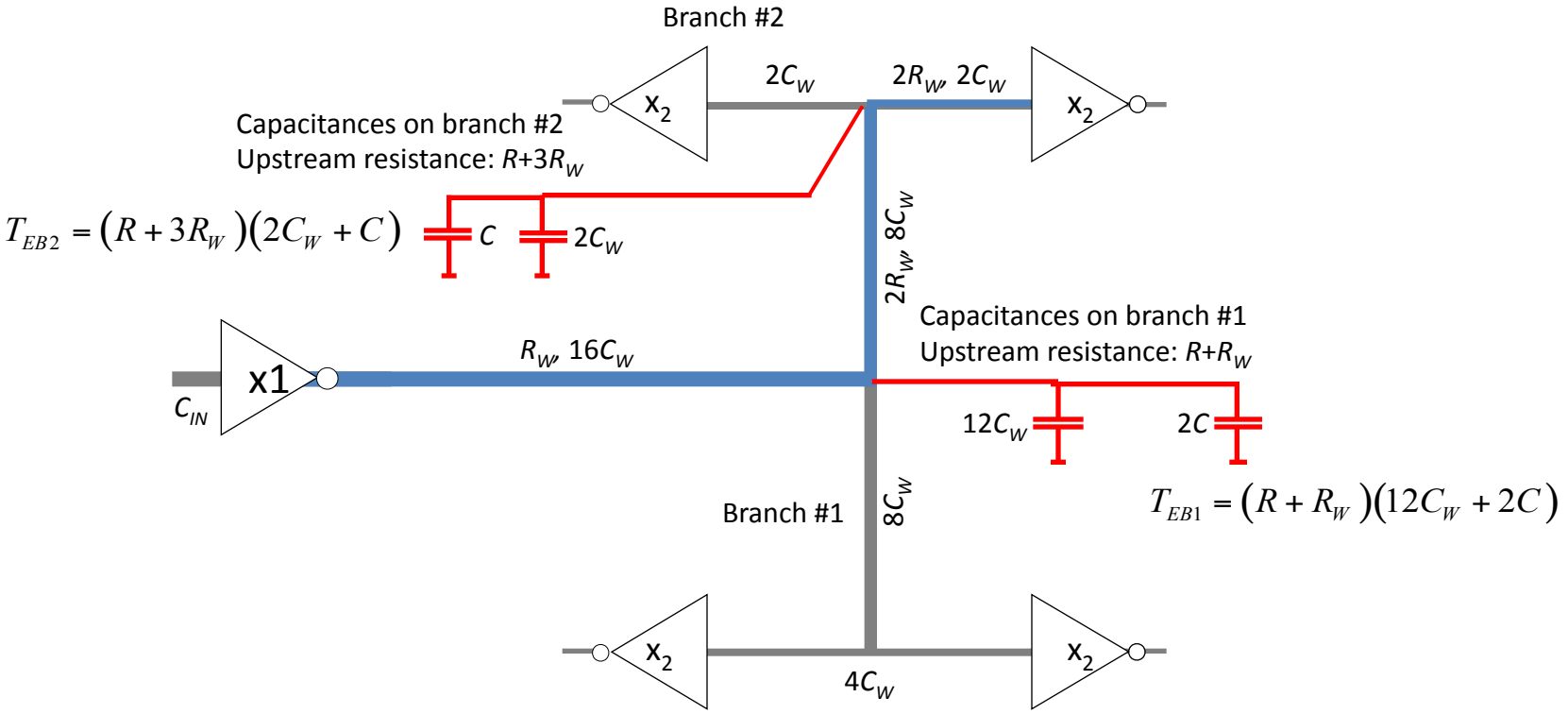


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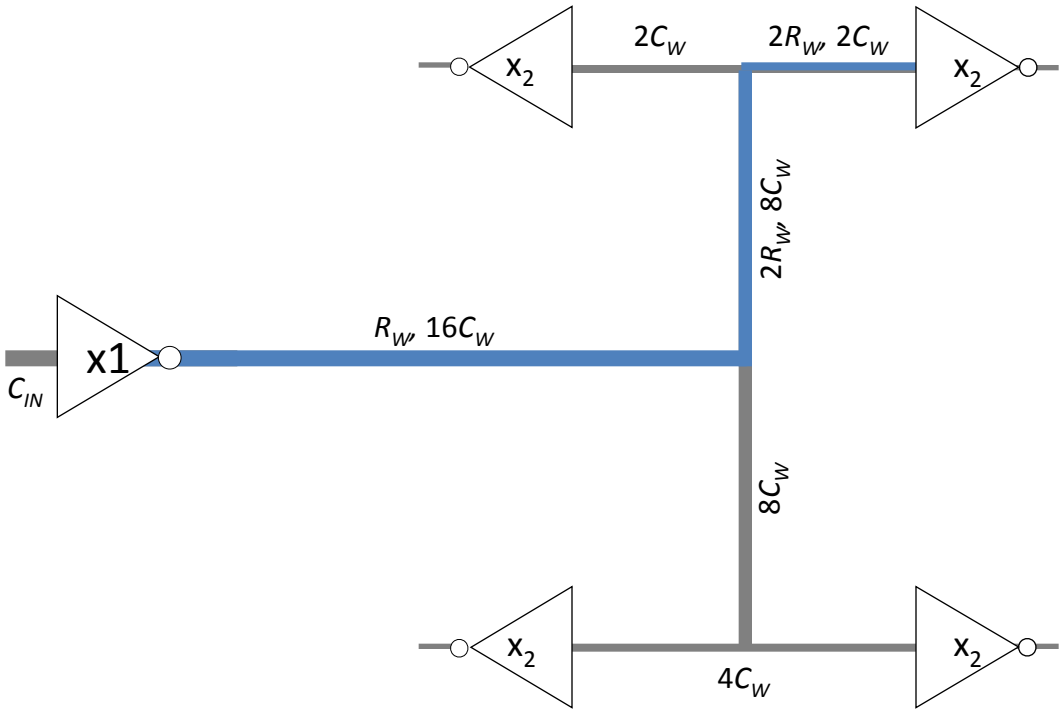
# Inverter sizing

How to size driver inverter to minimize the time constant, and hence the wire delay?

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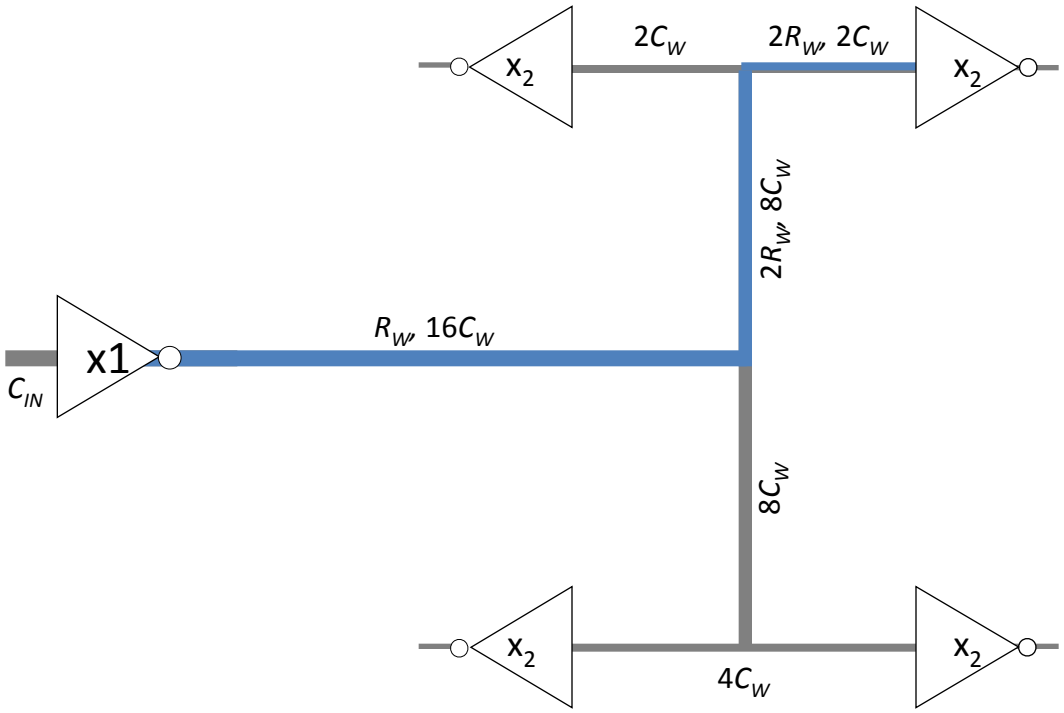
Normalize Elmore time constant: $$d = \frac{T_E}{RC} = p_{inv} + 4 + 40\frac{R_W C_W}{RC}\frac{R}{R_W} + 10\frac{R_W}{R} + 50\frac{R_W C_W}{RC}$$

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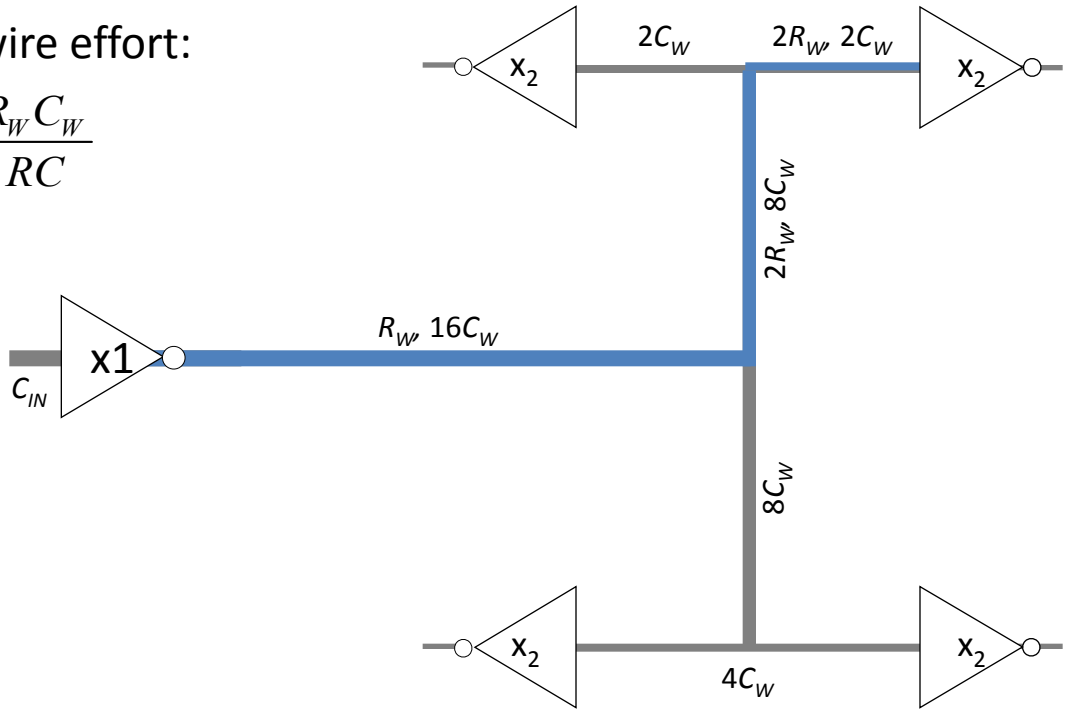


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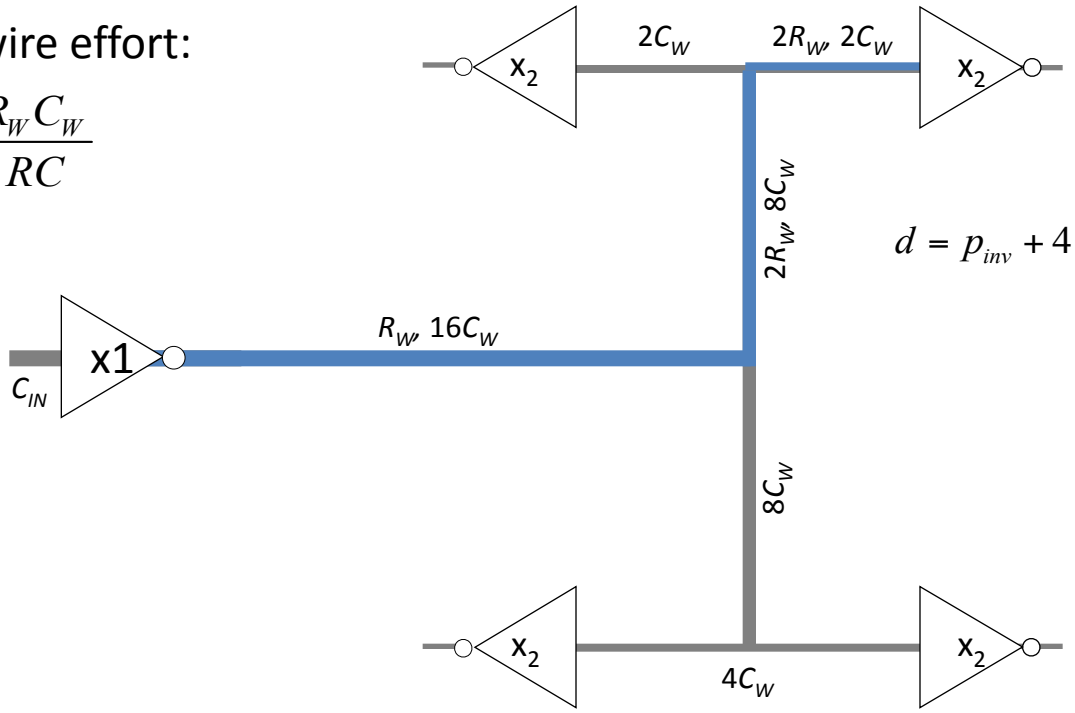


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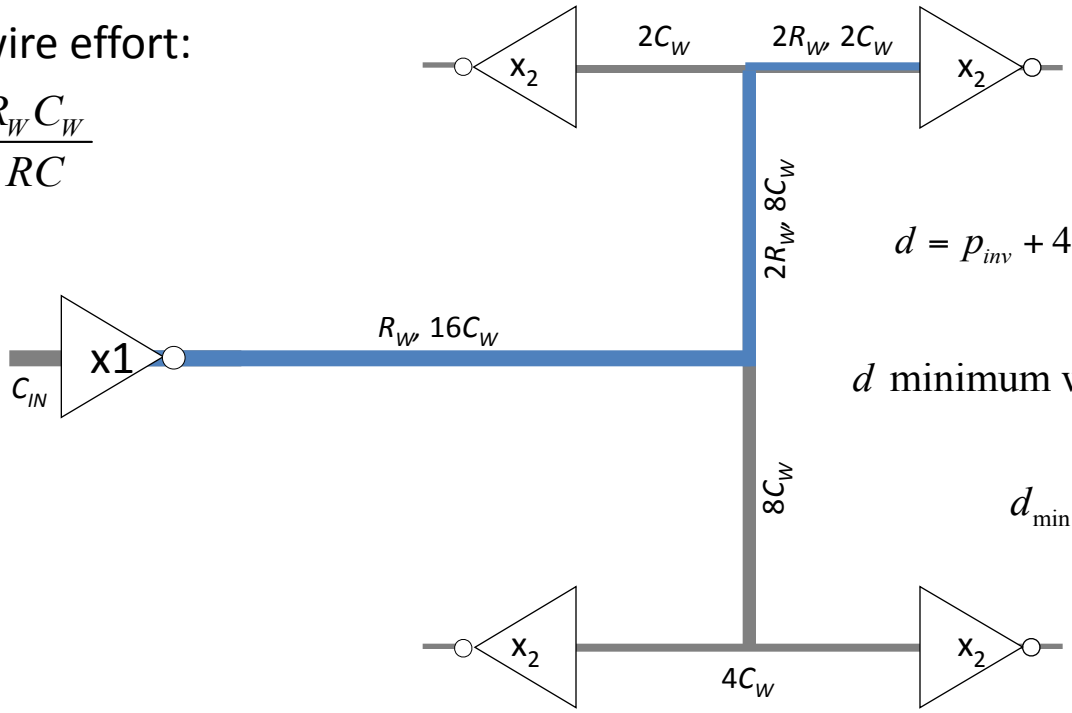


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$d$ minimum when $$\frac{\partial d}{\partial R} = 4\frac{W_E}{R_W} - 1\frac{R_W}{R^2} = 0$$

$$d_{\min} \text{ for } R = \frac{R_W}{2\sqrt{W_E}}$$

Total Elmore time constant: $$T_E = R\left(C_D + 4C\right) + 40RC_W + 10R_W C + 50R_W C_W$$

# Conclusion

We have learnt two things:

- The Elmore model – a generalized delay model
  - Relying on the existence of a dominating time constant
- How to handle the influence on delay of branches
  - Main timing path first, neglecting branches
  - Then consider branches neglecting any branch resistances only considering branch capacitances!

# Thanks a lot for listening!