On-chip interconnect

Lecture 9b on
Wire delay modeling and repeater insertion
Professor Kjell Jeppson
Tuesday October 2, 2018

Outline

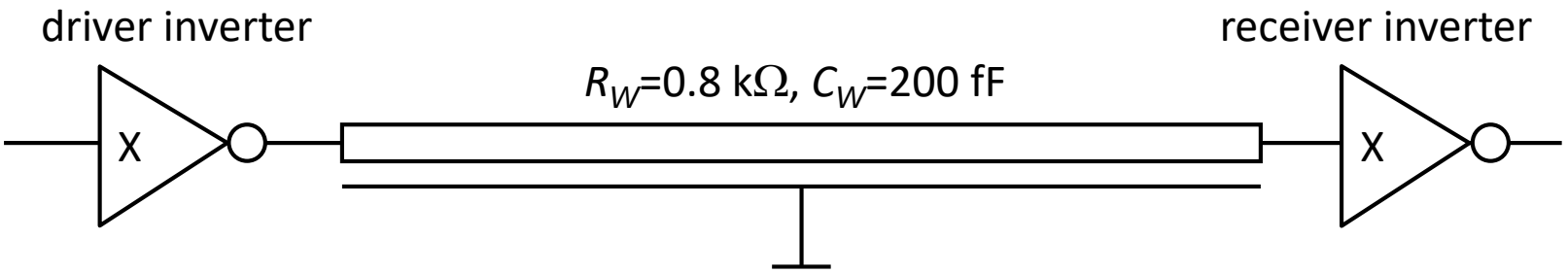
- Introduction
- Introduce a distributed RC π-model for delay estimates
  - Wire resistance per unit length *L*, *r*
  - Wire capacitance per unit length *L*, *c*
  - Distributed wire delay ~ $\frac{1}{2}rcL^2$
- For simplicity, assume the existence of a dominant RC time constant for describing the output signal at the wire end
- We will show how repeaters can be inserted to keep wire lengths short
  - Find the optimal number of repeaters for any wire length
  - Find the critical wire length for repeater insertion
- Introduce the concept of wire effort
- Conclusions

Wire delay example

Estimate the delay of an inverter driving an identical inverter at the end of the 1 mm wire! $W_P=2W_N$.

Assume wire cap c= 200 fF/mm, r=800 Ω/mm (from previous examples)

The wire will affect the propagation delay if the wire R_WC_W product is larger than the reference RC product of the inverter $R_{eff}C_G$=2 kΩ × 3.6 fF = 7.2 ps.



The given parameters yield a wire resistance of 800 Ω and a wire cap is 200 fF.
Wire resistance is distributed along the wire which must be modeled by segments
In Spice circuit simulations a 3-segment π-model is accurate to within 3%
However, for simple analytical estimate: use single segment π-model.

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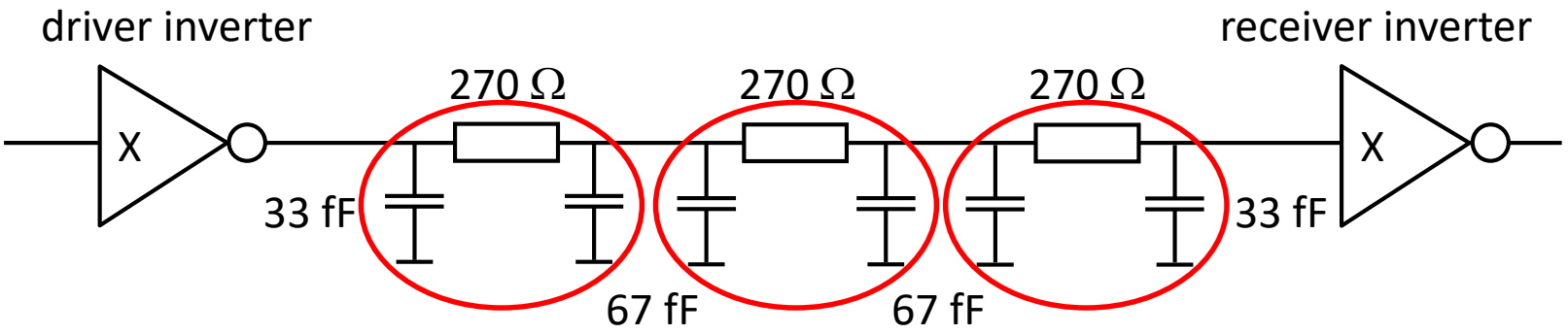

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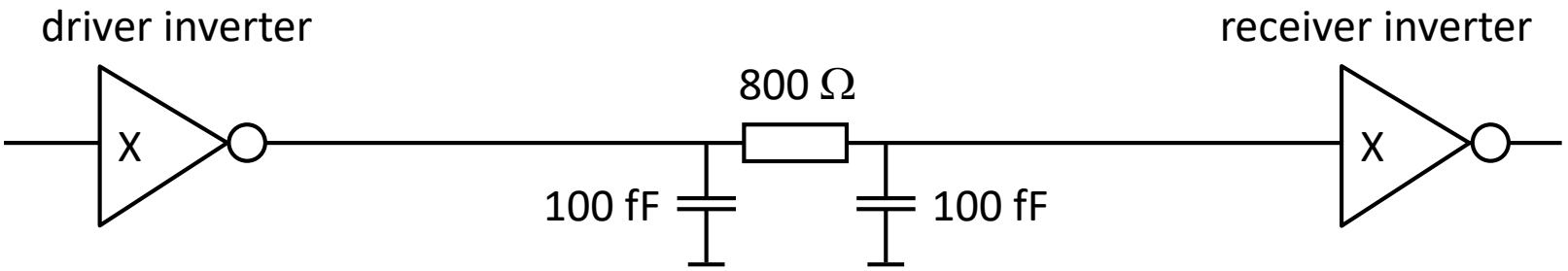

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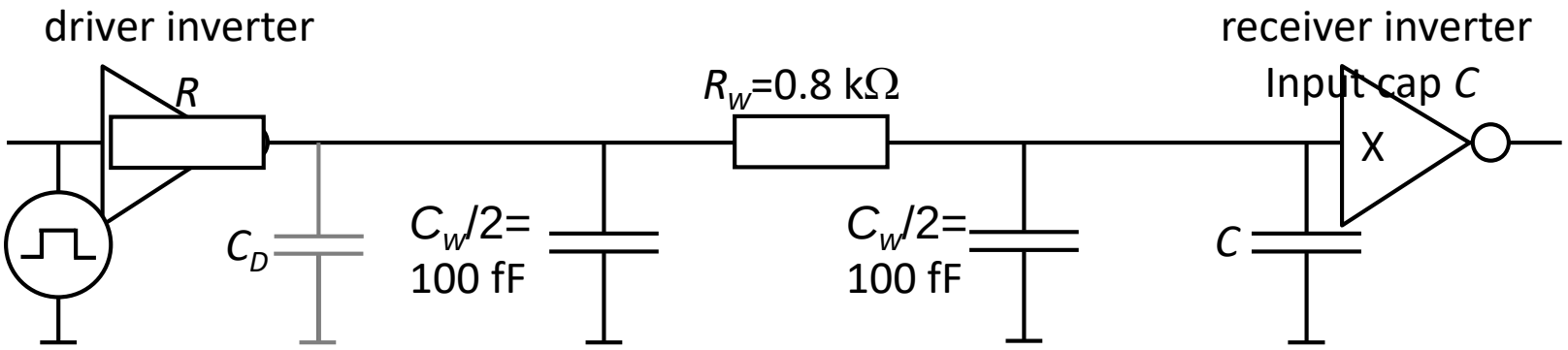


Wire π-model

Introduce electrical inverter models

What is the delay of this two-stage RC circuit?

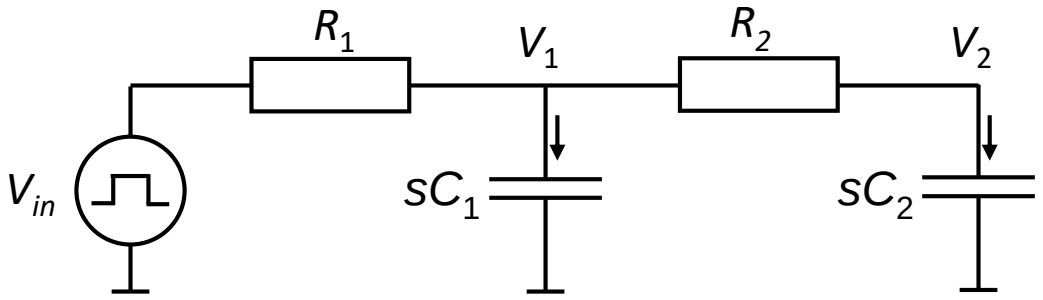
Can be found analytically from second-order differential equation!

Simplify wire circuit to find solution

Redraw the wire circuit as a two-stage RC circuit, where

Stage 1: resistance R_1 and capacitance C_1
Stage 2: resistance R_2 and capacitance C_2

- Get transfer function, or 2nd order linear differential equation



$$H(s) = \frac{1}{R_1 R_2 C_1 C_2 s^2 + \left(R_1\left(C_1 + C_2\right) + R_2 C_2\right)s + 1}$$

Most often one time constant is dominant, for the case of a falling output voltage resulting in $V_2(t) \approx V_{DD} \cdot e^{-t/\tau_E}$

Let´s denote the two solutions to the characteristic equation s_1 and s_2, respectively.

For the case of a falling output the solution is:

$$V_2(t) = V_{21}e^{s_1 t} + V_{22}e^{s_2 t}$$

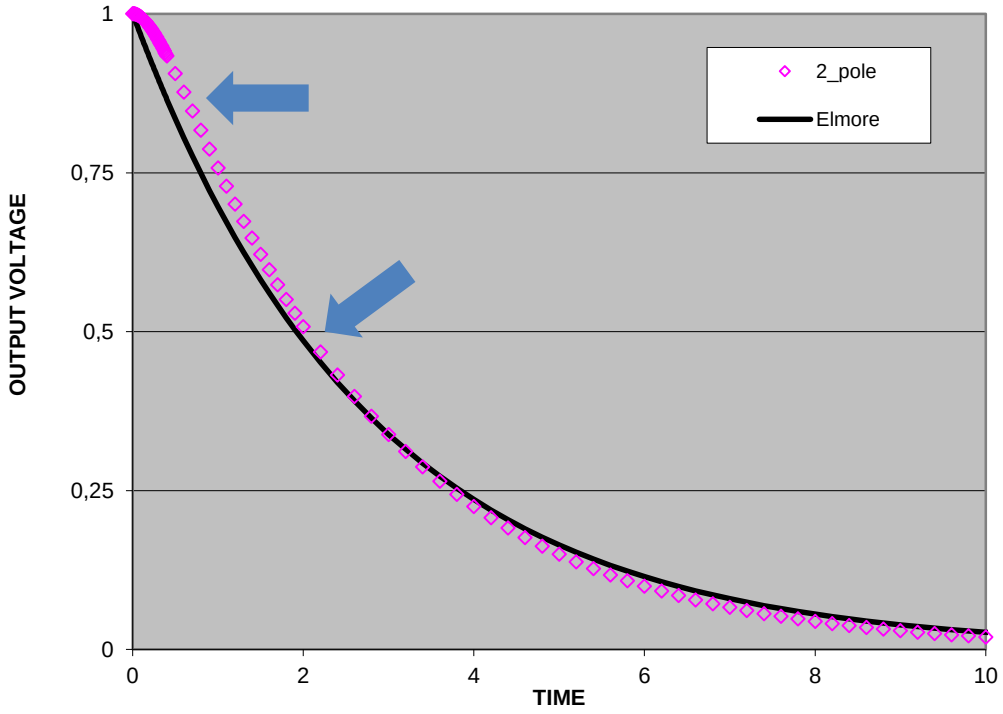
Characteristic eq. also yields sum of the two time constants

$$\tau_E = \underbrace{(-\tfrac{1}{s_1})}_{\tau_1} + \underbrace{(-\tfrac{1}{s_2})}_{\tau_2} = R_1\left(C_1 + C_2\right) + R_2 C_2$$

Propagation delay: $t_D = 0.7 \times \tau_E$

Approximative solution

Let´s have a look at a circuit example where R_1=0.8R_2, C_1=1.2C_2
Already for these 20% differences between R_1 and R_2, C_1 and C_2, respectively, one of the time constants become dominant, i. e. τ_1=2.45, τ_2=0.3
This graph compares the exact two-pole solution with the approximative exponential decay assuming a dominant time constant $\tau_E = \tau_1 + \tau_2$=2.75

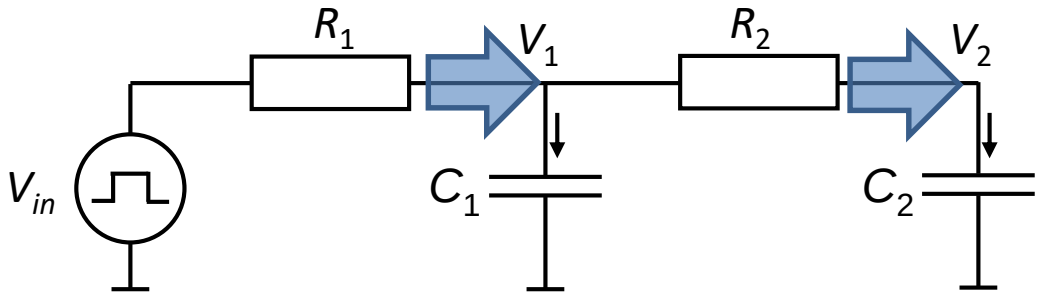


How to remember delay formula?

Estimate the delay of an inverter driving an identical inverter at the end of the 1 mm wire! $W_P=2W_N$.

Assume wire cap c= 200 fF/mm, r=800 Ω/mm (from previous examples)

- Now, let us return to the simplified two-stage RC circuit
- How to remember how to get the dominant time constant?



Each resistance is multiplied by its downstream capacitance!

$$\tau_1 = R_1\left(C_1 + C_2\right) + R_2 C_2$$

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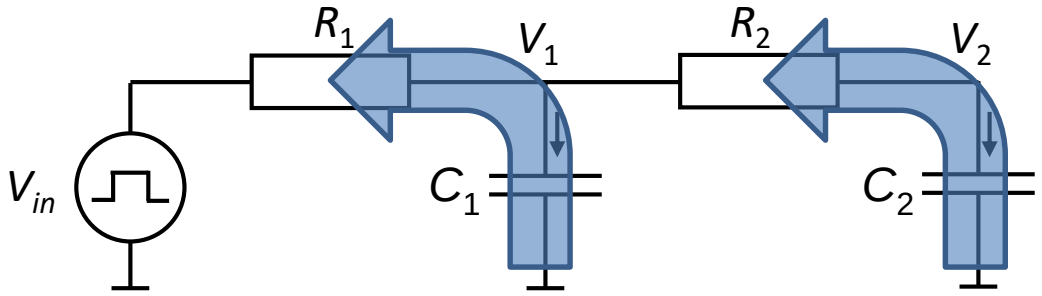

Or: Each capacitance is multiplied by its upstream resistance!

$$\tau_1 = R_1C_1 + (R_1 + R_2)C_2$$

Return to wire delay example

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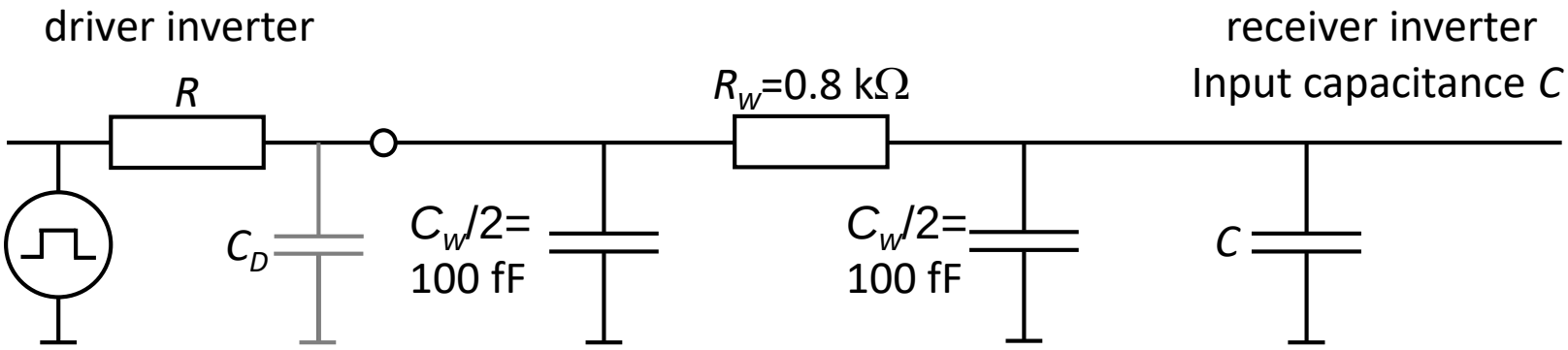

At this point, I have found it convenient to introduce the wire effort W_E: $W_E = \frac{R_W C_W}{RC}$

In our example, W_E=160/7.2≈22

and the normalized delay can be written $d = p_{inv} + 1 + W_E \frac{R}{R_W} + \frac{R_W}{R} + \frac{W_E}{2}$

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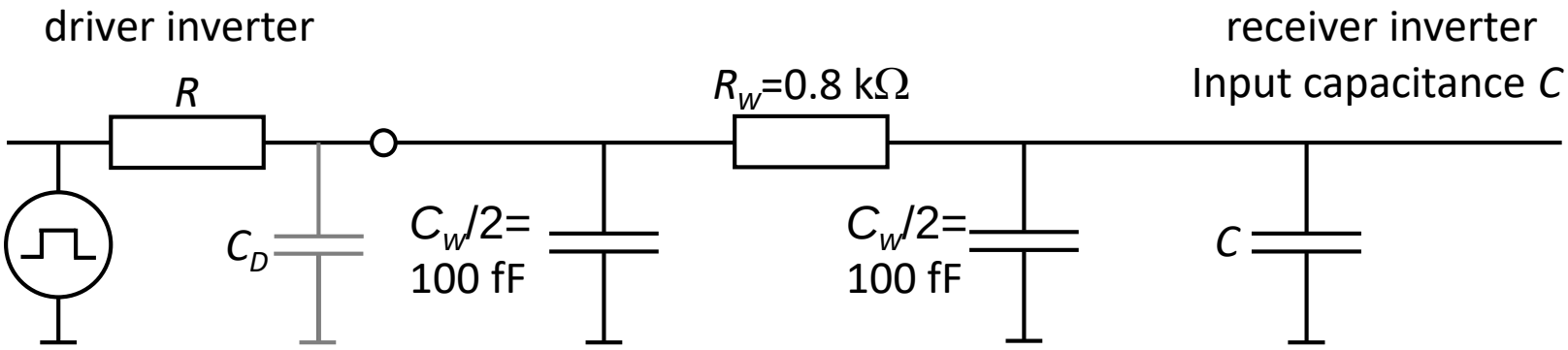

Having developed a delay model based on the assumption of a dominating time constant, let´s apply the model for finding the size of the inverter minimizing the delay!

$$\frac{\partial d}{\partial R}=\frac{W_E}{R_W}-\frac{R_W}{R^2}=0 \rightarrow R_{optimal}=\frac{R_W}{\sqrt{W_E}};\ R_W=0.8\ \text{k}\Omega,\ W_E=22 \rightarrow R_{optimal}=170\ \Omega$$

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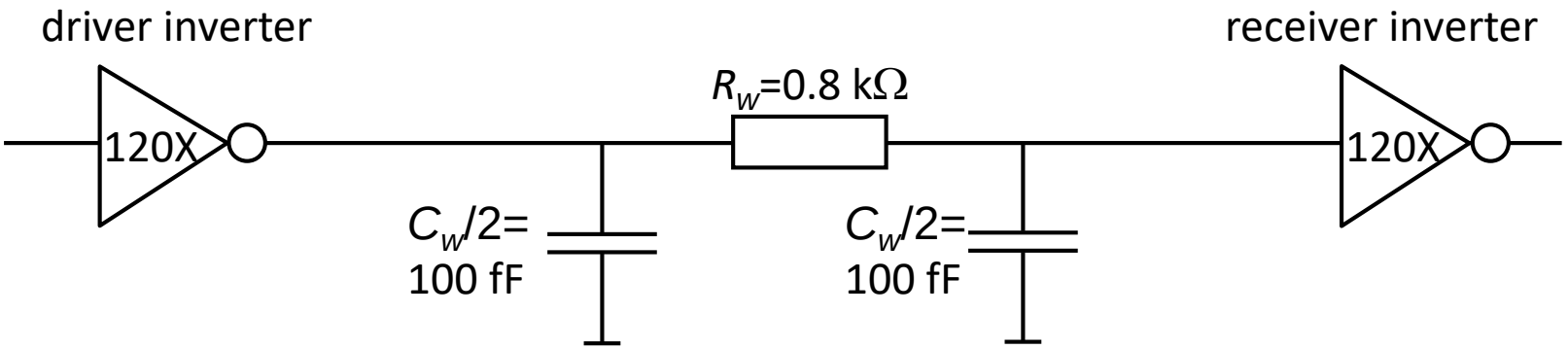
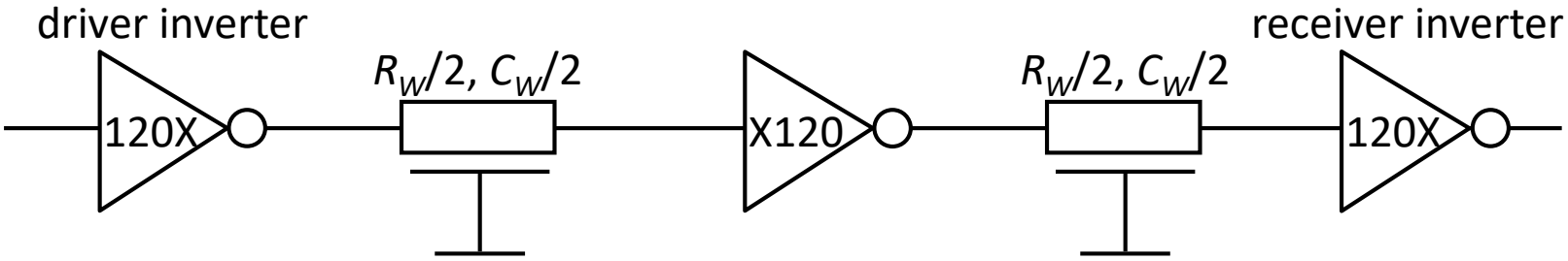


Having defined inverter size 10X for inverters with R=2 kΩ, 120X is the inverter size with R_{eff}=170 Ω minimizing the delay caused by the wire.
Total delay becomes 22.5 multiples of the basic 5 ps that we have defined for the 65 nm CMOS process, i.e. 112.5 ps, a value to be compared to the 10 ps with no wire.

Keeping wires short using repeaters

For keeping wires short, what if we divide the wire in the example into 2 segments by inserting a repeater in the middle?

A repeater is just an identical inverter that we call repeater!
To estimate the propagation delay, just add the two segment delays!



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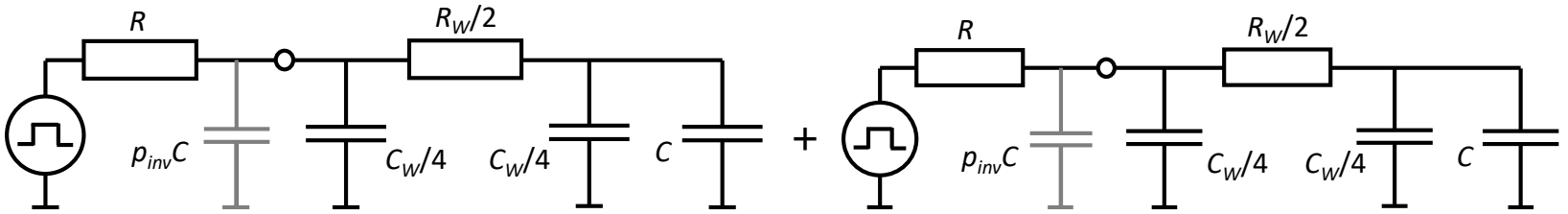


If we keep the total wire effort W_E=22, the sum of the two stage delays is

$$d = 2\times\left(\underbrace{p_{inv}+1}+\frac{W_E}{4}\frac{R}{R_W/2}+\frac{R_W/2}{R}+\frac{W_E/4}{2}\right)$$ (Using delay Eq. on slide 8)

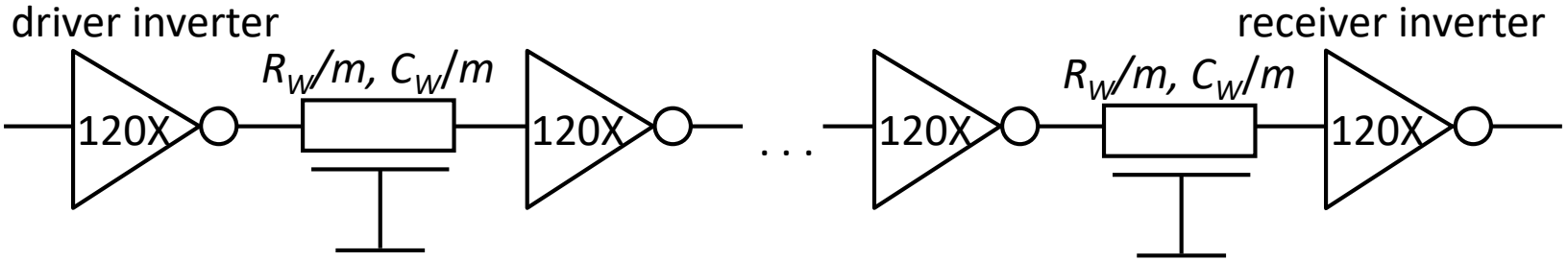
Keeping $R_{eff}=R_{opt}=\frac{R_W}{\sqrt{W_E}}$ ➡ $d_{\min}=2\times\left(2+\sqrt{W_E}+\frac{W_E}{8}\right)=2\times(2+2.35+2.35+2.8)=19$

Just a small decrease of the wire delay (from 22.5 to 19)! But still . . .

Keeping wires short using repeaters

But what if the wire is much longer, say 10-15 mm?

What would be the optimal number of segments, *m,* into which the wire should be split by inserting *m*-1 identical repeaters for minimizing the delay?



If we keep W_E as the total wire effort, the delay can be written

$$d = m \times \left(\underbrace{p_{inv}} + 1 + \frac{W_E}{m^2}\frac{R}{R_W/m} + \frac{R_W/m}{R} + \frac{W_E}{2m^2} \right) \Rightarrow m_{opt} = \sqrt{\frac{W_E}{2\left(p_{inv}+1\right)}} = \frac{\sqrt{W_E}}{2}_{p_{inv}=1}$$

The previous inverter sizing is still optimal, since the two middle terms yielding the relationship between *R* and R_w are independent of *m*!

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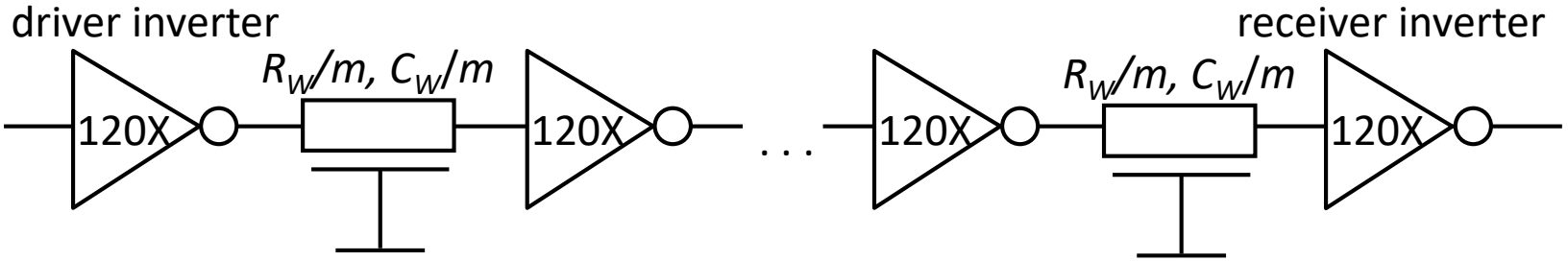


What is the critical wire length for considering repeater insertion?

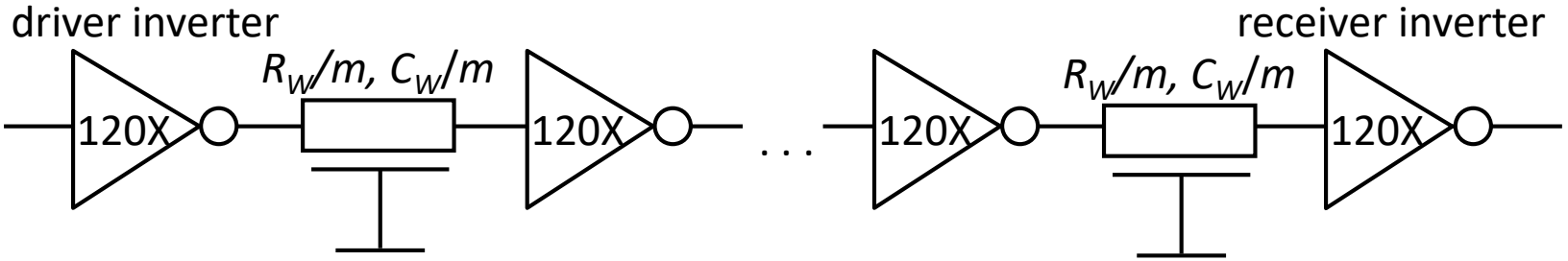
$$L_{crit} = \frac{L}{m_{opt}} = \frac{2L}{\sqrt{W_E}} = 2\sqrt{\frac{RC}{rc}} = 2\sqrt{\frac{7.2}{160}} = 0.42 \text{ mm}$$

Hence, in the case of our 1 mm wire example, it´s optimal to divide wire in two segments. However, the gain was small and the signal became inverted

Example: 10 mm wire

But what if the wire is much longer, say 10 mm?

The critical length being 0.42 mm suggests insertion of 22 repeaters, i.e. that we should divide the wire into 23 segments.



The wire effort is now W_E=16000/7.2 ≈ 2200
Hence, minimum normalized delay is 4√W_E=188≈190.
Summarizing the 23 stage delays gives the same result:

$$d = 23\times 2 + 2\sqrt{W_E} + \frac{W_E}{46} = 46 + 2\times 47 + 48 = 188 \approx 190$$

Important comment: An even number of repeaters does not invert the signal!

Conclusion

- Introduced a distributed wire RC model, the π-model
- Discussed the relevance of a delay model assuming the existence of a dominant time constant
- Understood that wires should be kept short since wire delay or flight time, increases with the wire length squared!

$$W_E = \frac{rcL^2}{RC} \sim L^2 \text{ ! Therefore, keep wires short!}$$

- For long wires, delay can be minimized by inserting repeaters
- We have derived expressions for the optimal number of segments, m_{opt}, and for the critical wire length L_{crit}
- $$L_{crit} = \frac{L}{m_{opt}} = 2\sqrt{\frac{(RC)_{inverter}}{(rc)_{wire}}}$$