Written examination in **Integrated Circuit Design MCC091**

Monday August 25, 2014, at 14.00-18.00 in the VV-building

Staff on duty: Lena Peterson, D&IT, phone ext: 1822, or mobile 0706-268907. Will visit around 14.30 and 17.00.
Administration: Send exams to Lena Peterson D&IT, and send lists to Jeanette Träff, MC2/Photonics.

Technical aids for students: None, this is a closed-book, no-calculator examination.
The results from the examination will be sent to you via the Ladok system within three weeks. The reviews of this exam will take place Monday September 8, 12.30-13.00 and Tuesday Sept 9, 12.00-13.00 in room 4128 at the CSE department. Solutions will be posted on the course web site in PingPong directly after the examination. Any student who does not have access to the 2013-2014 PingPong page can contact Lena Peterson (via e-mail to lenap@chalmers.se) to obtain the solution.

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The written examination contains six problems, each worth 10 points. You need 30 points to pass, 40 points for grade "4" and 50 points for grade "5". Any bonus points from the fall 2014 course instance will be included for the higher grades.

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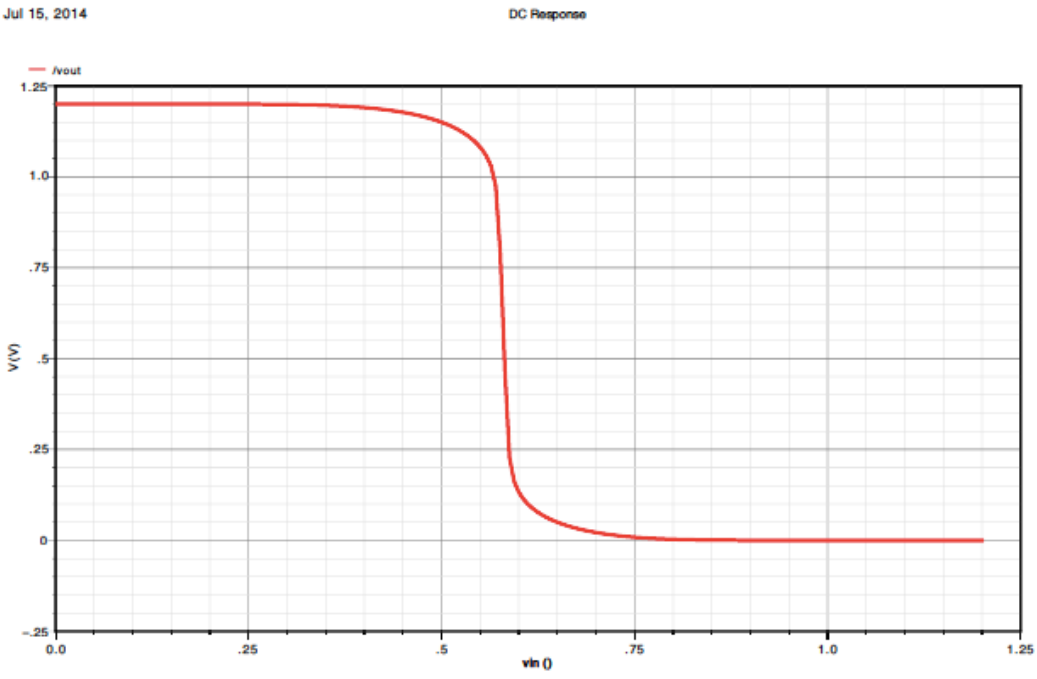
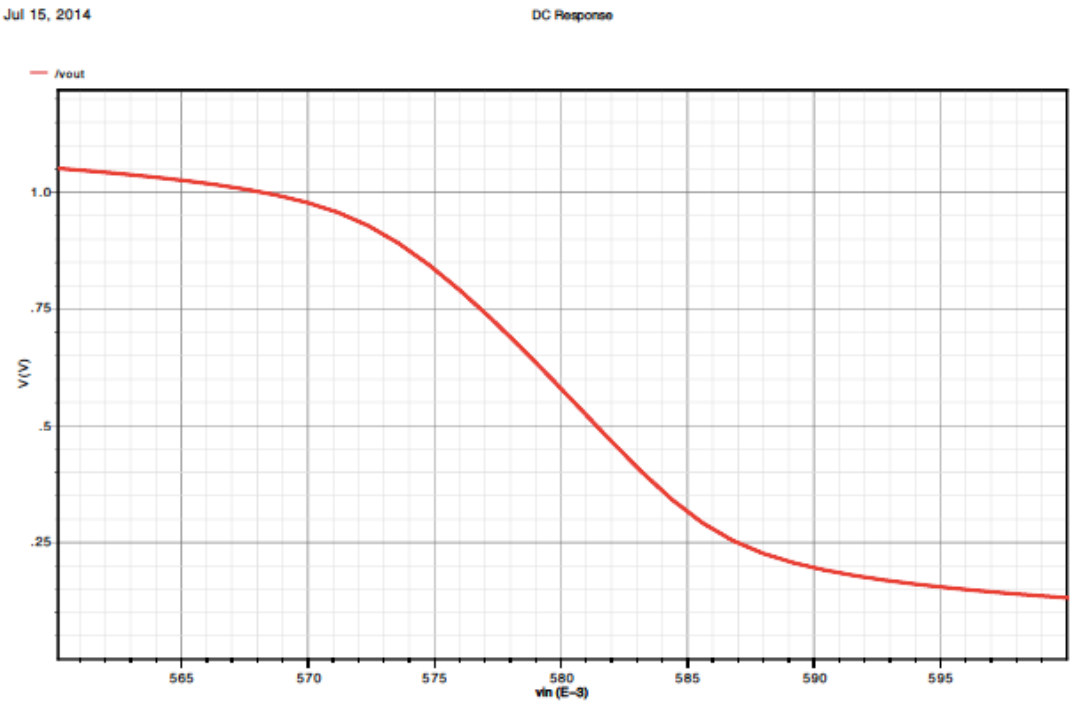
1. **Inverter switching voltage and gain.** Below is the voltage transfer curve from a simulation of a CMOS inverter such as the one you investigated in lab 1. On the next page you will find a more detailed view of the steepest part.



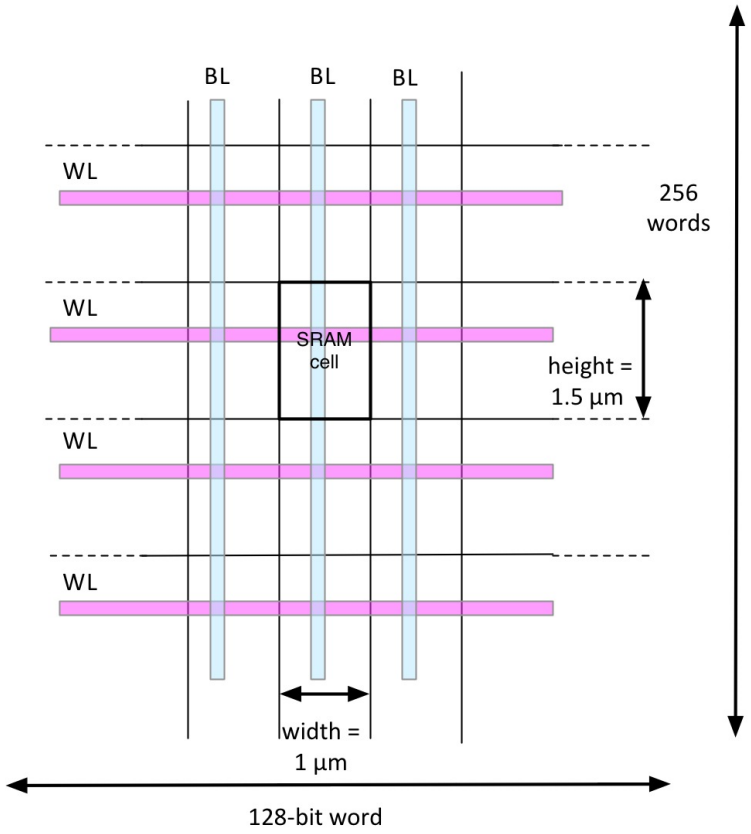


a) What is the inverter's switching voltage as determined from the curve? (2 p)
b) What is the small-signal voltage gain of the inverter at the switching voltage as determined from the curve? (2 p)
c) What if we make both the p and n transistors two times as wide and two times as long? Would the gain change then? If it would change, would it increase or decrease? Assume that the long-channel quadratic current equations hold. Motivate your answer. (2 p)
d) Repeat c) if we make the transistors just two times as **long**? (2 p)
e) Repeat c) if we make the transistors just two times as **wide**? (2 p)

f) **(Bonus question)** If we assume long-channel transistor equations with ideal channel-length modulation, how large would the changes in gain be in your answers for tasks c-e? (2 p)

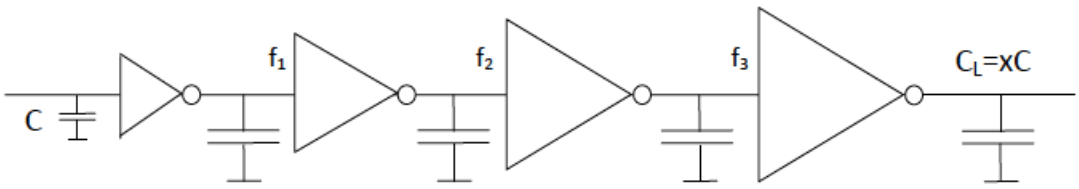
2. Wire models, delay and energy. On the next page is the general layout of a static random-access memory (SRAM). The word lines (WL) select the particular word that is to be read or written. The bit lines (BL) carry the bit values out when reading and supply the bit values that are to be written when writing. The bit lines are routed in metal 1 (blue) and the word lines are routed in metal 2 (purple). In each memory cell the word line is connected to two minimum-size nMOS transistors for accessing that particular memory cell.

A word line is 0.1 µm wide, which is the minimum width for an metal-2 wire in this particular process. A word line has a capacitance of 0.1 fF/µm to ground and an inter-wire capacitance to one adjacent word line of 0.02 fF/µm and the M2 layer has a resistance of 0.1 Ω/□. A minimum-size nMOS transistor has a gate capacitance Cg = 0.1 fF. V_{DD} is 1 V.

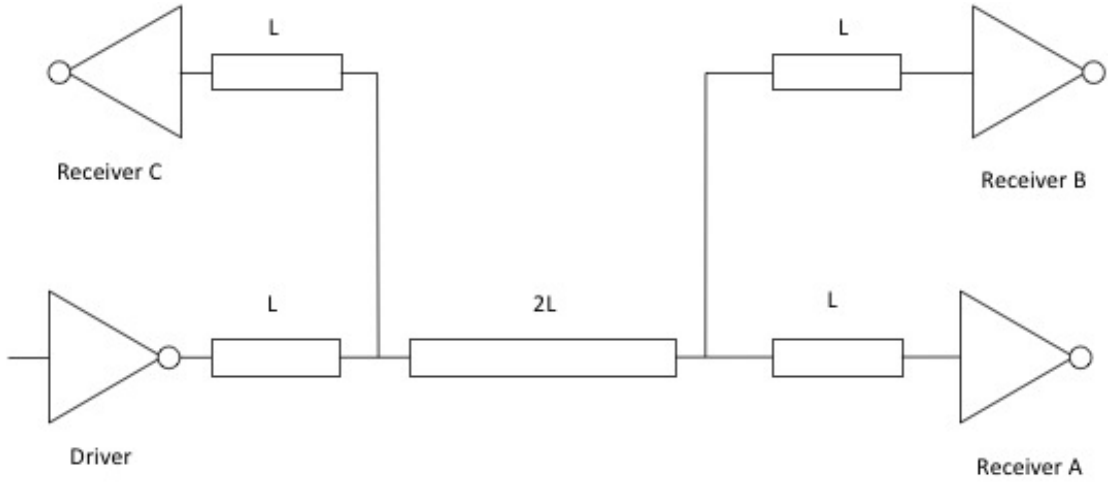


a) Calculate the resistance for one WL. (1 p)
b) Calculate the total capacitance for one WL including the capacitance of the access transistors. (1 p)
c) Draw a circuit diagram for the WL and the inverter that is driving it. Assume the driver is an inverter with the same equivalent resistance as the WL resistance. Calculate the delay. For simplicity neglect the parasitic capacitance of the driver. (2 p)
d) Calculate the energy required for accessing the memory when reading the memory once. (2 p)
e) Estimate what would happen to the delay and energy computed in c) and d) if one could make the memory cells half as high and half as wide. Assume that the inter-wire capacitances are pure plate capacitances and the driver is re-sized so that its equivalent resistance still is the same as that of the wire. Reflect on the result. (4 p)

3. Driving large capacitances Show, by deriving the optimal solution, that the optimal solution for the case below when driving a large capacitive load is that all the tapering factors should be the same. Specifically, you should show that the optimal solution in the case below is f1=f2=f3= $\sqrt[4]{x}$. (10 p)



4. **Wire delay with branching** In the clock network on a chip there is a driver driving three receivers over a number of wire segments as shown in the figure below:



The driver and the three receivers are identical. They all have an equivalent resistance which is R, an input capacitance which is C and an output capacitance which is pinv*C. A wire of length L has a total resistance that is R/4 and a total capacitance that is 2C.

a) Calculate the delay from the driver to receiver A. (4 p)
b) Calculate the clock skew between receivers B and C. (4 p)
c) Suggest a new wiring arrangement that makes the clock skew derived in b) equal to 0 while keeping the delay from the driver to receiver A the same as the one calculated in a). (2 p)

5. **Prefix adders, compound gates and logical effort**. Prefix adders can be designed in countless ways and many researchers have tried to improve them over the years. In the 80's Ling came up with a way simplify the circuitry in the generate path at the expense of one additional XOR gate in the sum calculation. Further extensions on Ling's approach are employed in many of today's microprocessors.

In a Ling adder one computes a signal called "pseudogenerate", which we denote H, rather than the signal "generate", G, which we have used in all prefix adders discussed in class. The main advantage of Ling's approach is that the first row in the prefix network is simpler to implement and that part of the setup network can be eliminated. The rest of the prefix network remains the same.

The logical function for the 2-bit pseudogenerate function H2:1 is H2:1= G2 + G1 = A2B2 + A1B1 where A1, B1, A2 and B2 are bits from the adder inputs.

a) Draw the transistor diagram of a static CMOS gate that computes the inverse of the function H2:1 from A1, B1, A2 and B2. (2p)
b) Calculate the logical effort, g, for this gate's four inputs and also the gate's parasitic delay, p. Assume that the ratio between the gate capacitance and diffusion capacitance in the particular CMOS process is pinv and that the transistors are scaled so the worst-case resistance of all paths are the same. You may also assume that the pMOS transistor is twice as wide as the nMOS transistor in the reference inverter. (2p)

The corresponding static gate for computing the regular G2:1 inverse is more complex. Usually, that computation is done in two steps, where the 1-bit G signals for each bit of the two input numbers are computed in the setup stage and the resulting G signals are used as the inputs to the G2:1 gate in the prefix network. But here we show a compound gate that computes the 2-bit G signal in one step from the adder inputs A1, A2, B1 and B2:

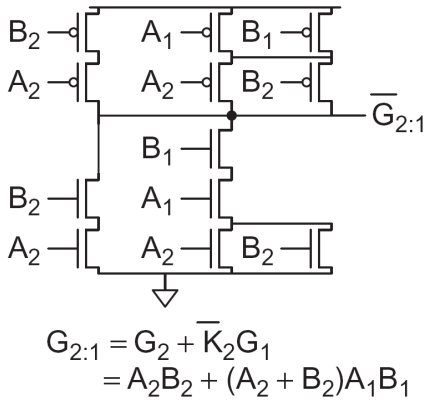


Figure 1: The 2-input generate gate from Weste & Harris figure 11.36 (a).

c) Calculate the logical effort, g, for all inputs of the G2:1 gate in Figure 1 above and the parasitic delay, p, for the gate. Use the same assumptions as in task b). (4 p)
d) Ling's approach can be incorporated in any type of prefix adder. As mentioned, the rest of the prefix network remains the same. With Ling's approach the sum calculation requires two XOR gates rather than the one XOR gate in regular prefix adders, but only one of them is the critical path. Reason about when it would make sense to use Ling's approach. (2 p)
e) **(Bonus question)** In Weste & Harris there is also a circuit diagram for the 3-input pseudogenerate static CMOS gate, which is shown below. But there is one typo in the figure. What is the typo? (2 p)

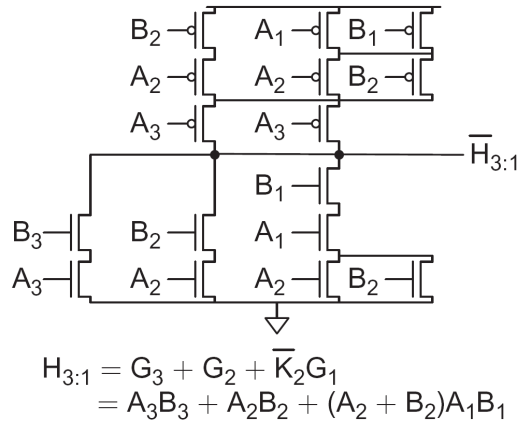
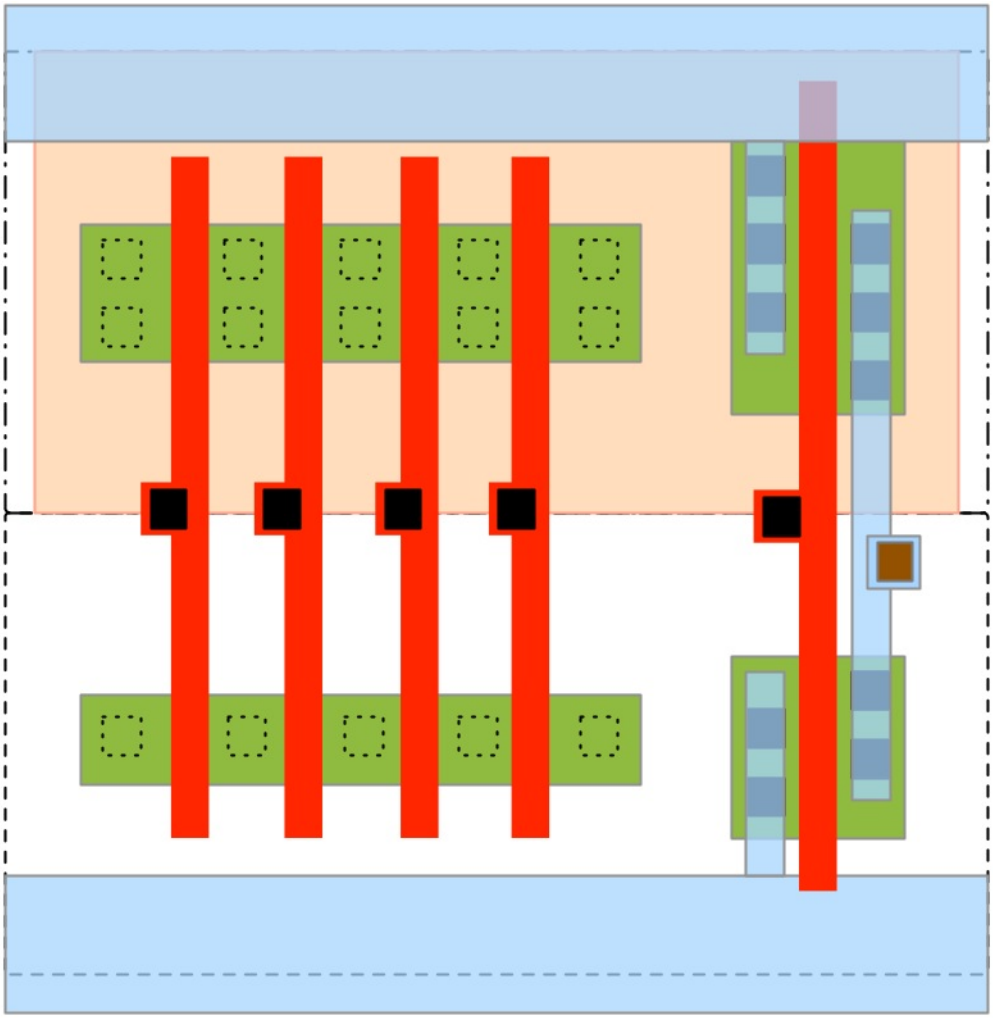


Figure 2: The 3-input pseudogenerate static CMOS gate from figure 11.37 (a) in Weste & Harris.

6. Layout of standard cell Your task is to use the attached standard-cell layout template to draw the layout of a logic H2:1 cell, where H2:1= A2B2 + A1B1, and where A1, B1, A2 and B2 are the input bits. If you have solved problem 5a you already have the circuit schematic. Your goal is to minimize the output parasitic capacitance of the compound gate. To reach this goal you may have to change the ordering of the transistors. If you do so, draw the modified circuit diagram on your solution sheet. Tear off the attached template and hand it in with your solutions! (There are two copies template sheets in case you make a mistake).

STANDARD-CELL LAYOUT TEMPLATE FOR H2:1 CELL **Exam number:_____**

Label all poly lines, except the inverter one. If you have changed the circuit diagram from your solution to problem 5 a) redraw the circuit diagram below the layout.



STANDARD-CELL LAYOUT TEMPLATE FOR H2:1 CELL **Exam number:_____**

Label all poly lines, except the inverter one. If you have changed the circuit diagram from your solution to problem 5 a) redraw the circuit diagram below the layout.