Written examination in **Integrated Circuit Design MCC091**

Friday October 31, 2014, at 14.00-18.00 in Hörsalsvägen lecture halls

Staff on duty: Lena Peterson, D&IT, phone ext: 1822, or mobile 0706-268907. Will visit around 14.30 and 16.45.
Administration: Send exams to Lena Peterson D&IT, and send lists to Susannah Carlsson, MC2.

Technical aids for students: This is a closed-book, no-calculator examination.
The results from the examination will be sent to you via the Ladok system within three weeks. The reviews of this exam will take place Monday November 17, 12.30-13.00 room 4128 at the CSE dept and Tuesday Nov 18, 12.30-13.00 in Lena's office. Solutions will be posted on the course web site in PingPong shortly after the examination. Any student who does not have access to the 2014-2015 PingPong page can contact Lena Peterson (via e-mail to lenap@chalmers.se) to obtain the solution.

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The written examination contains six problems, each worth 10 points. You need 30 points to pass, 40 points for grade "4" and 50 points for grade "5". Any bonus points from the fall 2014 course instance will be included for the higher grades.

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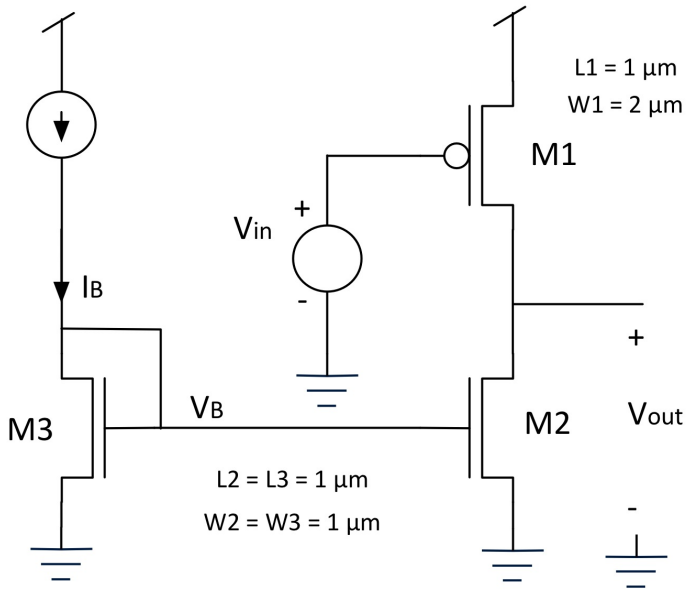
1) Power consumption The power consumption of a CMOS inverter can be minimized through circuit optimizations. How should each parameter in the table below (which is also repeated at the end of the exam on a separate sheet that you can turn in with your answer sheets) be changed to reduce the three different components of the inverter power consumption? For each parameter indicate **I** for increase, **D** for decrease or **N** for does not affect this type of power consumption. (10 p)

Goal	**Circuit parameter to optimize**	**I** (Increase**), D** (Decrease) or **N** (does Not affect)
Minimize the dynamic power consumption due to the charging and discharging of the capacitive load C_L.	V_{DD}	
	C_L	
	Transistor threshold voltages $\|V_T\|$	
	Transistors widths (first order)	
Minimize the power consumption due to short-circuit current during transition (assume a fixed rise and fall time at the inverter input).	V_{DD}	
	C_L	
	Transistor threshold voltages $\|V_T\|$	
	Transistors widths	
Minimize the static power dissipation, that that is the power due to the transistor leakage currents.	V_{DD}	
	C_L	
	Transistor threshold voltages $\|V_T\|$	
	Transistor widths	

2) **Amplifier large and small signal analysis** In the figure below is an amplifier with an active load where the gain pMOS transistor is M1, the nMOS transistor M2 acts as the active load and M3 and M2 form a current mirror to bias the gain transistor. Assume the following parameters: V_{DD} = 1.2 V, V_{Tn}=0.25 V, V_{TP} = -0.3 V (=-0.25V_{DD}) and the Early voltages $V_{An} = V_{Ap}$ = 15 V and finally K'_p = 160 µA/V^2, K'_n = 320 µA/V^2. Assume that the square-law model is valid. The transistor lengths and widths are the ones shown in the figure.

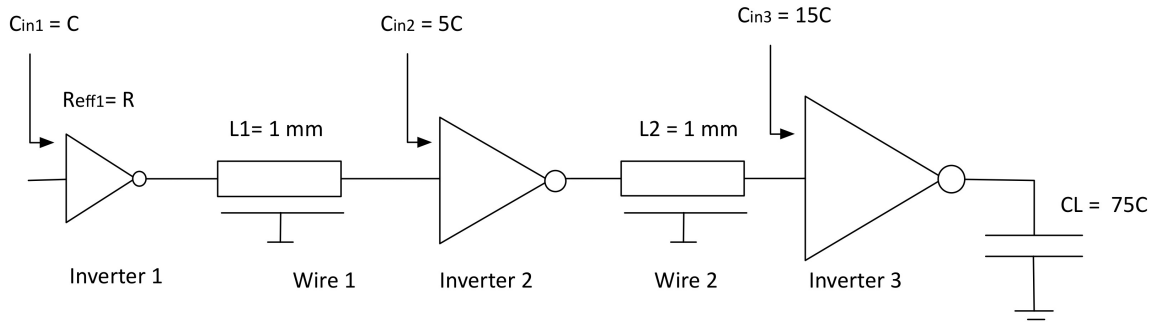


a) Determine what value of I_B would be required to set the operating point such that V_{OUT} = 0.6 V when V_{IN} = 0.75 V (=5/8 V_{DD}). (For simplicity neglect the Early effect in this calculation). Remember that the current mirror has its output current equal to its input current as long as its output transistor (M2 in this case) is in saturation. (1 p)
b) If the current I_B has the value you calculated in a) what is V_B? (1 p)
c) In this operating point, at what output voltage will M2 just enter its linear operating region? (2 p)
d) In this operating point, at what output voltage will M1 just enter its linear operating region? (2 p)
e) Draw the small-signal diagram for the amplifier. What is the expression for the voltage gain derived from the small-signal diagram? (2 p)
f) Calculate the magnitude of the small-signal voltage gain, $|A_V|$, for the amplifier. (2 p)

3) **Logic design, compound gates** As a designer of a datapath you are assigned the task to design a comparator for two positive unsigned numbers A and B. The instructions are that there should be two one-bit output signals for the result. One of these should have the two possible values A=B and A≠B. If the first signal has the value A≠B then the other one-bit signal should indicate whether A<B or A>B.

a) Perform the logical design of a one-bit cell that can be used in such a comparator. The cell should give a two-bit output that indicates if A=B, A>B or A<B. Clearly explain how you encode the two one-bit result signals. Include a truth table for the two one-bit output signals of your cell. (3 p)
b) Implement you one-bit cell as in static CMOS. There should be one compound gate for each of the two one-bit output signals. In addition you may have to use inverters at the outputs and/or inputs. Assume that the two one-bit input data signals, A and B, but not the inverses, are available as inputs to the cell. (5 p)
c) Show how to connect eight instances of you cells to form an 8-bit comparator. Clearly show how the inputs of the first cell should be connected. (The "first" cell is either the least or the most significant bit, depending on your design.) (2 p)

4) Wire delay & tapering The chip output pads where the internal signals get connected to the outside world, are large capacitive loads for the internal circuitry. In this problem such a large capacitive load is driven across a 2-mm chip over a long metal line. In the middle of the line a tapered inverter has been inserted and close to the capacitive load there is an even larger inverter. The metal-2 line is 0.2 µm wide and in total it is 2 mm long, but it has been divided up in two 1-mm wire segments. The first inverter has an input capacitance C and an effective resistance R. The sheet resistance for the metal-2 layer is RS = 0.0001R/□ and the wire capacitance is 0.05C/µm. Note that this capacitance value includes also all edge effects for the wire and is therefore given by length rather than by area. The whole circuit is shown here:

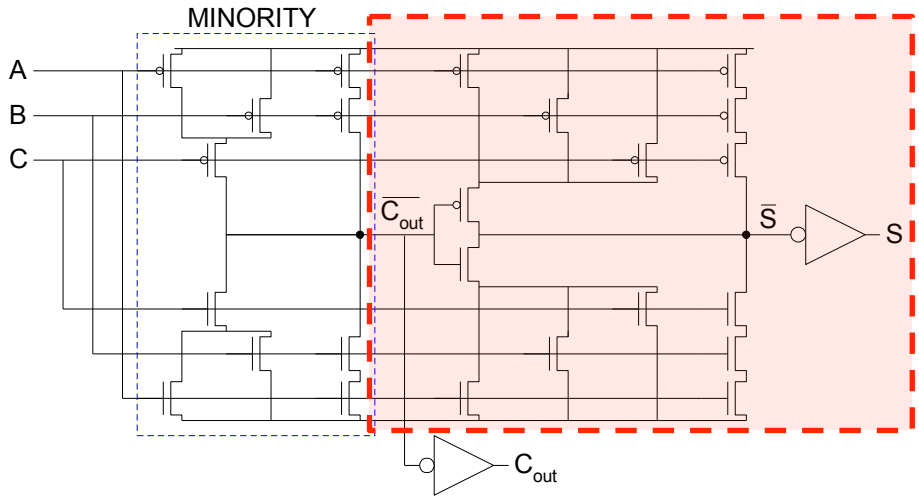


a) Calculate the resistance and capacitance of the wire segments expressed in R and C. (1 p)
b) Draw an equivalent circuit model for the entire circuit that can be used to calculate the total delay. For simplicity assume that the output capacitance of an inverter is the same as its input capacitance. (2 p)
c) Calculate the total delay from the first inverter to the load. (3 p)
d) What if we could move the middle inverter while the total wire length is still 2 mm. That is, if the two wire segments were to have different lengths, what percentage of the 2 mm wire should be driven by the leftmost inverter for minimum delay? (4 p)

5) Layout, parasitic capacitances In labs 2 and 3 you created a standard cell for the carry part of the full-adder cell. Below you see the schematics from the Weste & Harris book of the entire full adder.

a) Your task here is to create also the layout of a standard cell for the sum part (highlighted part in schematics). You are to use the template that can be found at the end of the exam (there are two in case you make a mistake). Use a single-line-of-diffusion approach and make sure that each input signal has to connect to the cell only once. You can assume that also C_{out} is routed in in metal2. Do not use metal 2 inside the cell except to connect to the incoming inputs. (7 p)

b) In our relative delay model we express the parasitic delay of any logic gate as p^*p_{inv} where p_{inv} is the parasitic delay of a standard inverter. The parasitic delay is due to the drain areas connected to the output of the logical gate. What is p for your sum cell as determined from your layout from a) ? Assume that shared drain areas contribute the same parasitic capacitance as do non-shared drain areas. Are there any improvements you could make to your layout to decrease p? Motivate your answer!(3 p)



6) Prefix adders During the course, you have designed a Sklansky prefix tree adder, and carefully analyzed the worst-case propagation delay. During lecture time, we have even made attempts to size the dot-operator cells for minimum delay. In this last task of the written exam, you will be asked to design a Brent Kung adder, and to calculate its worst-case delay.

a) The first task is to use the prefix tree template shown below to complete the design of a Brent Kung adder. Just as in the Sklansky adder a binary tree structure is used to create the block "Generate" and "Propagate" signals, $G_{16:0}$, $P_{16:0}$, respectively. However, the adders differ in the way they create the carries needed for the SUM calculation. In the Brent Kung adder these are obtained from the leaf cells of two smaller inverse types of trees, the roots of which are CIN and C7:0. These leaf cells are shown in the template. Compared to a Sklansky adder, the Brent Kung adder reduces the branching of the C7:0 node from eight to four dot operator cells. The template is repeated at the end of the exam so that you can tear it of and hand it in with your exam. (4 p)

b) The number of dot operator cells needed for creating a block G, P binary tree for an N-bit adder seems to be N-1. As an example, in the template below 15 cells are shown to be needed to create the block P and G of a 16-bit adder. Show that this is consistent with the formula for the sum of a geometric series, $2^0 + 2^1 + 2^2 + ... + 2^k = 2^{k+1} - 1$ (2 p)

c) According to this formula, the total number of dot operator cells needed in an N-bit Brent Kung adder should be N-1+2(N/2-1)=2N-3. Is this the number of cells in your Brent King adder from a)? (1 p)

d) In the diagram for the Brent Kung adder you have designed in task a) highlight the critical path for meeting the timing constraint. Then calculate the worst-case carry delay through its prefix tree. Assume that all gates are non-inverting, and have an X4 drive strength, and that they have an input capacitance corresponding to that of an X2 inverter, which makes the logical effort of any non-inverting gate equal to ½. Assume that this assumption holds also for the X4 XOR gates for the SUM calculation. For simplicity also assume a parasitic delay p=8 for the AO21 gate. (3 p)

PREFIX TREE TEMPLATE FOR BRENT KUNG ADDER

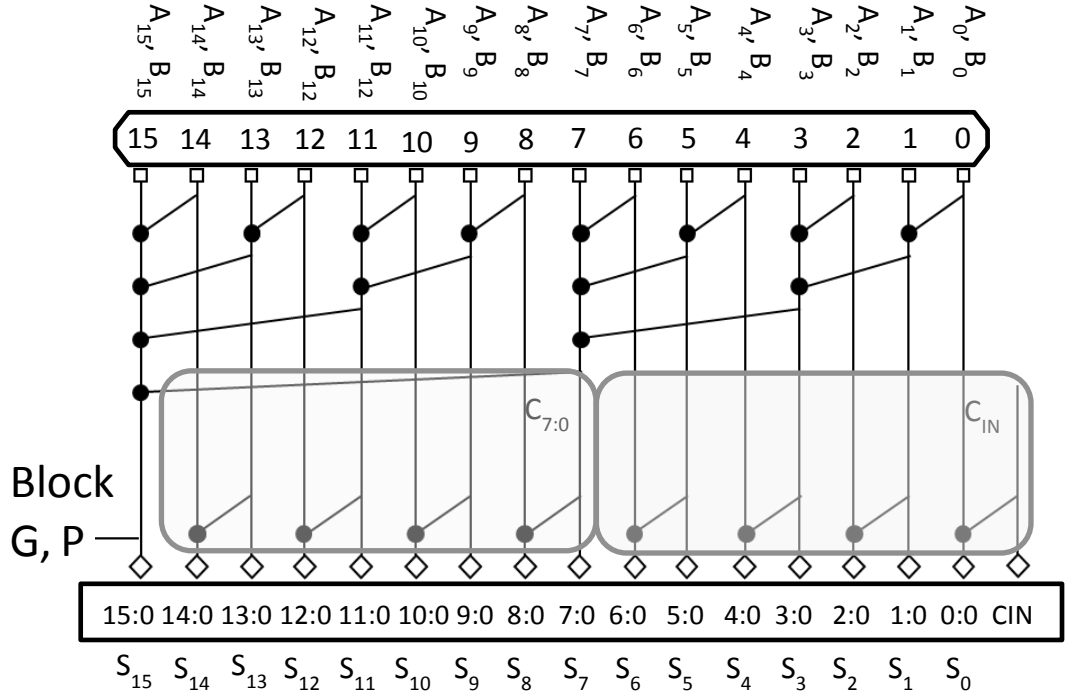


Table for problem 1 to hand in with solution

Exam number:_____

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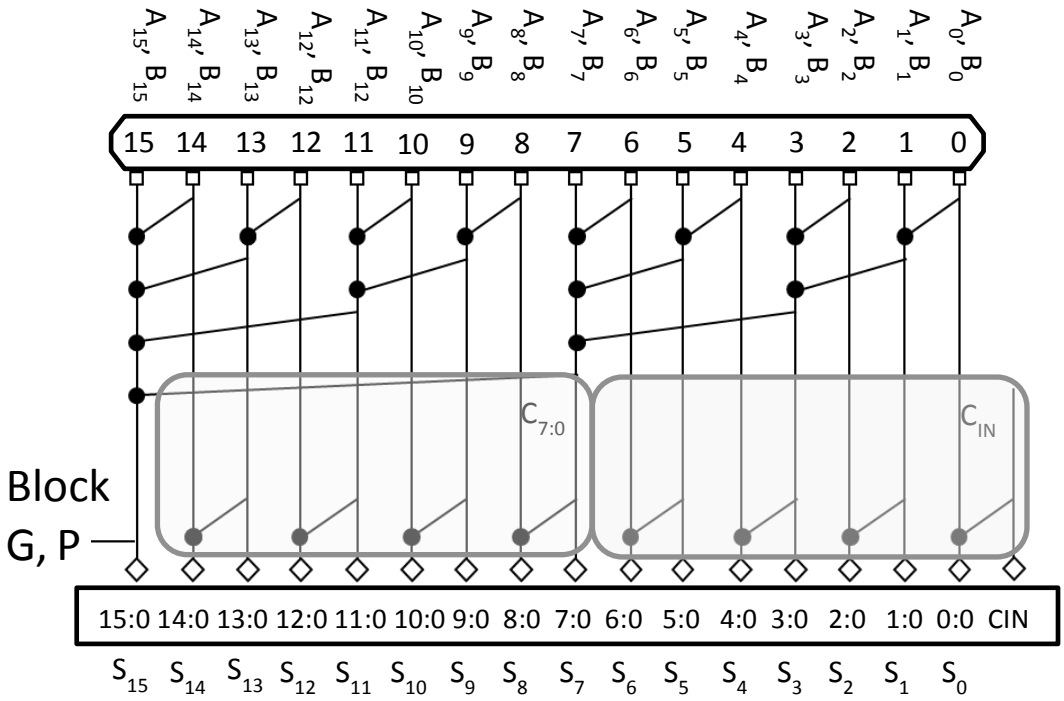
	Transistor widths	

Diagram for problem 6 to hand in with solution

Exam number:_____

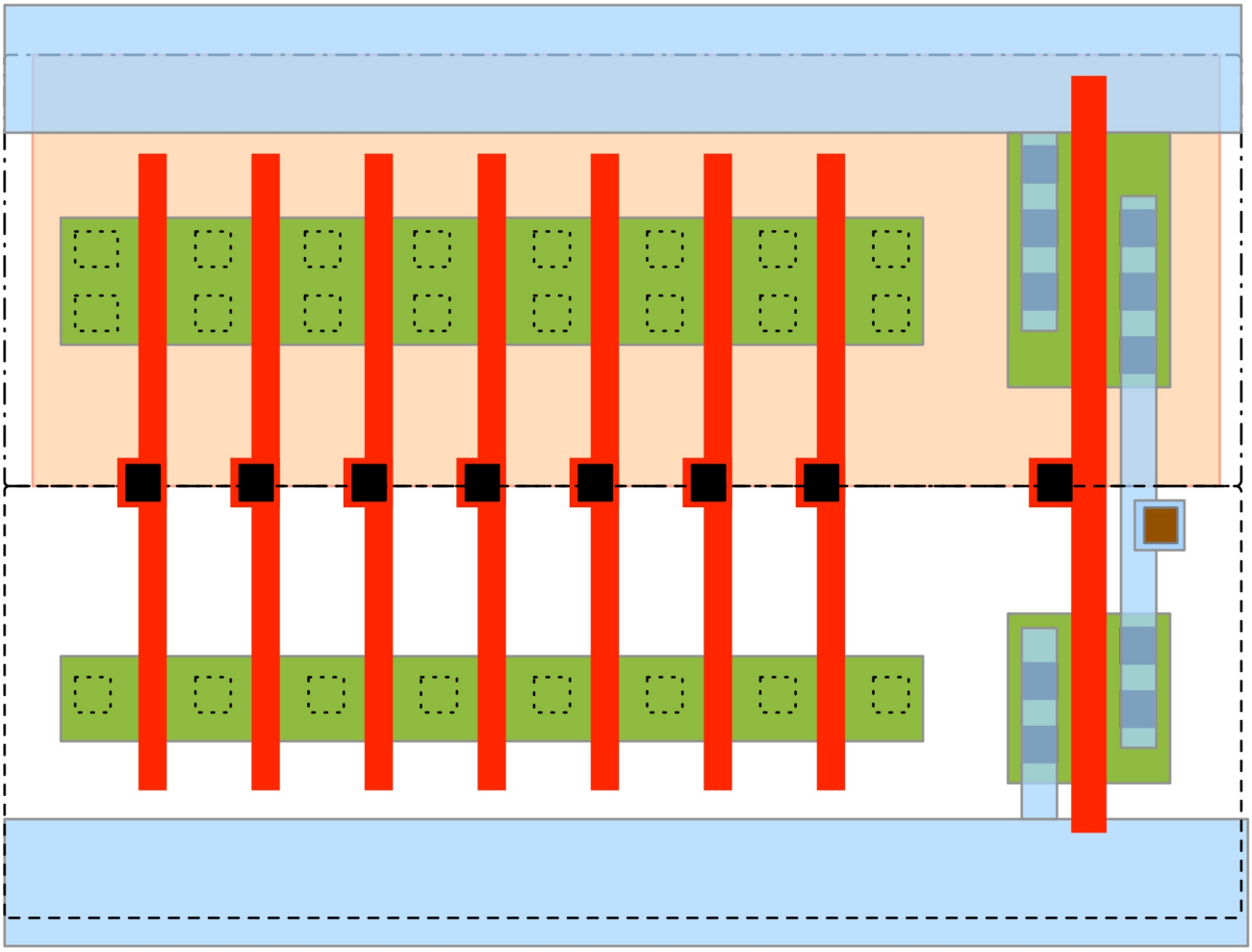
PREFIX TREE TEMPLATE FOR BRENT KUNG ADDER



Problem 5 STANDARD-CELL LAYOUT TEMPLATE FOR SUM CELL

Exam number:_____

Label all poly lines, except the inverter one. If you have changed the circuit diagram from the one shown in the problem redraw the circuit diagram below the layout.



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