Solution **Integrated Circuit Design MCC091 Fri**day October 31, 2014

1) Power

Note: No motivation was required but I include one here anyway for the benefit of future students.

For dynamic power the expression is:

$$P_{dyn} = fC_L V_{DD}^2$$

Thus, for dynamic power we have V_{DD}: **D**, V_T: **N,** C_L: **D** and Width: **N.**

For the short-circuit power we have $P_{SC}=V_{DD}*I_{SC}$ and it is the regular drain-current equation in the saturation region that gives the short-circuit current. This current flows when both transistors are on during the transition, so we can roughly assume that the input voltage is $V_{DD}/2$ if we want to have a detailed expression for it:

$$P_{SC} = V_{DD} I_{SC} \approx V_{DD} k' \frac{W}{L} (\frac{V_{DD}}{2} - V_T)^2$$

Thus, for short-circuit power we have V_{DD}: **D**, V_T: **I,** C_L: **N** and Width: **D.**

Similarly, for the static current the power is $P_{stat} = V_{DD}*I_{sub}$. The subthreshold (leakage) current depends exponentially on the gate-to-source voltage; the further below the threshold voltage, V_T, V_{GS} is when the transistor is fully off the lower the subthreshold current; so a higher threshold voltage gives a lower subtreshold current when V_{GS} = 0 V. Also again, the current is proportional to the transistor width.

Thus, for static power we also have V_{DD}: **D**, V_T: **I,** C_L: **N** and Width: **D.**

2) Amplifier large- and small-signal analysis

a) The required saturation current through the pMOS transistor is:

$$I_{D_p} = \frac{k'}{2}\frac{W}{L}(V_{GS} - V_{TP})^2 = 160V_{DD}^2(\frac{5}{8} - 1 + \frac{1}{4})^2 = \frac{160 * 1.44}{64} = 3.6\ \mu A$$

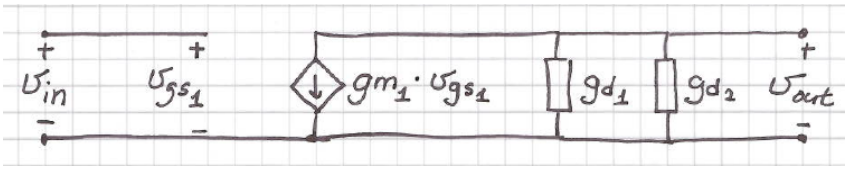
Thus, I_B has to have this value for the pMOS transistor to be biased in saturation.

b) Since $K_P = K_N$ (2/1*160 = 1/1*320) the active load transistor (M2) and the gain transistor (M1) must have the same effective gate voltage, $V_{GT}=|V_{GS}-V_T|$, for their saturation currents to be the same. The V_{GT} of the pMOS transistor is $V_{DD}/8$ = 0.15 V so we have $V_B = V_{TN}$+ 0.15 V = 0.4 V.

c) $|V_{DS}| >= V_{DSAT} = |V_{GT}|$ is the requirement for the transistor to be in the saturated region. For M2 this means V_{OUT} = 0.15 V.

d) For M1 the saturation requirement means $V_{OUT} = V_{DD} - |V_{GT}|$ = 1.05 V.

e) See below:



f) We can use the approximate current-related expressions for g_m and gd:

$$g_m = \frac{2I_D}{V_{GT}} \quad g_d = \frac{I_D}{V_A}$$

Then we get

$$|A_V| = \frac{g_{m_1}}{g_{d_1} + g_{d_2}} \approx \frac{\frac{2}{|V_{GT}|}}{\frac{1}{V_{Ap}} + \frac{1}{V_{An}}} = \frac{V_A}{|V_{GT}|} = \frac{15}{0.15} = 100$$

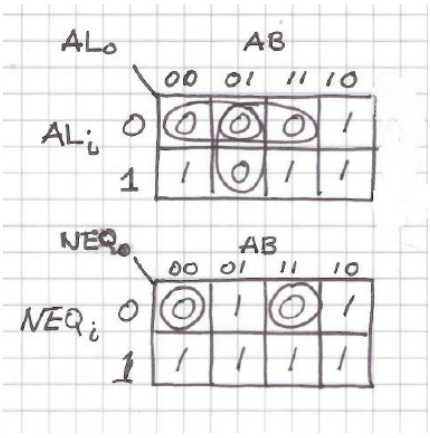
3) There are several possible solutions here depending if you let the signals pass from MSB to LSB or from LSB to MSB and how you code the signals. In the solution given here the signals pass from LSB to MSB and they are quite similar to adders you have already designed.

a) We use two signals called NEQ and AL. If in the cell A and B are not equal NEQ is set to 1. Furthermore, when A is not the same as B, AL is set to 1 if A is 1 and to 0 if B is 1. This corresponds the generate situation in the adder. If A=B then we should just pass the incoming values of NEQ and AL to the corresponding outputs of the cell; this situation corresponds to the propagate situation in the adder.

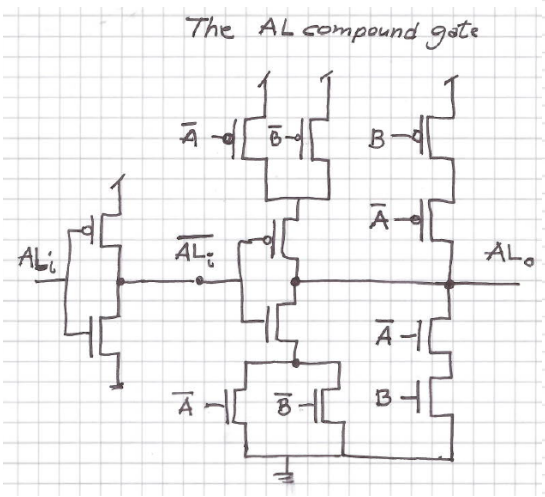
$$NEQ_o = A\bar{B} + \bar{A}B + NEQ_i$$

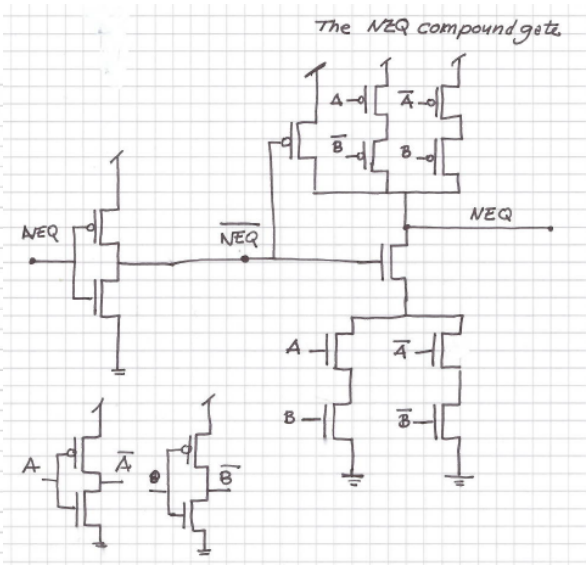
$$AL_o = A\bar{B} + (AB + \bar{A}\bar{B})AL_i$$

b) To arrive at the compound gates it is good to use the Karnaugh diagrams and circle the zeros to find the pull-down network (these are shown below). To find the pull-up network one does the same with the ones while remembering that the inputs have an additional inverse due to the pMOS bubble.

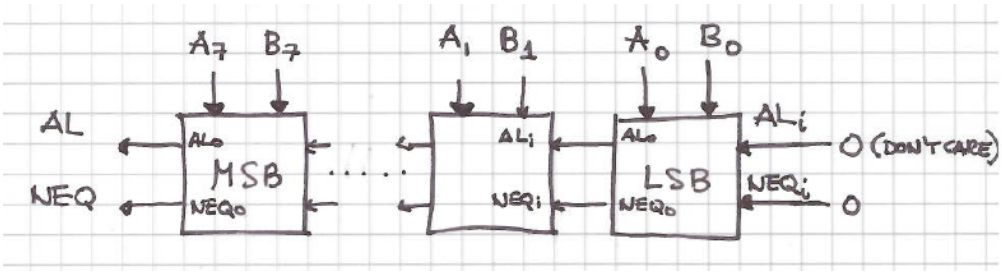


The resulting gates from these Karnaugh diagrams are shown below. Four inverters are also needed as shown.

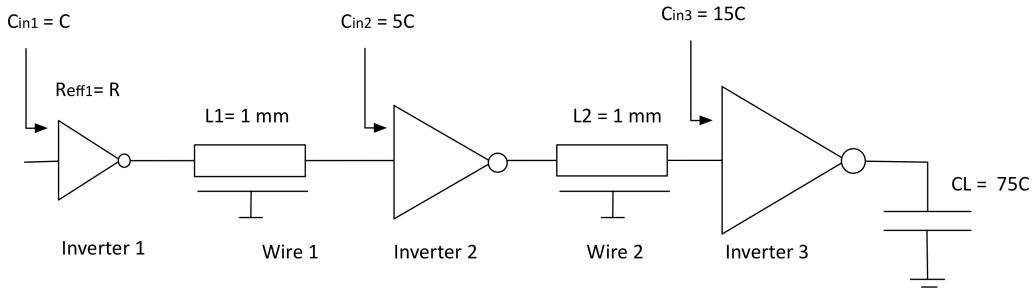




c) The setup can be seen below. The input value for the first ALi signal does not matter but the NEQi signal of the LSB cell must be set to 0. Only if all cells fulfill the propgate condition does the 0 appear at the NEQ output of the last cell.

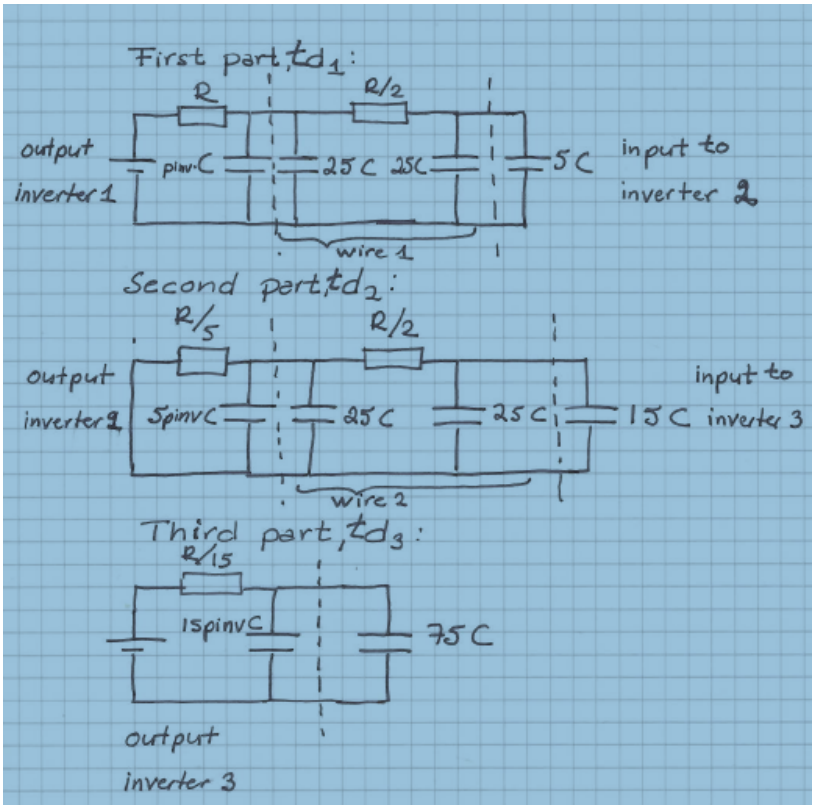


4) The setup is repeated below:



a) The capacitance of the entire wire is 2000*0.05C = 100C. That is each 1-mm wire has a capacitance that is 50C. The resistance of the entire wire is 2000/0.2 (number of squares) *0.0001 R = R; that is each 1-mm wire has a resistance that is R/2.

There are three parts to the delay: t_{d1}: the delay from inverter 1 to inverter 2, t_{d2}, the delay from inverter 2 to inverter 3 and td3, the delay from inverter 3 to the load. To show the diagram clearly we have split it up in these three parts below:



b) The corresponding delays, with $p_{\underline{inv}} = 1$, are:

$$t_{d1} = RC(1 + 50 + 5) + \frac{RC}{2}30 = RC(56 + 15) = 71RC$$

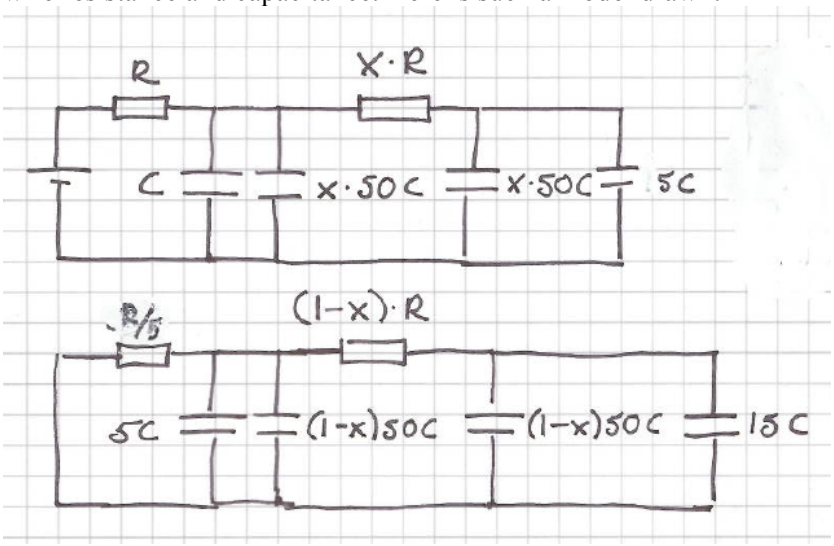
$$t_{d2} = \frac{RC}{5}(5 + 50 + 15) + \frac{RC}{2}40 = RC(14 + 20) = 34RC$$

$$t_{d3} = \frac{RC}{15}(15 + 75) = 6RC$$

In total we get:

$$t_d = t_{d1} + t_{d2} + t_{d3} = (71 + 34 + 6)RC = 111RC$$

c) Only delays t_{d1} and t_{d2} depend on the wire segments. To find the optimal split of the 2-mm wire we have to express the wire resistance and capacitance for the two segments as fractions of the entire wire resistance and capacitance. Here is such a model drawn:



The corresponding expressions for the two delays are:

$$t_{d1} = RC(1 + x100 + 5) + xRC(x50 + 5) = RC(6 + 105x + 50x^2)$$

$$d_2 = \frac{RC}{5}(5 + 100(1 - x) + 15) + (1 - x)RC((1 - x)50 + 15)$$

With further simplification we get:

$$t_{d2} = RC(4 - 20(1 - x) + 50(1 - x)^2 + 15(1 - x)) = RC(4 + 35(1 - x) + 50(1 - x)^2)$$

We need to take the derivate of the delay and set it equal to 0 to find the optimum value for x. We can do that either by summing the two delays first or by taking the derivative of each part and then set the sum of the derivatives equal to 0. Here we choose the second approach. Do not forget to take the derivative also of (1-x)!

$$\frac{dt_{d1}}{dx} = RC(105 + 100x)$$

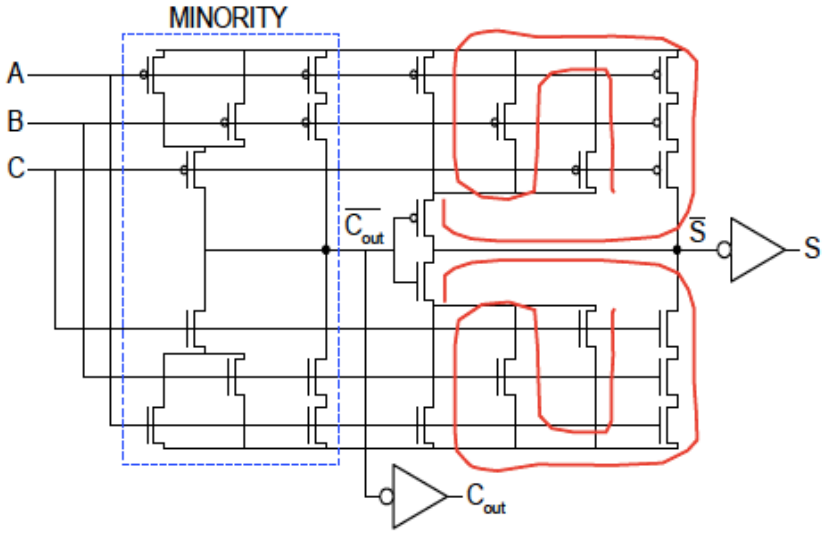
$$\frac{dt_{d2}}{dx} = RC(-135 + 100x)$$

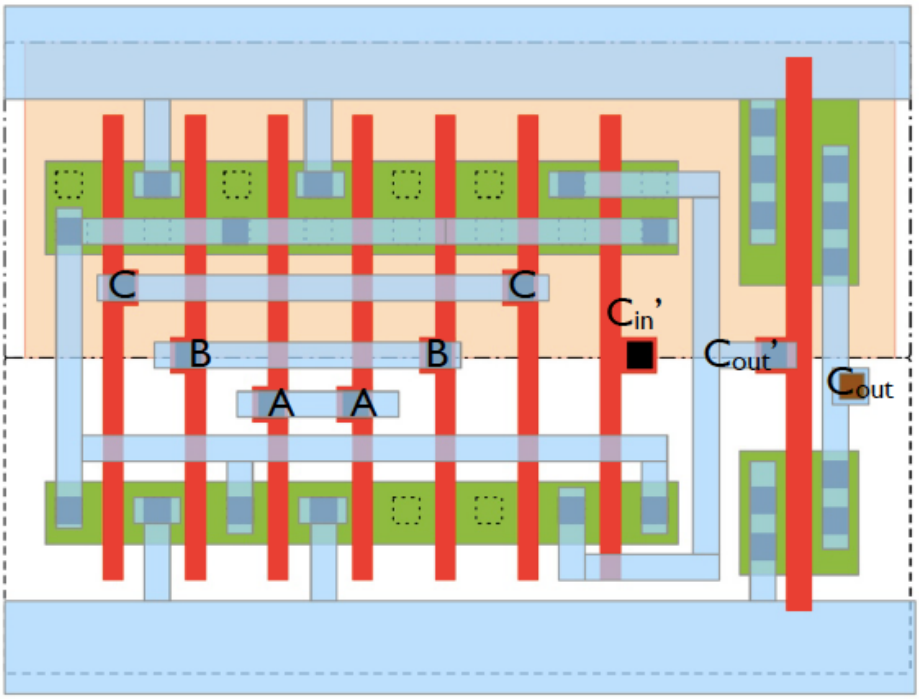
When we sum and set to 0 we get 200x = 30 and thus we arrive at x= 0.15. That is the length of the first wire should be 0.3 mm and the length of the second one1.7 mm.

The total delay is then $t_d = RC(21 + 53 + 6) = 60RC$. So we have reduced the delay by almost 50% by moving the middle inverter. (To calculate the resulting delay is not part of the problem but is it good to check that the delay really is reduced – if not there is probably a mistake somewhere).

5)

a) The p- and n-nets are symmetrical so we do not have to do Euler graphs. There are (at least) two straightforward solutions to finding the single-line-of-diffusion solution. We show one of them here.

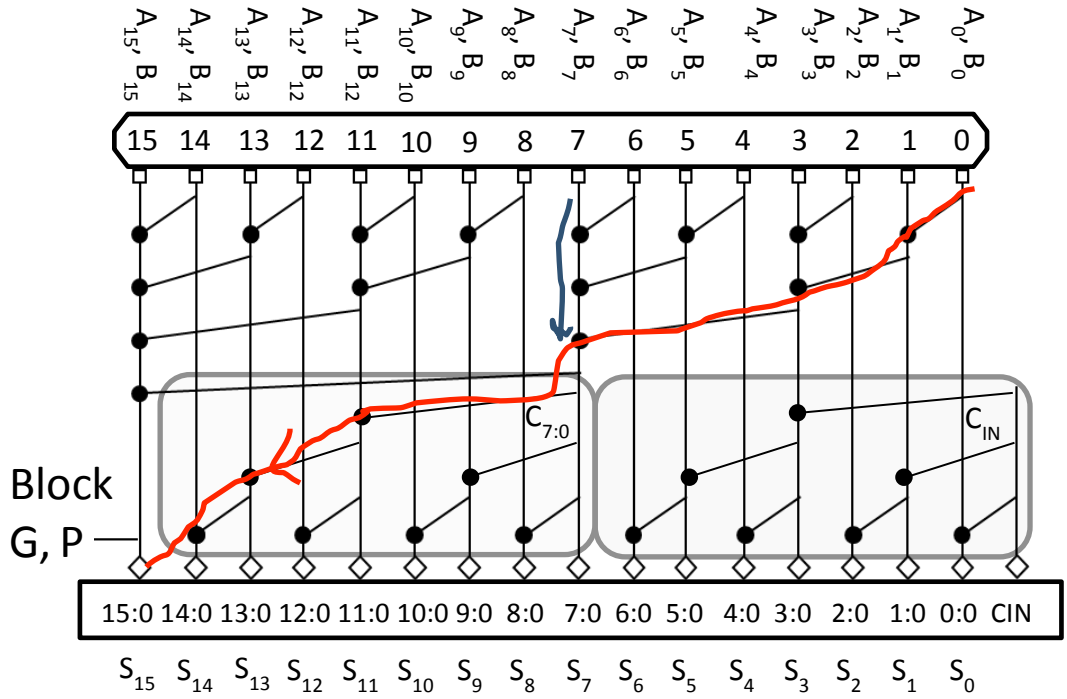




b) In the layout above there is only one p-diffusion drain area and one n-diffusion drain area connected to the output node so the parasitic delay for the circuit as it is laid out above is the same as that for an inverter.

6)

a) & d) The Brent Kung adder completed and marked in red its critical path.



a) See above.
b) $k=\log_2(N/2)$, that is $k+1= \log_2 N$, and $2^{\log_2 N}=N$
c) It holds here, of course.

d) The critical path can be seen above. A sketch of the circuit for calculating the worst-case delay can be seen below:

Bit 0: AND gate drives 2 AOI gates
Bit 1: AOI gated drives 2 AOI gates
Bit 3: AOI gate drives 2 AOI gates
Bit 7: AOI gate drives 4 AOI gates + 1 EXOR gate
Bit 11: AOI drives 2 AOI gates + 1 EXOR gate
Bit 13 AOI drives 1 AOI gates + 1 EXOR gate
Bit 14: AOI drives 1 EXOR gate

Total fanout for alla the tagates is: 2+2+2+5+3+2+1 = 17
The interal delay for the AOI gates is 8 and for the and gate 7 and the logical effort of all gate is g = ½:
Thus, we have a total delay d = 17*1/2+ 6*8+7 =7.5+55= 63.5

Note that if the summation tree is drawn incorrectly in a) the fanout will be different. The most common mistake is that one or more of the carry-in connections are missing which changes the fanout for bits 0,1 or 3.

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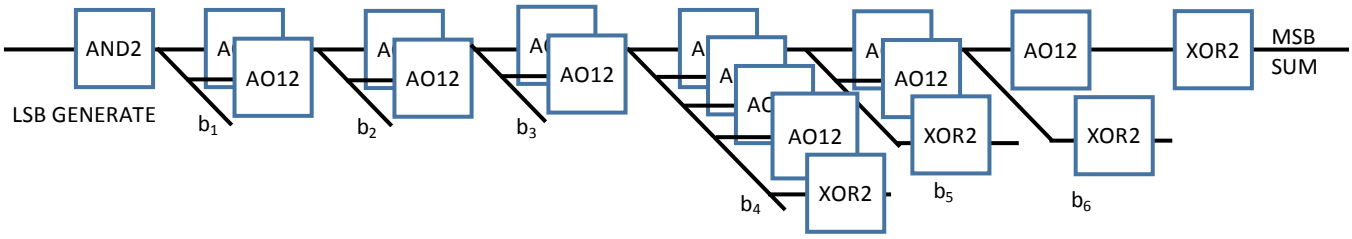

The total relative delay for this critical path is (neglecting the XOR gates for the sum calculations):

d = (7+0.5*2)+2(8+0.5*2)+(8+0.5*5)+(8+0.5*3)+(8+0.5*2)+(8+0.5*1)= 55+0.5*17=63.5

Note that the logical effort, g, is 0.5 for all gates rather than 1, which we have for the output inverters themselves, because at the output of the AO and AND gates there is an X4 inverter, whereas the input transistors have X2 sizes. The parasitic delays of the AO and AND gates comprise also the delay of the AOI or NAND gates (because these delays are not changed by the capacitive load at the output of these gates), and therefore the parasitic delays are quite high.

To get the delay in seconds one has to multiply the relative delay with τ. With τ = 5 ps we arrive at a critical-path delay of 317.5 ps.