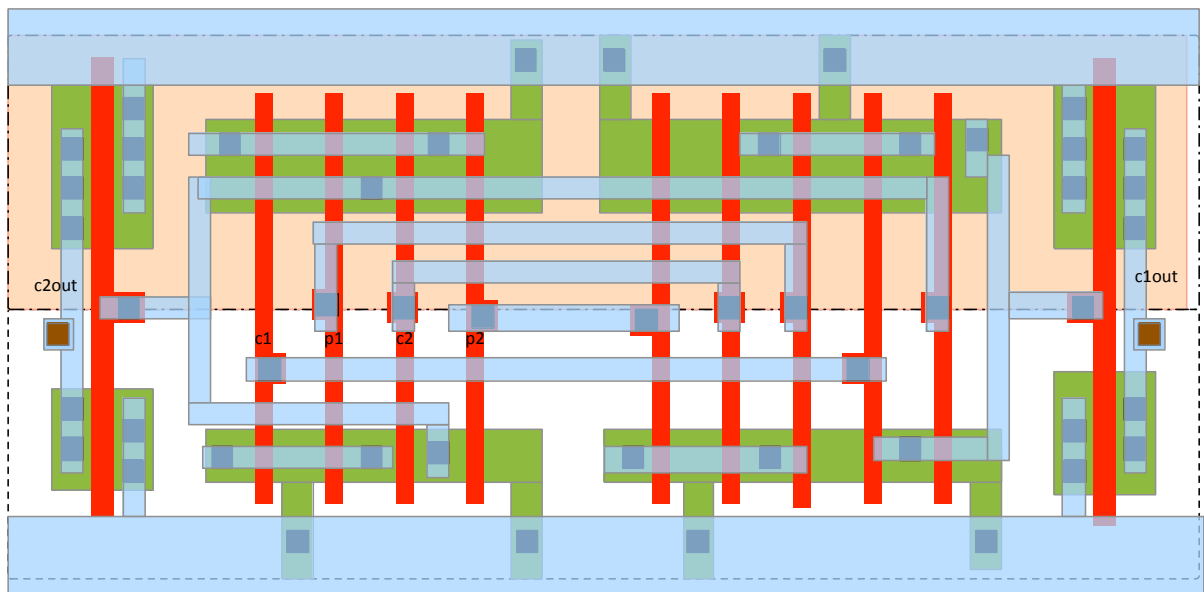# Solution to examination in **Integrated Circuit Design MCC091**
Thursday October 29, 2015 Version 1.0

Changes since version 0.91. Solution to problem 1.b was added. Solution to task 3 was updated to use V_{DD} = 1.2 V rather than 1.0 V. Also a calculation mistake in the solution to task 4a has been corrected.

1) **Layout and logic functions**

   a) c2out = p2+c2(c1+p1)

   b) Layout is shown below. Other solutions are also possible.
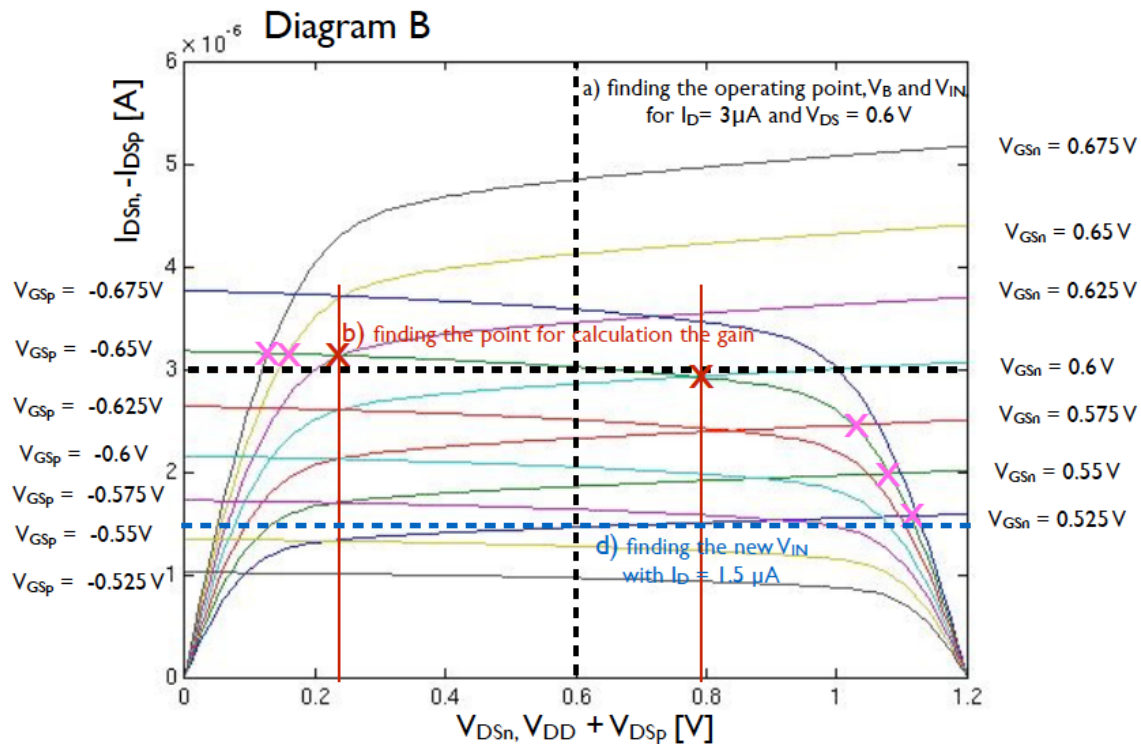

2) **Amplifiers and transistor characteristics**

   a) V_B is forced by I_B from the current source, to the voltage V_{DD}-V_{GS3} ,where V_{GS3} is the voltage that gives the current 3µA (while also V_{DS3} for M3 is the same as V_{GS3}). From the black lines added to diagram B, this gives us V_{GS3} = -0.65 V and thus **V_B = 0.55 V**. V_{IN} has to be set to the voltage that gives also M1 the current 3 µA. From diagram B we find that it is a V_{GS1} slightly higher than 0.6 V, approximately **V_{IN} = 0.605 V**.

   b) Transistor M_2 (the active load) is biased on the "load line" V_{GS2} = -0.65 V. The points where this line intersects the nMOS curves are marked by crosses in diagram B . The two red crosses show the steep part where both transistors are in saturation. From these two points we find that the gain is $|A_V|$ is approximately (0.79-0.24)/(0.625-0.6) = **22**.

   c) The small-signal diagram is:

   The expression for the gain is **$|Av| = g_{m1} / (g_{d1} + g_{d2})$.**

   d) The expression for the gain derived in task c) is independent of the bias current. We have gm ≈ $2I_D/V_G T$, where V_{GT} is short for V_{GS}-V_T, and $g_d = I_D/V_A$ where V_A is the Early voltage. The gain is then $|A_v| = V_A/V_{GT}$. So under the assumption that V_A remains the same only V_{GT} will change when the

current is decreased. Lower current implies lower V_{GS1} and thus an **increased** gain. From diagram B we find (blue line) that for the drain current 1.5 µA V_{GS1} has to be 0.525 V. The decrease in V_{GT} is then from 0.305 to 0.252. The increase in gain in percent gain is $100 * (1/0.225 – 1/0.305)/1/0.305 = 100*(0.305/0.252-1) = 21$ %. So we get an **increase of around 20%.**

Diagram B

3) **Dynamic and static power** Note! This solution has been updated. The problem states V_{DD}=1.2 V, but the previous solution used V_{DD}=1.0 V which was the intended V_{DD}.

a) (This problem is also an example in Weste & Harris) The capacitance for the logic part is 50 million transistors * 0.3 um * 1.8 fF/um = 27 nF and for the memories 950 million * 0.1 um * 1.8 fF/um =171 nF. The power consumption for the logic part is then 0.1 * 1 [GHz]*1.2^2 [V^2]*27[nF] = 3.88 W. The dynamic power for the memories is : 0.02 * 1 [GHz]*1.2^2 [V^2]*171 [nF] = 4.92 W. All in all the dynamic power for the chip is **8.8 W.**

b) (0.9*25*10+0.1*25*100+25*5)*0.3= **200 mA**. (This problem is also an example in Weste & Harris) The static power is due to the subthreshold leakage and gate leakage. We assume that half of all transistors as on and half are off. Only off transistors contribute subthreshold leakage and only on transistors contribute gate leakage current. For the memory part we have the total leakage current: 425 million transistors * 0.1 um * 10 nA/um + 425 million transistors 0.1 um*5nA, that is 425 million* 0.1 um*15 nA/um = **637.5 mA** of leakage current. For the logic part we have 25 million transistors that are on, and 25 that are off. Of the off ones 5% have the high VT. So the leakage current is (0.95*25*10+0.05*25*100+25*5)*0.3= **146.25 mA**. All in all the leakage current is 783.75 mA and the power (since P=U*I) is **940 mW**. (Note that this result is not the same as in the book because there is a calculation error in book solution).

c) The dynamic power for the logic part would increase by 20 % since the capacitance increase by 20% and all the other factors stay the same. The leakage current would be ((0.99*25+5)*10+0.01*25*100+30*5)*0.3= **270 mA**. So it would not save any dynamic power because the added 5 million transistors have more leakage than what we save by having fewer low VT transistors.

d) The dynamic power of 3.88 W from a) corresponds to 3.23 A of current. When this current is drawn through the power-gate switch there should be no more than 50 mV of voltage drop across it. Using Ohm's law, we find the maximum resistance of R= 0.06 [V]/3.23 [A] = 0.0186 Ω. So the transistor has to be very wide! W = 2000 [Ω.µm]/0.0186[Ω] = 107526 µm = 108 mm. So the transistor is around 11
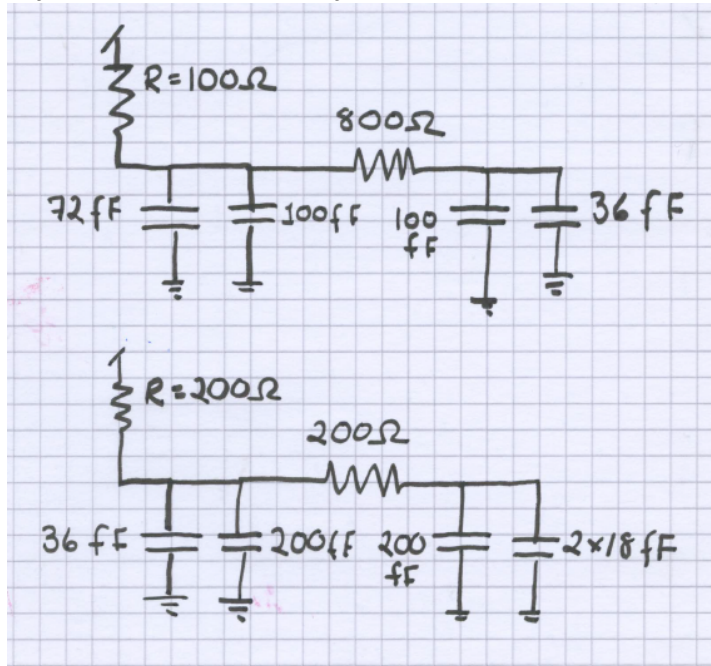
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cm wide! (In practice it can be a bit less wide since the transistor resistance at low V_{DS} is smaller than R).

e) The capacitance of the switch is W * 1 fF/um; that results in 107526 fF or 107.5 nF. The energy is then 155 nJ (since $E = CV_{DD}^2$ and V_{DD} is 1.2 V). The static power for the logic part from b) is 146 mA * 1.44 V^2 = 210 mW. Power is energy per time. So how long time for the total energy due to leakage to be equal to E_{sw}? We get $E_{sw} = E_{leak} = P_{leak}*t$ so $t = E_{sw}/P_{leak}$ = 186 [nJ]/210 [mJ/s] (since Watts are Joules/second). We get **t = 0.89 μs**.

BONUS QUESTION

f) Obviously the case in c) is not good since both the dynamic power and the leakage is higher than in b), but in the general case it is a question about determining when to spend all the energy to turn the power off. One has to be rather good at predicting the down-time to spend the energy required. So it may be better to spend more on the dynamic power if the static power can be reduced without having to turn the power off, since it is very costly to do so.

4) **Wire delay, wire and inverter delay**

a) There are two parts in this circuit as is shown in the figure above. For the second part we use a collapsed tree in this solution, but one can also use Elmore branches. Elmore for first part: 100 Ω* (72 + 100 + 100 + 36)fF + 800 Ω* (100 + 36)fF = 139.6 ps. Elmore for the second part: 200 Ω*(36+100+100+36)fF +200Ω* (100 + 36) fF=3*200*136 fF = 81.6 ps. All in all the delay becomes td = 0.7*(139.6 + 81.6) = **155 ps.**

b) We know that for the 2-input NAND gate we have g_{NAND} is 4/3 and p_{NAND} is 2 (otherwise we could derive theses numbers). The path effort from A to B is then F= G*H= (4/3)*72/*1.5 = 64. For minimum delay all stage efforts should be the same. In this case all stage efforts, f, should be 4 since 4*4*4=64. To find the inverter sizes we can start from the output or the input of the path. From the input we have 4/3*h_{NAND} = 4 => h_{NAND} = 3 so the input capacitance of the first inverter in the buffer should be **4.5 fF**. The input of the second inverter should 4 * 4.5 fF = **18 fF**. These capacitances correspond to drive strenghs 200 / 4 = **50X** for the second inverter and 50/4 = **12.5X** for the first inverter.

c) The resulting normalized delay d is (4+4+4+P)τ where P is the sum of the parasitic delays for the three gates . We have P = 2 + 1+ 1 = 4. Here we use our prior knowledge that the 2-input NAND gate has p= 2, but we could also derive it, if we did not remember. Thus, we have d = 16τ. But what is τ in this process? We had better check that too. It is 0.7*R*C = 0.7*72fF*0.1 kΩ = 5 ps. So, the delay from A to B is 16*5 ps = **80 ps.**

COMMENT: Is the total delay from A to C now 80 ps + 200 ps = 280 ps or is there some delay we have not accounted for, since we assumed infinite drive strength at point B in task a)? In our path delay calculation in b) we accounted for the electrical effort of the second buffer so we have accounted for that delay and therefore it is correct to assume that the total delay is the sum of the two delays.

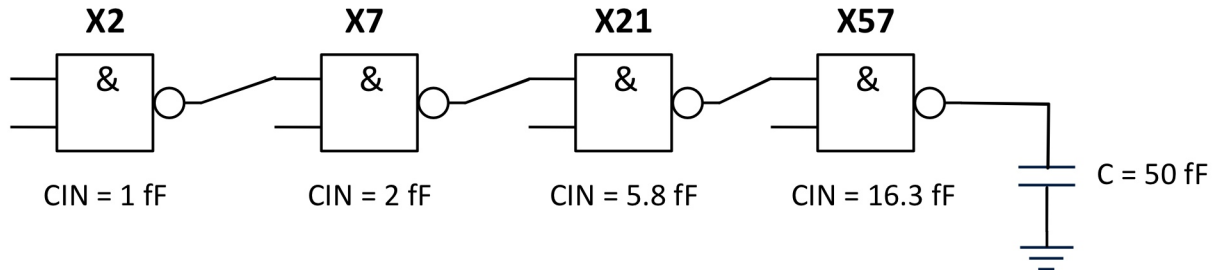## 5) Critical timing paths, logical effort

Table 1

INVERTER DATA	X2	X4	X7	X13	X27	X53	X106
Input capacitance [fF]	1	1.3	1.6	3.3	5.8	12	25.1
KLOAD = 0.7Reff [kΩ]	4.1251	2.3529	1.6004	0.7612	0.4298	0.2101	0.1021
Intrinsic delay	13.2	11.9	10.5	10	9.9	10.1	10.6

Note: Unit for intrinsic delay is ps.

Table 2

2-input NAND data	X2	X7	X21	X57
Input capacitance [fF]	1	2	5.8	16.3
KLOAD = 0.7Reff [kΩ]	6.9746	2.2207	0.6572	0.2312
Intrinsic delay	17.6	15.9	14.9	14.6

Note: Unit for intrinsic delay is ps.

a) **The FO4 delay is 20 ps**. We use the data from Table 1 inverters of size X13-X106 since for these the parasitics is almost constant. FO4 is: intrinsic delay + $4*C_{INPUT}*K_{LOAD}$. To be clear I make a table here (which is not required in the student solutions):

Size	Input cap * KLOAD [ps]	Parasitic delay [ps]	FO4 delay [ps]	Pinv (intrinsic delay/tau)
X13	2.511	10	20.04	3.98
X27	2.493	9.9	19.87	3.97
X53	2.521	10.1	20.18	4,01
X106	2.560	10.6	20,84	4,14

We see that the FO4 delay is 20 ps with tau = 2.5 ps and pinv = 4 (which is very high!).

b) **The logical effort, gNAND, is 1.5**: We use data from Table 2, sizes X7 – X57. The logical effort, gNAND, is CINNAND*KLOADNAND/ tau. To be clear, I again make a table here (which is not required in the student solutions):

Size	LOAD-dependent delay= Input cap * KLOAD [ps]	Parasitic delay [ps]	gNAND = load-dependent delay/tau	pNAND = (intrinsic delay/tau)
X7	4.441	15.9	1.77	6.36
X21	3.812	14.9	1.52	5.96
X57	3.768	14.6	1.51	5.84

It looks like we should also discount the data from the X7 NAND. If we only use the data from X13 and X57 we get: gNAND=1.5.

c) **The parasitic delay, pNAND, is 6.** The parasitic delay is defined as the intrinsic delay/tau. pNAND is also listed in the table above. Again we discard the X7 data. The intrinsic delay is around 15 ps and tau is 2.5 ps so we get pNAND = 6 (also see table above). This value for p is very high, since what we have used theoretically is p = 2.

COMMENT: We can note, however, that the inverter also has a very high p. If we express pNAND as p*pinv we get 1.5* pinv which is reasonable for a good layout, where there are two pMOS transistors sharing one diffusion area.

d) We first determine the electrical efforts: We have h1=2/1 = 2, h2 = 5.8/2 = 2.9, h3 = 16.3/5.8 = 2.8 and h4 = 50/16.3= 3.1. Thus, we have htot = h1 + h2 + h3 + h4 = 10.8

All in all we have: d = gNAND* htot+ 4*pNAND.

With our extracted model, gNAND = 1.5 and pNAND = 6, we get: **d = 40.2.**

With our theoretical numbers, gNAND = 4/3, pNAND = 2 * pinv and pinv = 1, we get **d = 22.4**

COMMENT: With our theoretical numbers, gNAND = 4/3, pNAND = 2 * pinv, but with pinv = 4, we get d = 48.4 which is much closer.

6) Adders

PART A

a) If the group propagate signal for the carry-skip block (P7:0, cell D13) is 1 the multiplexer should select the carry-in to the block (CIN, cell S13), if it is 0 is should select the carry out generated from the block (G7:0, cell C13). The function is then:

$$C_{OUT} = P_{7:0} \cdot C_{IN} + \overline{P_{7:0}} \cdot G_{7:0}$$

It is also OK to give the excel expression.

b) The logic cells are one AO gate for the group generate and one AND gate for group propagate. Here is a figure from Weste and Harris:

PART B

c) Ladner-Fischer diagram from Weste & Harris book.