Written examination in **Integrated Circuit Design MCC091**

Tuesday January 5, 2016, at 8.30-13.30 at Lecture halls, Hörsalsvägen

Staff on duty: Lena Peterson, D&IT, phone ext: 1822, or mobile 0706-268907. Will visit around 9.30 and 11.45.
Administration: Send exams to Lena Peterson D&IT, and send lists to CSE student administration office.

Technical aids for students: This is a closed-book exam. Allowed aids: A Chalmers-allowed calculator (non graph-drawing) plus pencil, eraser, ruler, and dictionary (these are always allowed). **The results** from the examination will be sent to you via the Ladok system within three weeks. The grading reviews will take place Friday January 22 2015, 12.15-13.15 in room 4128 and Tuesday January 26, same time and room. Solutions will be posted on the course web site in PingPong on January 7. Any student who does not have access to the 2015 PingPong page can contact Lena Peterson (via e-mail to lenap@chalmers.se) to obtain the solution.

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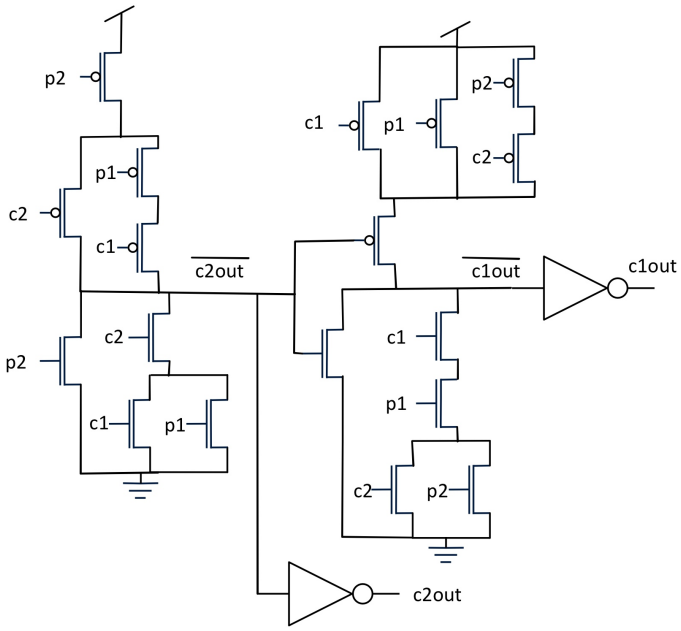
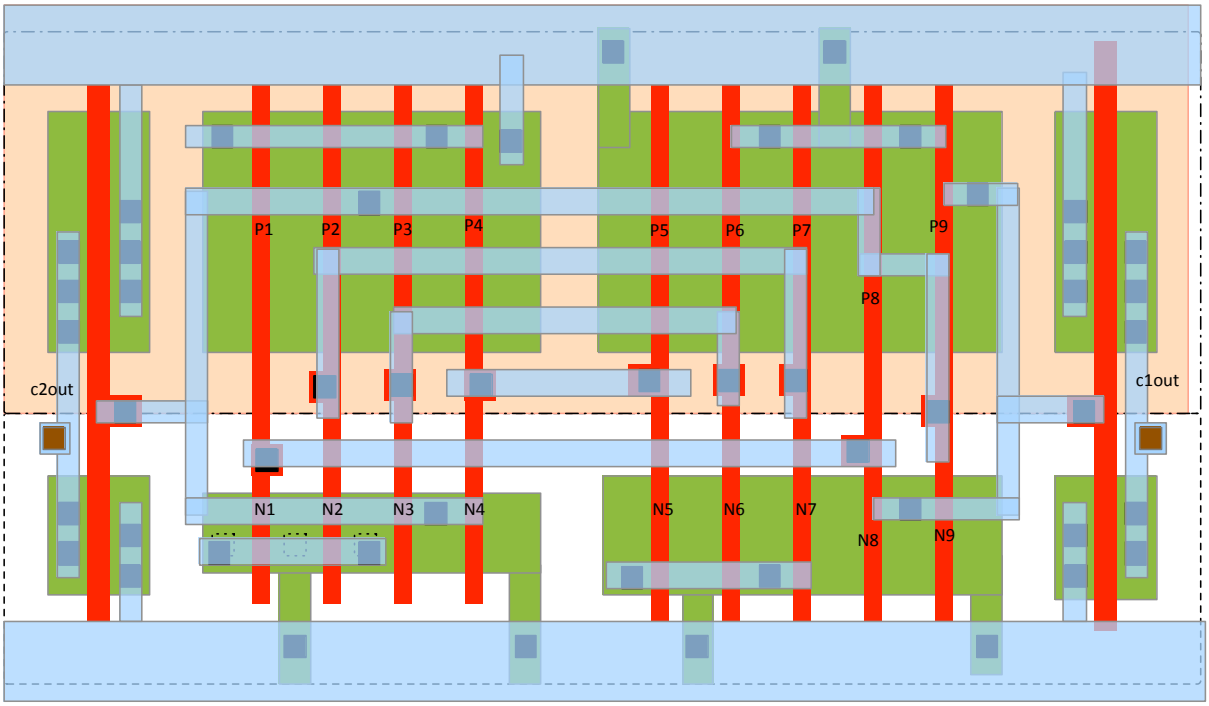
The written examination contains six problems, each worth 10 points. You need 30 points to pass, 40 points for grade "4" and 50 points for grade "5". Bonus points from the fall 2015 course instance will be added for the higher grades.

1) Logical effort, parasitic delay, layout

In the figure below is the schematic for a proposed carry chain in an unusual adder that can add three numbers. The signals p1 and p2 are partial sums of the three input bits and c1 and c2 are the two carry bits.



In the figure below (on the next page) is a layout for the carry-chain cell.



a) In the layout above the transistors in the compound gates have been scaled to make the worst-case delays equal to, or less than, that of the reference inverter where the pMOS transistor is twice as wide as the nMOS transistor. To facilitate the use of the single-line-of-diffusion layout style all pMOS and nMOS transistors in each gate have been scaled the same, which makes some worst-case delays **shorter** than the delay of the reference inverter. Which transistors could be made narrower than they are in the in the layout above, and what widths should they have to make all worst-case delays the same? Refer to the transistors by their labels in the layout. Hint: There is at least one transistor in each pull-up and pull-down network, so at least 4 transistors could be made narrower. (4 p)

b) From the **schematic** on the previous page, derive the logical effort, g, for the $c1$ input of the first gate and the $\overline{c2out}$ input of the second gate and the parasitic delay, p, for each of the gates. Use the transistor sizes from your solution to task a). (4 p)

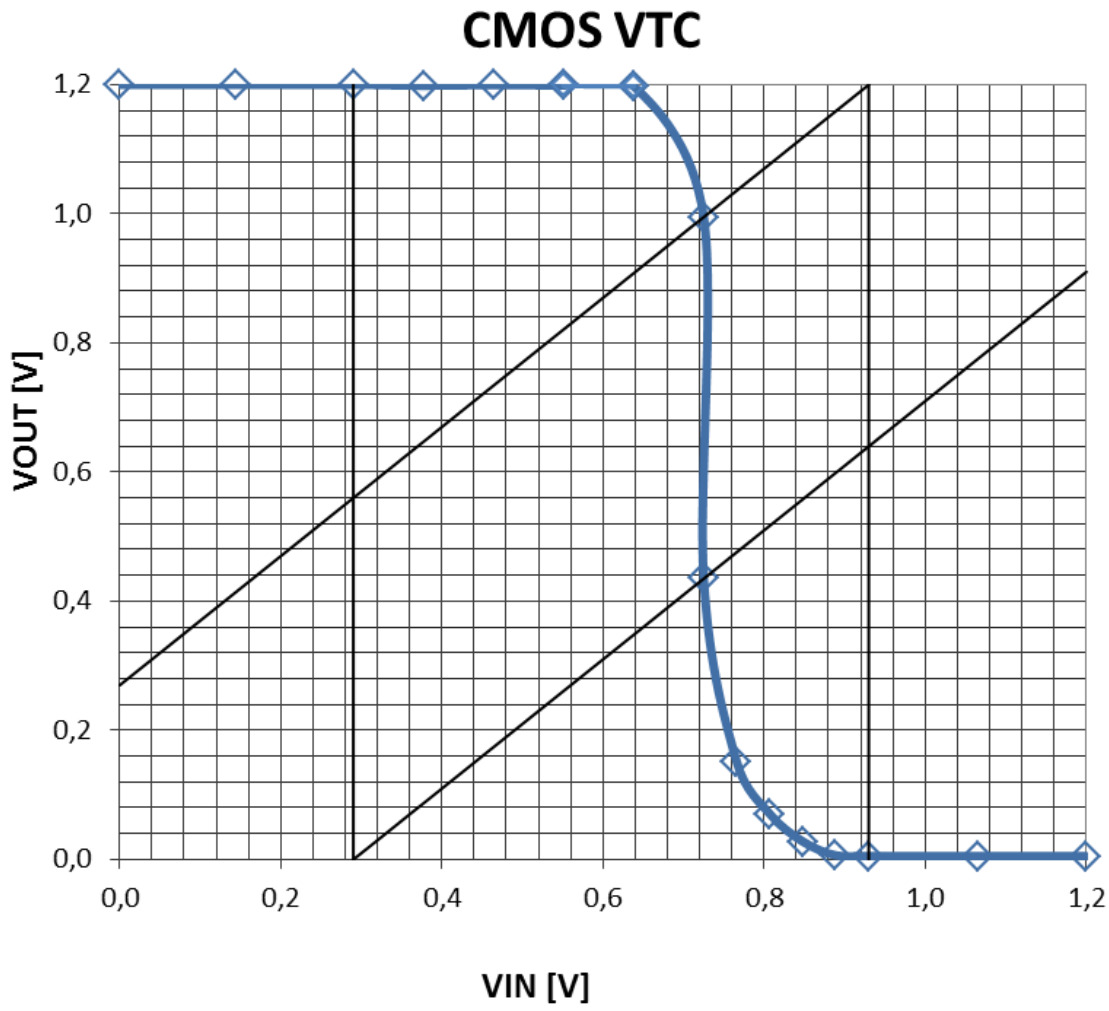
c) From the **layout** in the figure above, what are the worst-case p values for the two compound gates? That is, the p values when the resistance of the conducting transistors is equal that of the reference inverter. Assume the transistor sizes shown in the layout above. Also assume that each diffusion area has the same capacitance as the gate capacitance of a transistor of the same width. (2 p)

2) **Noise margins**

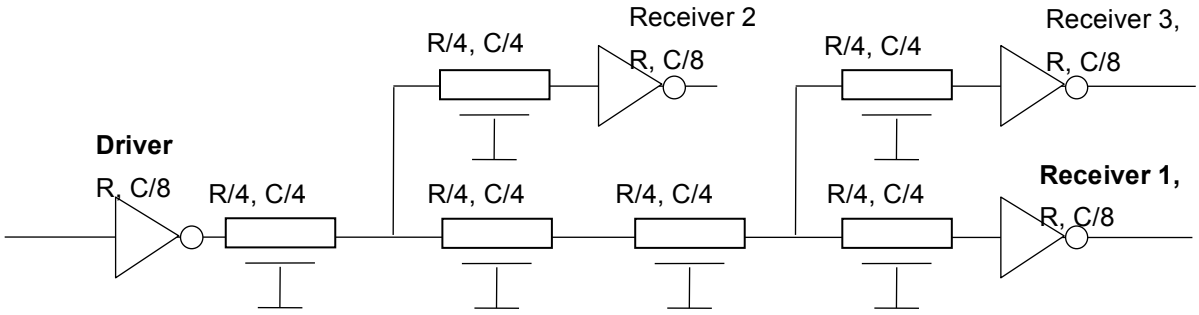
a) Explain what noise margins are. (2 p)

b) Why is it important to have high noise margins? And why does it get increasingly important in modern CMOS processes? (2 p)

c) Determine both noise margins, that is NML and NMH, from the voltage-transfer curve for a 3-input NOR gate shown in the figure below. (VTC is repeated at the end of exam so you can turn in with exam.) (6 p)



3) **Wire and inverter delay** The figure below shows part of a clock-distribution network where the driver inverter drives a network of wires and three receiver inverters. Assume that all inverters have an output capacitance equal to its input capacitance.



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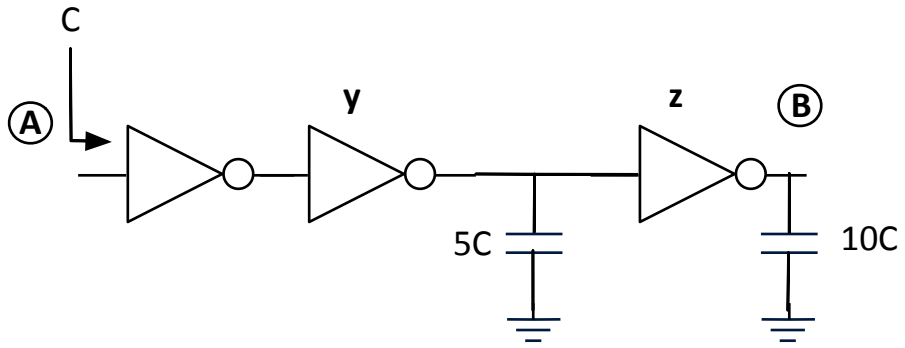
a) Draw an electrical model for the circuit in the figure above, which you can use to calculate the delay from input of the Driver to the input of the Receiver 1. (2 p)

b) Calculate the delay from the Driver input to the input of Receiver 1. (2 p)

c) Calculate the clock skews to the input of the receivers, between each pair of receivers, that is 1&2, 1&3 and 2&3. (4 p)

d) How will the clock skew between Receivers 1 and 3, calculated in task c), change if the output of Receiver 1 is connected to the input of an inverter identical to the ones in the figure above and Receiver 3 is connected to an inverter with transistors twice as wide? (2 p)

4) **Path delay with wires, inverter sizing** Below you see a schematic of three inverters driving two medium-length wire segments, which are modeled as lumped capacitances since their resistances are very small. The first inverter has an input capacitance C as is indicated in the figure.



a) Find an expression for the path delay from A to B in the figure. (3 p)

b) Using the expression you found in task a), size the two last inverters to minimize the delay, that is determine the input capacitances of the two later inverters, yC and zC, to minimize the delay. (5 p)

c) Calculate the resulting delay with the inverters sized as calculated in b), assuming that you use the 65-nm process where the FO4 delay is 25 ps and the inverter output capacitances are equal to their input capacitances (2 p)

5) **Scaling of delay and power** Emilia reads a highly interesting paper from 1992 about the Alpha processor[1]. This processor was fabricated in a 0.75 µm CMOS process with a supply voltage of 3.3 V. The processor operated at a whopping 200 MHz and dissipated 30 W. To assess how impressive a feat this design was, she would like to know what the FO4 delay was in that CMOS process. It is impossible to find any data for that process, but she has some data for a 0.35 um process, which also had a supply voltage of 3.3 V. In the 0.35 µm process she found out that that KP_n = 110 uA/V^2 for nMOS transistors and that they had a threshold voltage, V_{Tn}, of 0.5 V and that the gate capacitance, C_{ox} was 4.60 fF/um^2. She also has a (partial) table from the course textbook with some information about transistor scaling.

In this problem assume that the square-law current equation holds for the MOS transistors in both CMOS processes and that a pMOS transistors of the same width has half the current of an NMOS transistor and that all transistors have a parasitic capacitance equal to its input capacitances.

a) Estimate the FO4 delay in the 0.35-um process. (3 p)
b) From your result in a) estimate the FO4 delay in the 0.75 µm process. How many FO4 delays in the logic, does the clock frequency of 200 MHz correspond to? (3 p)
c) If we assume that all the power dissipation in the Alpha processor was due to dynamic power dissipation, what would its power dissipation have been in the 0.35 µm process? (2 p)
d) What if we had also scaled down V_{DD} from the 0.75 um process to the 0.35 µm process, with the same scale factor as other characteristics, what would the Alpha processor dynamic power be in the 0.35 um process then? (2 p)

TABLE 7.4 Influence of scaling on MOS device characteristics

Parameter	Sensitivity	Dennard Scaling	Constant Voltage	Lateral Scaling
Scaling Parameters				
Length: L		$1/S$	$1/S$	$1/S$
Width: W		$1/S$	$1/S$	1
Gate oxide thickness: t_{ox}		$1/S$	$1/S$	1
Supply voltage: V_{DD}		$1/S$	1	1
Threshold voltage: V_{tn}, V_{tp}		$1/S$	1	1
Substrate doping: N_A		S	S	1
Device Characteristics				
β	$\frac{W}{L}\frac{1}{t_{ox}}$	S	S	S
Current: I_{ds}	$\beta(V_{DD}-V_t)^2$	$1/S$	S	S
Resistance: R	$\frac{V_{DD}}{I_{ds}}$	1	$1/S$	$1/S$
Gate capacitance: C	$\frac{WL}{t_{ox}}$	$1/S$	$1/S$	$1/S$

[1] D.W. Dobberpuhl; et al. (November 1992). "A 200-MHz 64-b dual-issue CMOS microprocessor". *IEEE Journal of Solid-State Circuits* **27** (11): 1555–1567. doi:10.1109/4.165336

6) **Prefix adders** One of the authors of the course textbook, David MoneyHarris, has patented several new prefix adders. In his patent[2] are figures of the PG networks for three novel 32-bit prefix adders. The figures are numbered 5A, 5B and 5C and are shown on this page and the next one. The figures are also repeated at the end of the exam so that you can tear that page off and hand it in with your solutions.

a) Draw the critical paths for each of the three adders in the figures of the PG networks. For each of the adders, what is the number of PG (dot) cells in the critical path? (3 p)

b) Discuss the pros and cons of the three adders identifying at least one benefit and one drawback for each of them. (3 p)

c) Find an expression for the path delay for the critical path, that you identified in task a), of the PG network for adder 5B. Assume that we know that an the AO gates used have g=2 and assume that all AO gates are sized the same. For simplicity also assume that all the SUM cells are sized so that they have the same input capacitance as do the AO gates and ignore any buffers (that is assume they are not there). You do not have to include the delay of the setup cells or the SUM cells in the delay. (4 p)

d) BONUS QUESTION For adder 5A find **all** paths that have the **same number of dot operators** as does the critical path. How many such paths are there? Indicate them in the on the additional figure for adder 5A available on the tear-off sheet. (2 p)

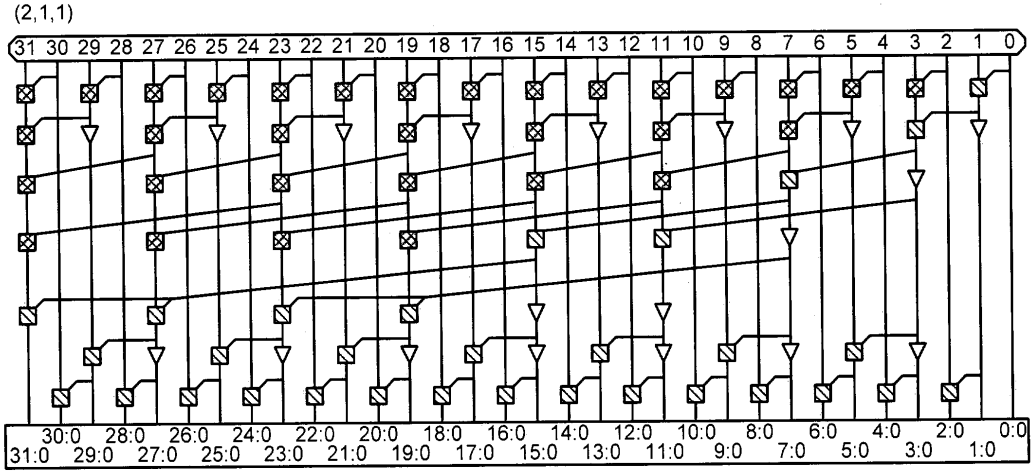


FIG. 5A

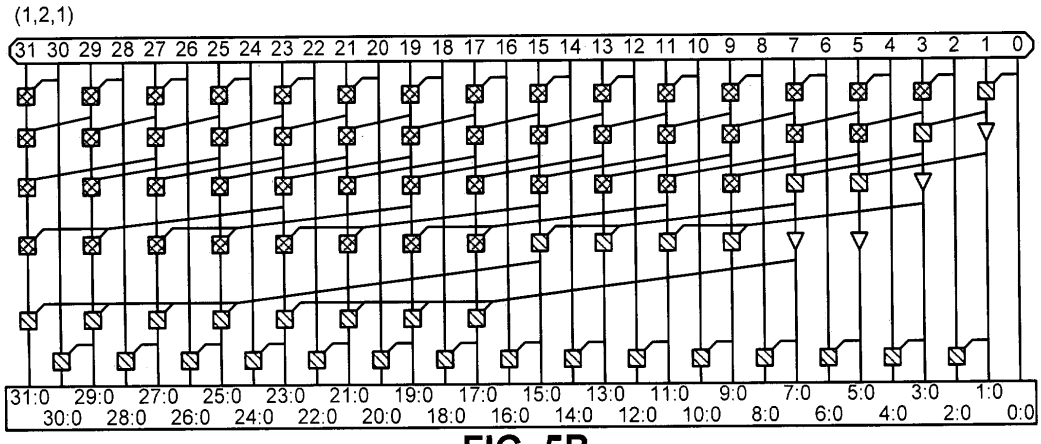


FIG. 5B

[2] Patent No US 7,152,089 B2 Parallel Prefix Networks That Make Tradeoffs Between Logic Levels, Fanout and Wiring Racks.

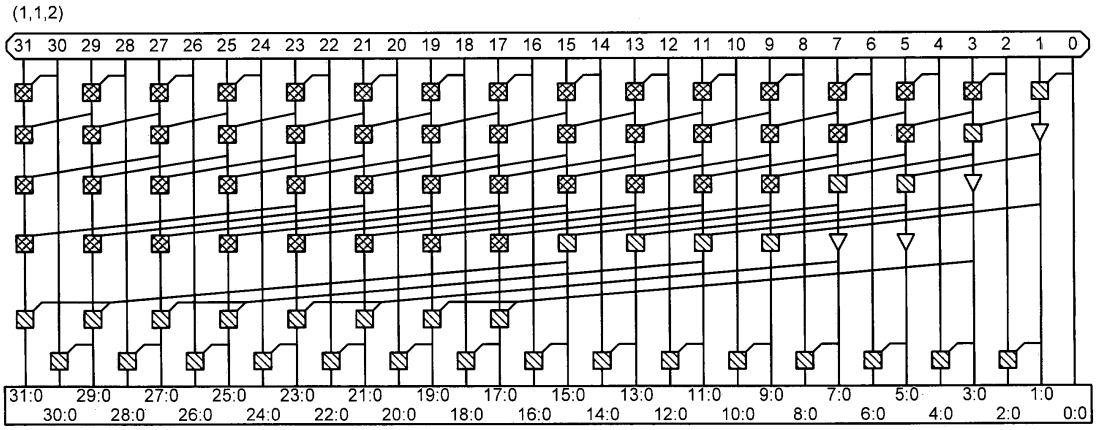


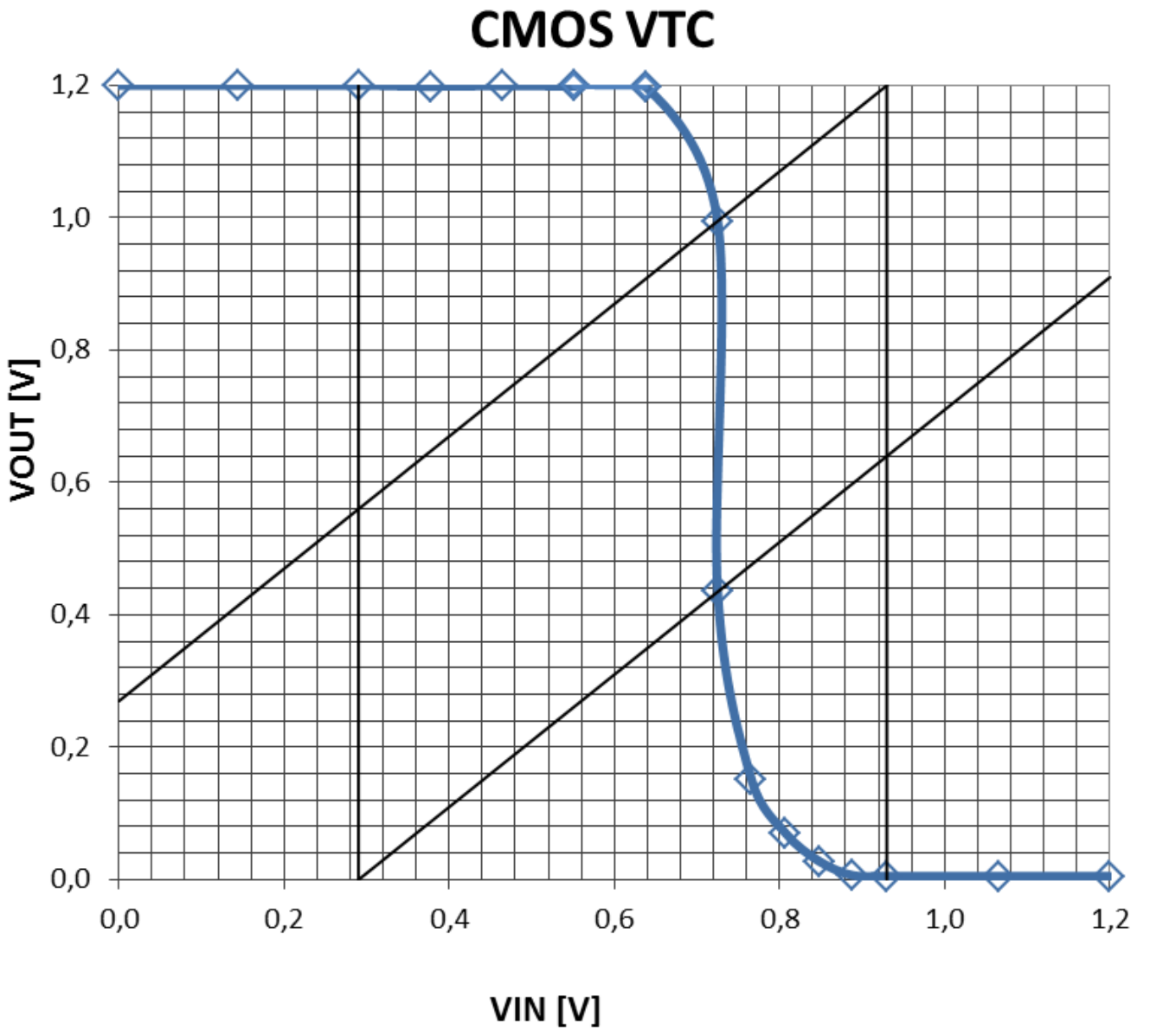
FIG. 5C

THE END!

Tear-off templates for tasks 2c and 6a & d are on the following pages

MCC091 2016-01-05 VTC for determining noise margins in task 2c

Anonymous code: _____



MCC091 2016-01-05 Harris' 3 PG networks for task 6b & d (next page)
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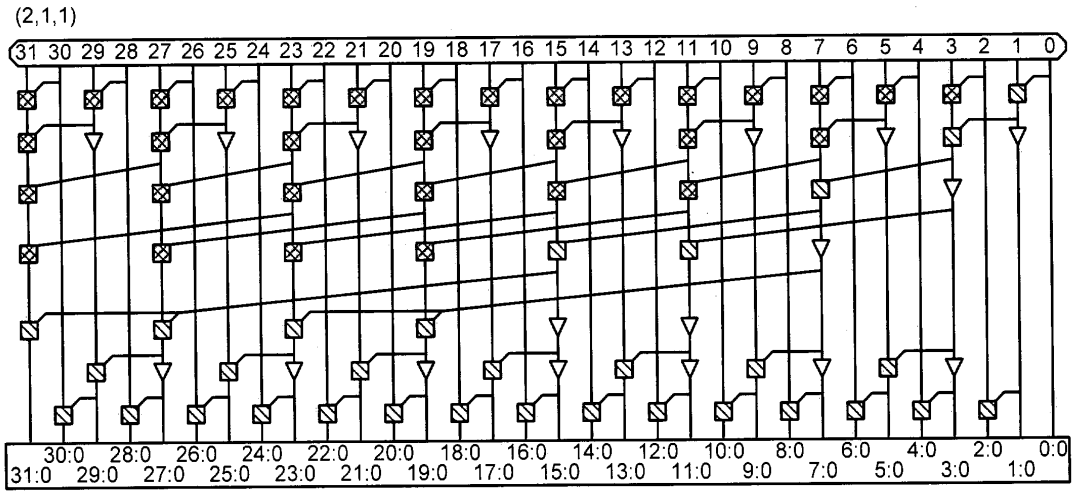

FIG. 5A

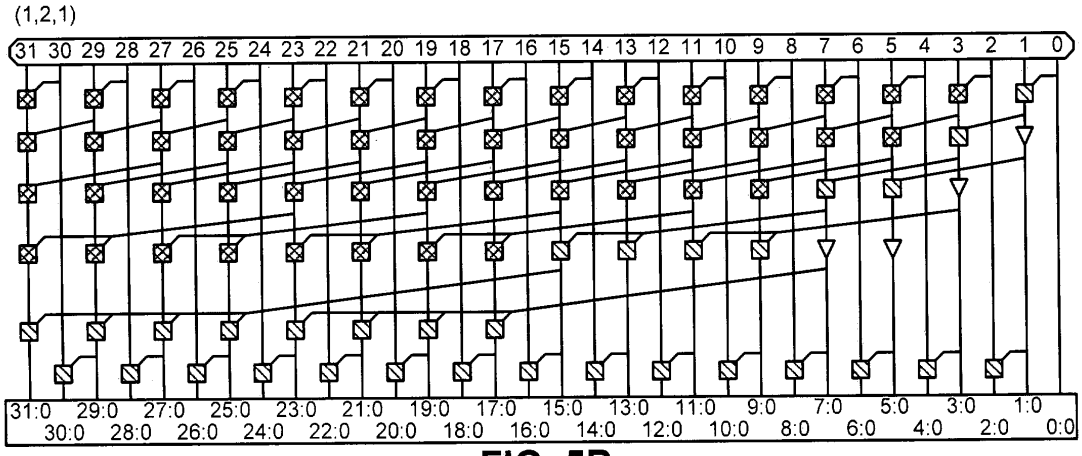

FIG. 5B

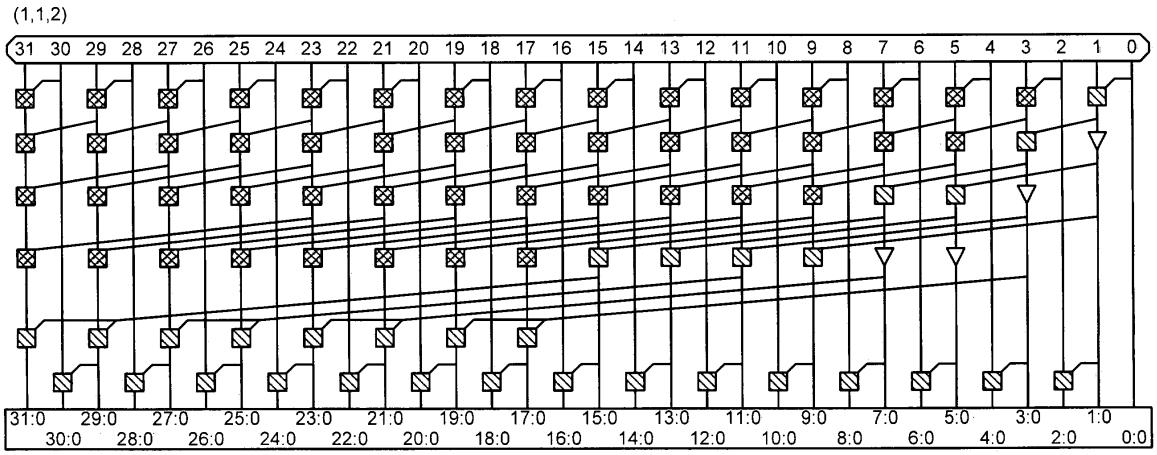

FIG. 5C

(2,1,1)

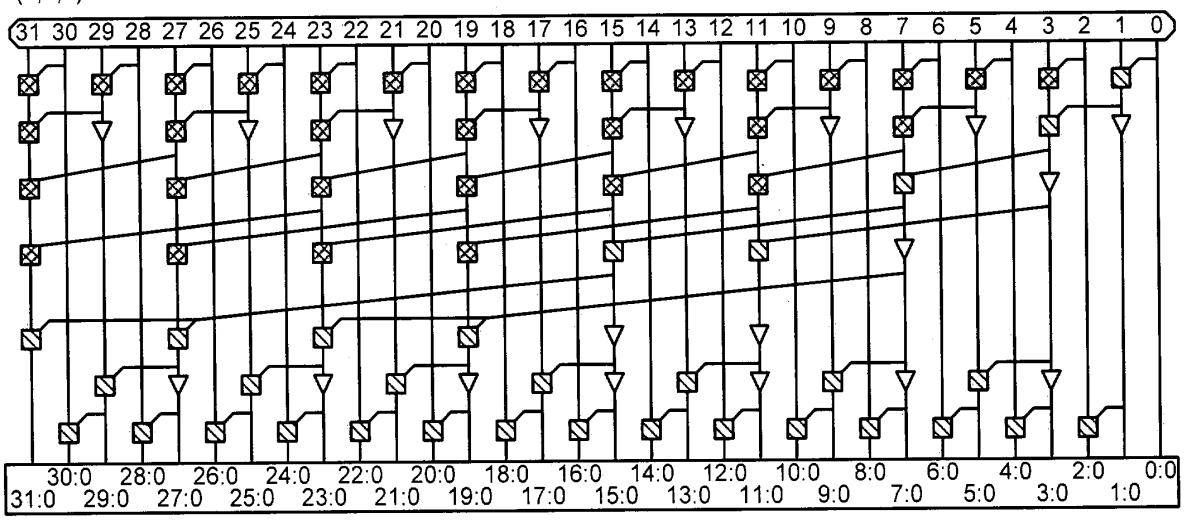

FIG. 5A

(1,2,1)

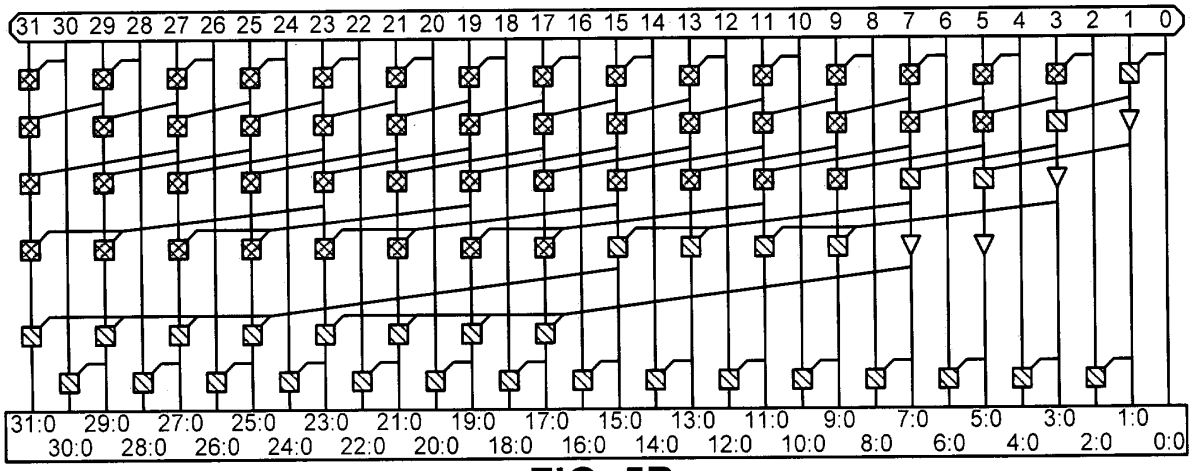

FIG. 5B