Written examination for

MCC092 Introduction to Integrated Circuit Design

Thursday December 22, 2016, at 8.30-13.30 at SB building

Staff on duty: Lena Peterson, D&IT, phone ext: 1822, or mobile 0706-268907.

Lena will visit around 9.30 and 12.00.

Administration: Lena Peterson will pick up exams; send lists to CSE student administration office.

Allowed technical aids for students: This is a closed-book exam. Allowed aids: A Chalmers-allowed calculator (non graph-drawing) plus pencil, eraser, ruler, and dictionary (these are always allowed).

The results from the examination will be sent to you via the Ladok system within three weeks. The grading review will take place Tuesday January 17 2017, 15:15-16:15 in room 4128.

Solutions: will be posted on the course web site in PingPong no later than Friday December 23. Any student who does not have access to the 2016 course web site can contact Lena Peterson (via e-mail to lenap@chalmers.se) to obtain the solution.

Instructions:

Write legibly.

State any assumptions you make.

Partial credits can be awarded but requires that you **explain** your reasoning and calculations.

Number all pages and write your code on each page.

Put only one problem per page.

Good luck!

Grades:

The written examination contains six problems, each worth 10 points. You need 30 points to pass (grade "3"), at least 40 points for grade "4" and at least 50 points for grade "5". Bonus points from the fall 2016 course instance will be added before the higher grades are assigned.

1. **Logical functions, layout, transistor sizing.** David Harris, the author of our textbook, holds quite a few patents. One of these[1] is for static CMOS gates that have multiple outputs. The schematic for one such gate is shown in Figure 1 a), taken from the patent (but the gate in the figure is not one of the patented gates).

   a) What are the four logical functions for the four outputs Y1 through Y4 indicated in the schematic in Figure 1 a)? (2 p)

   b) Draw the layout for the gate in Figure 1 a) in the template provided in Fig. 1 b). For simplicity we have assumed that all transistors have the same width although that may not be a good sizing. The template is repeated twice at the end of the exam. Hint: Remember that diffusion can be used to route V_{DD} or ground short distances. (5 p)

   c) What if your task was to ensure that the worst-case resistance is the same for the p-net and the n-net for all four logic functions, Y1 – Y4. How would you size the transistors then? Assume that the drive strength of an nMOS transistor is twice that of a pMOS transistor with the same width. There are multiple solutions – you only have to give one. (3 p)

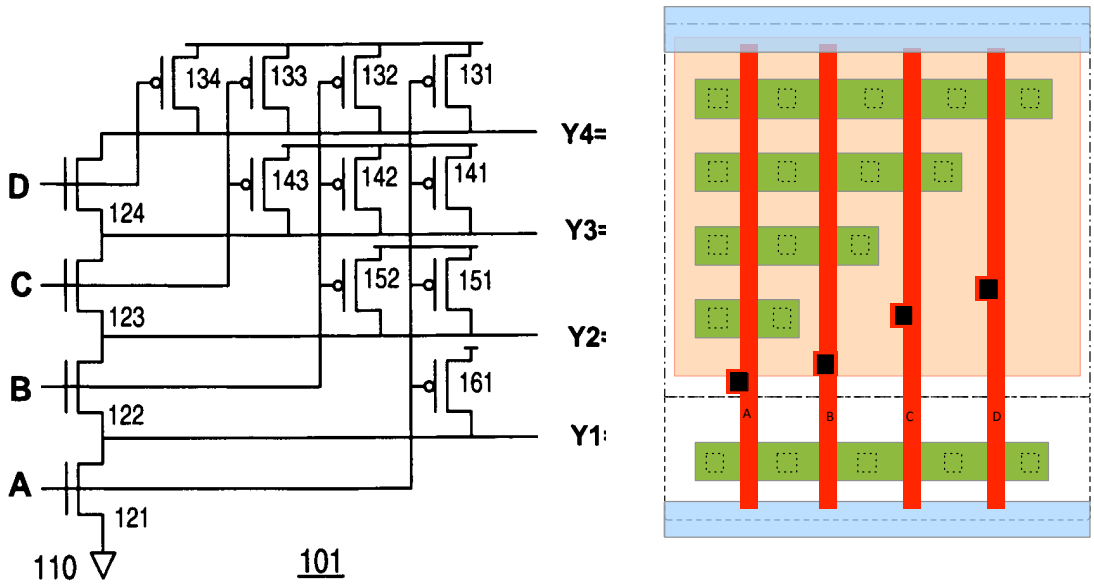

Figure 1 *a) A multiple-input, multiple output static CMOS gate with four logical functions. b). A layout template in which to lay out the gate. The template is repeated twice at the end of the exam for your convenience.*

[1] US patent 7570081.

2. **Voltage transfer curve, noise margin** Figure 2 shows the voltage transfer curves for **three** of the four logical gates in the schematic Figure 1 a) with all transistors having the same width as is shown in the layout template, and with all four inputs, A-D, connected together, so that there is now only one input. The VTCs have been simulated in a DC analysis in Cadence in the 65-nm process that you used in the labs.

   a) Which logical output of Y1-Y4 corresponds to each of the three VTCs named X (red), Y(green) and W(purple) in the graph in Figure 2? Motivate! (3 p)
   b) What is the definition of the noise margins and why is it important to have a large noise margins? (3 p)
   c) In Figure 2 is also a plot of the derivative of the VTC for the X output (the red dash-dotted line). From the data given in Figure 3 calculate the noise margin for the X output. The graph in Figure 3 is repeated in larger scale on the next page. (4 p)

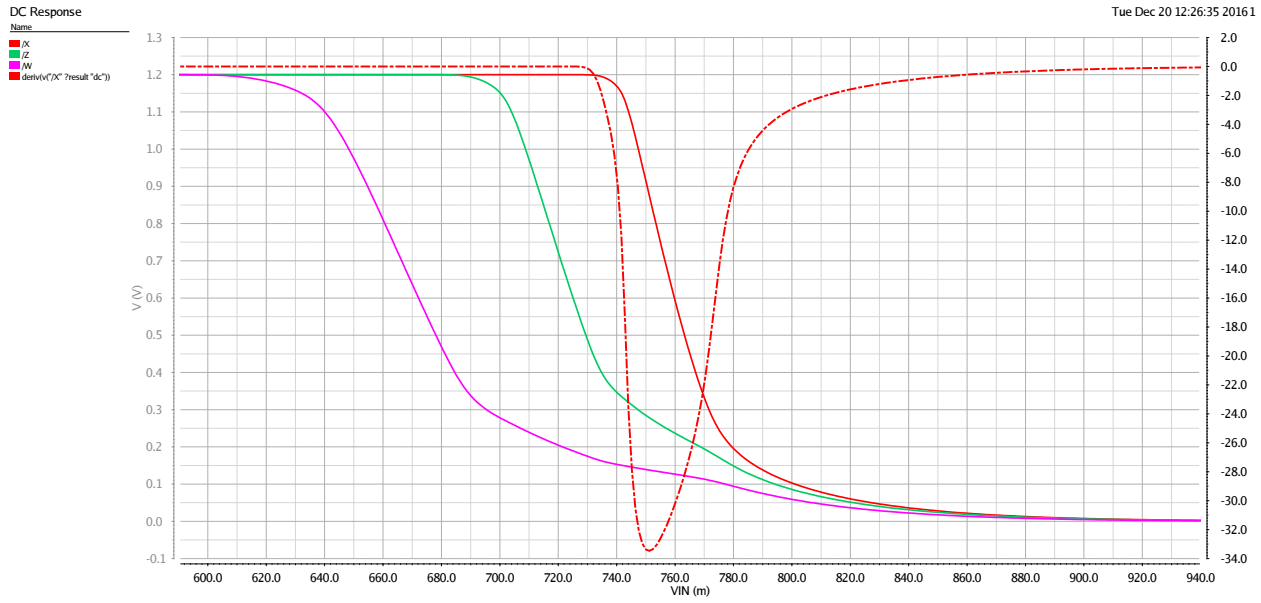

Figure 2: *Voltage transfer curves (VTC) for outputs X, Y and W and the derivate of the VTC for output X.*

DC Response

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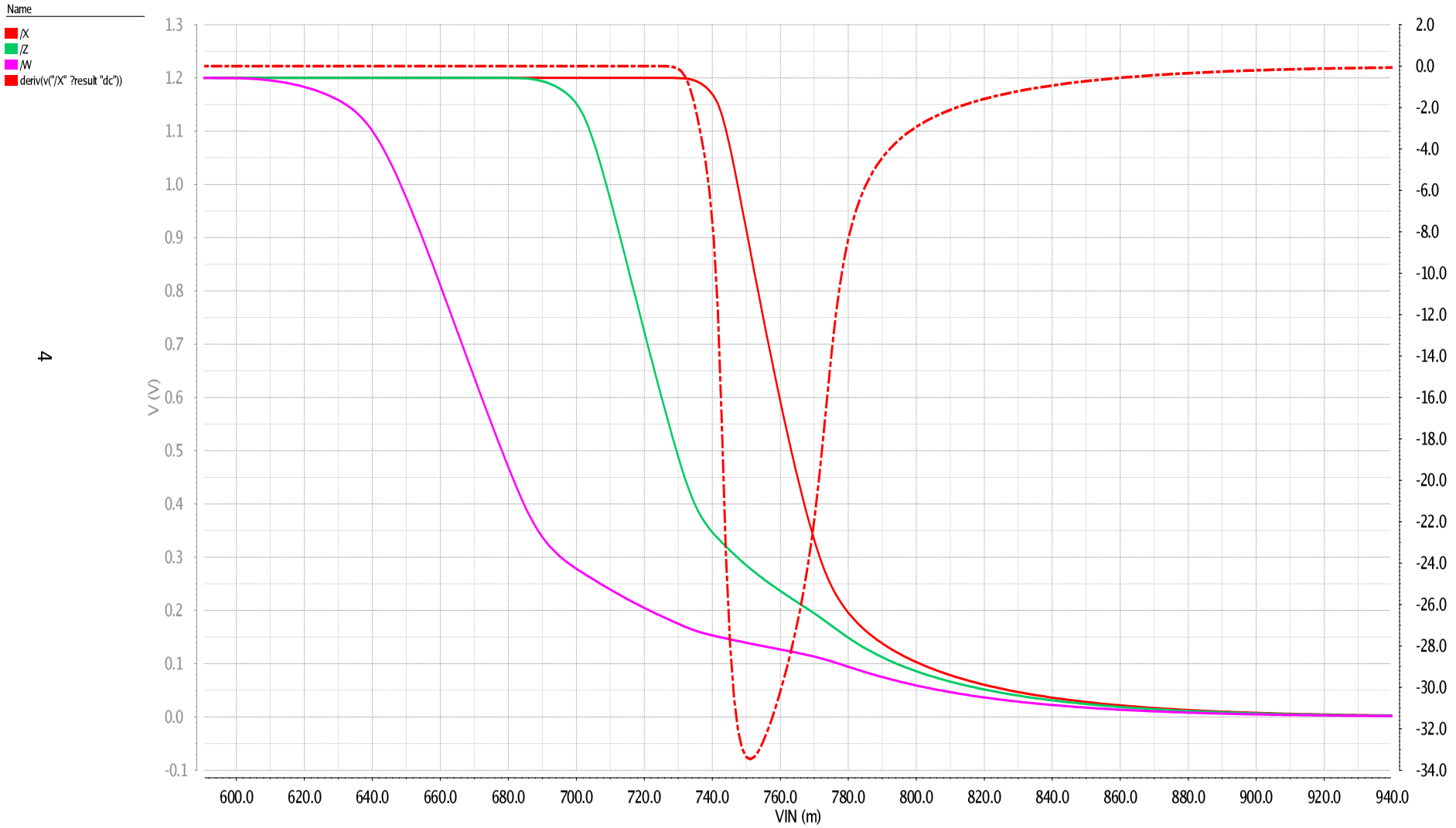

3. **Logical effort, path effort** In Figure 3 you see a block diagram schematic of a register file with 16 32-bit words and a 4-to-16 decoder that selects one of the 16 registers according to the address A[3:0]. In this problem your task is to size the decoder circuitry shown in detail in Figure 4.

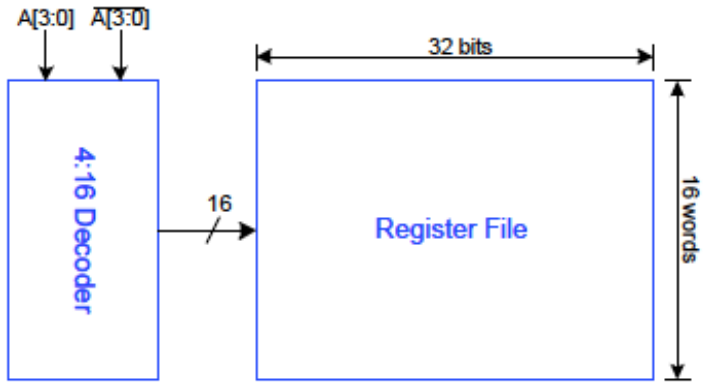

***Figure 3**: The register file with its 4-to-16 decoder.*

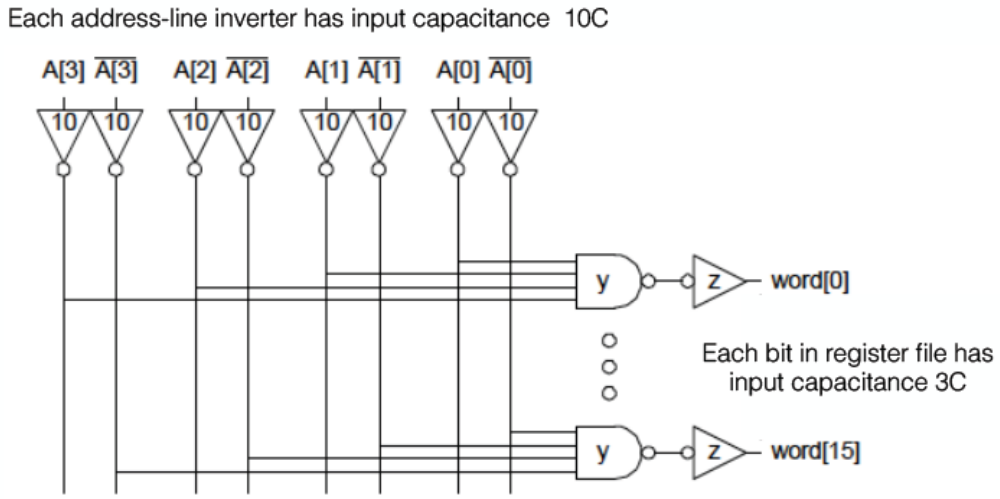

***Figure 4**: A detailed schematic of the decoder circuitry.*

a) How should the 4-input nand gate (y in Figure 4) and inverter (z in Figure 4) be sized for minimum delay with the assumptions given in Figure 4? Assume that an nMOS transistor has twice the current of a pMOS transistor of the same width. (5 p)

b) What is the resulting delay, including parasitic delays with the sizing from you result in task a)? Assume that the inverter output capacitance is the same as its input capacitance. (2 p)

c) What if we had a wider register file of 16 64-bit words? Would it be faster to use two inverters in the place of inverter z? (One would also have invert the address bits of course, but that could easily be achieved by swapping the lines for each address bit and its inverse). Motivate your reply! (3 p)

4. **Power, energy consumption** In this problem you will analyze the energy consumption for a video-rendering application run on a processor dedicated to this application. The processor can run at different supply voltages and has both a sleep mode and a hibernation mode. You final task is to determine of the hibernation mode is useful for this particular application.

Application: The digital video in the video-rendering application has 25 frames per second. One frame is 640x480 pixels. Each pixel is represented by 24 bits. The number of operations needed per pixel is 8 and these operations take 10 clock cycles to complete on the PP processor. The computations for one frame have to be completed in the time allotted for that frame.

PP processor: The PP processor used for this application has some characteristics shown in Table 1. You also know that it is fabricated in a CMOS process where the threshold voltages are 0.3 V. You may assume that the quadratic current equations hold in this process.

Table 1: Data for the PP processor

Supply voltage V_{DD} [V]	Maximum clock frequency [GHz]	**Current** due to dynamic power consumption @ max clock frequency and a realistic activity factor [mA]	Idle current @ room temperature @ max clock frequency and a low activity factor [mA]	Static current in **sleep mode** @ room temperature (clock signal turned off for logic, but clock generation maintained) [mA]	Static current in **hibernation mode** (clock generation stopped and internal supply voltages turned off) [μA]
1.2	1.0	600	100	60	60
1.0	?	?	80	37.5	60
0.8	?	?	64	28	60

Sleep mode: The time it takes to enter sleep mode is 10 μs and it takes 20 μs for the processor to wake up from sleep mode. The energy required to switch the clocks off is 10 μJ.

Hibernation mode: The time it takes to enter hibernation mode is 1 ms and it takes 19 ms to wake up from hibernation mode. The energy required to turn off V_{DD} is 500 μJ.

a) Fill in the four empty cells in Table 1 above with reasonable values. (4 p)

b) Considering only dynamic power, how much energy will be used for **one frame** of the video-rendering application in these two cases: 1.2 V and 0.8 V supply voltage? (2 p)

c) How much energy will be dissipated due to static power consumption for **one frame** for the two cases: 1.2 and 0.8 V supply voltage? Assume that the processor immediately enters sleep mode when no computations are required for the video-rendering application. (2 p)

d) What is your recommendation regarding the hibernation mode? Should it be used or not for the video-rendering application? Motivate your reply using data given in this problem and your results from tasks a)-c). (2 p)

5. **Wire delay** In Figure 5 you see a driver inverter loaded by four identical receiver inverters across an H-tree wire interconnect.

   a) Calculate the FO4 delay for the driver inverter when loaded as shown in Figure 5. (5 p)

   b) Determine the inverter resistance, R_{eff}, that minimizes the FO4 delay as calculated in a). You may assume that the inverter output capacitance, $C_{D,}$ is equal to the inverter input capacitance, C_G. (5 p)

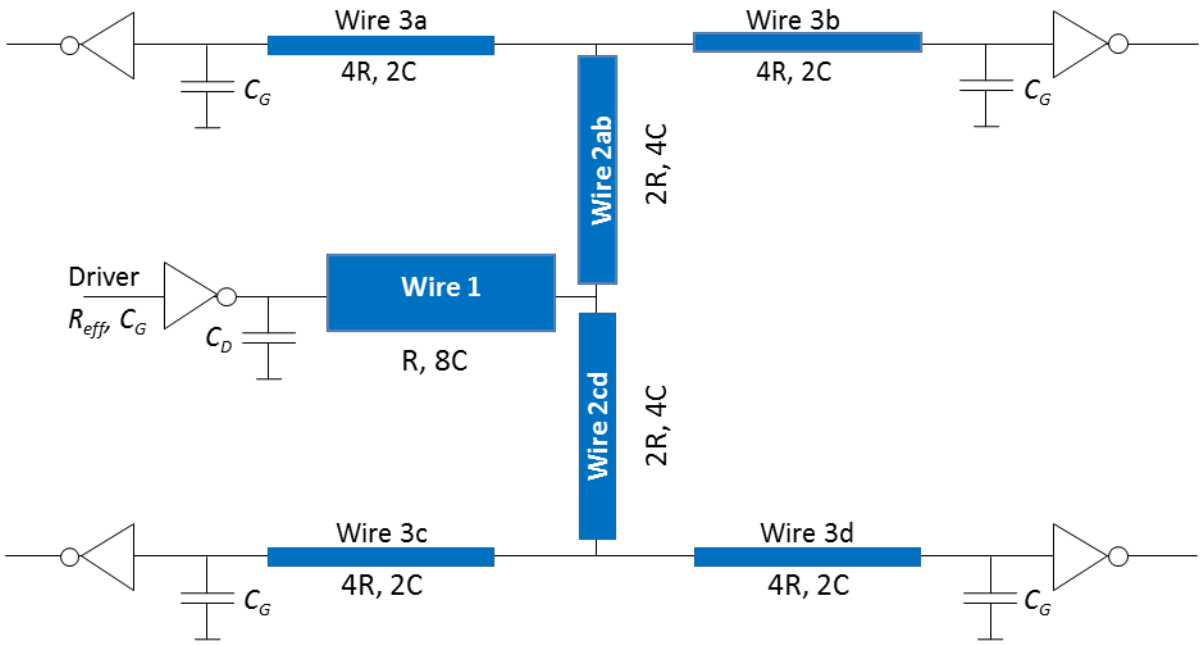

Figure 5. *A driver inverter loaded by four identical receiver inverters across an H-tree wire interconnect.*

6. **Prefix Adders** Figure 6 shows the beginning of the design of an unknown prefix adder. As you can see from the figure, in this type of adder no dot-operator cell in the forward or backwards tree drives more than two other dot-operator cells. (The triangles in the diagram are buffers that you can ignore in this problem.)

   a) Your task is to complete the adder design by adding the missing dot-operator cells, in the red box, so that all input carries needed for the SUM operations are available at the bottom. As an example, group carries C15:0, C11:0 and C7:0 (indicated with blue in Figure 6) are already available to form SUM16, SUM12 and SUM8, respectively. A fully correct solution should maintain the design principle that no cell in the tree drives more than two other dot-operator cells. Solutions that do not fulfill this principle, but are logically correct, will give partial credit. The figure is repeated twice at the end of the exam so that you tear off and turn in with you solutions. (7 p)

   b) What is the critical path of the prefix tree you have drawn in task a)? Indicate it clearly in the complete tree that you hand in. (3 p)

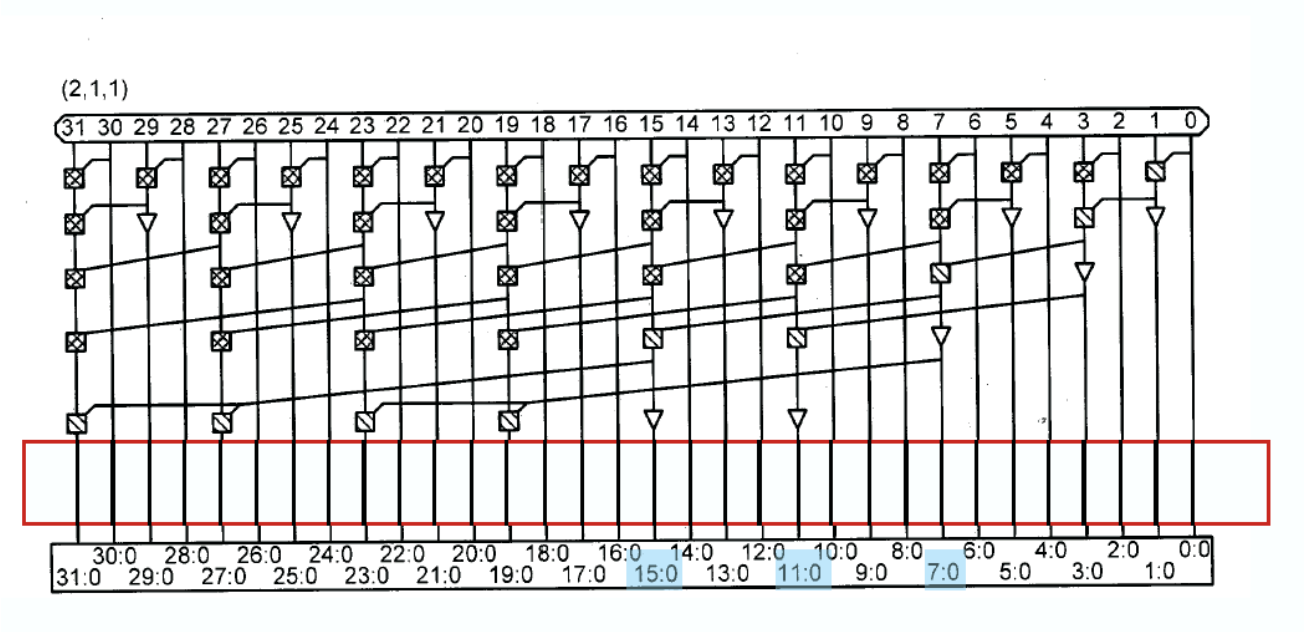

Figure 6. *An unknown prefix adder where the output of any dot-operator cell is connected to a maximum of two other dot-operator cell inputs.*

THE END!

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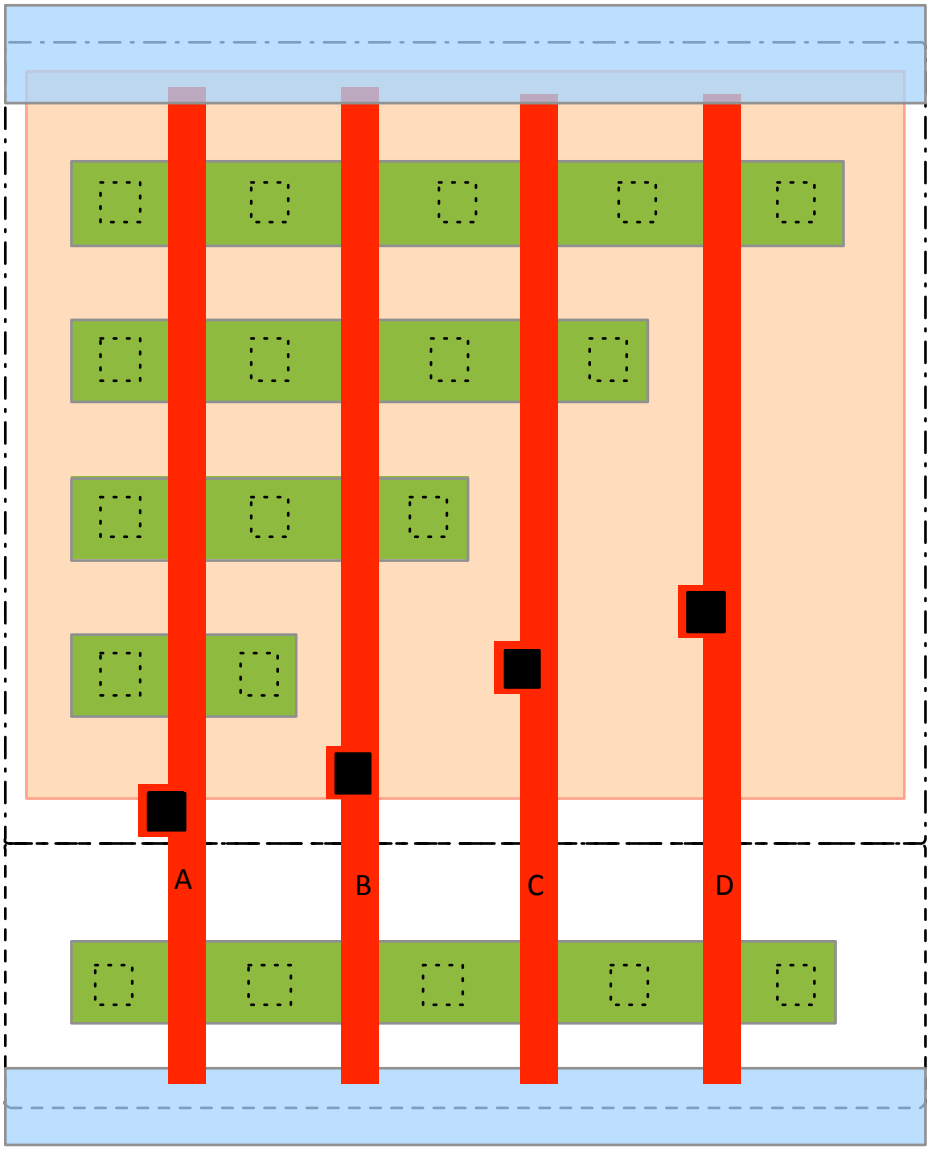
Label all output nodes clearly. The layout should correspond exactly to the schematic in Figure 1 a.



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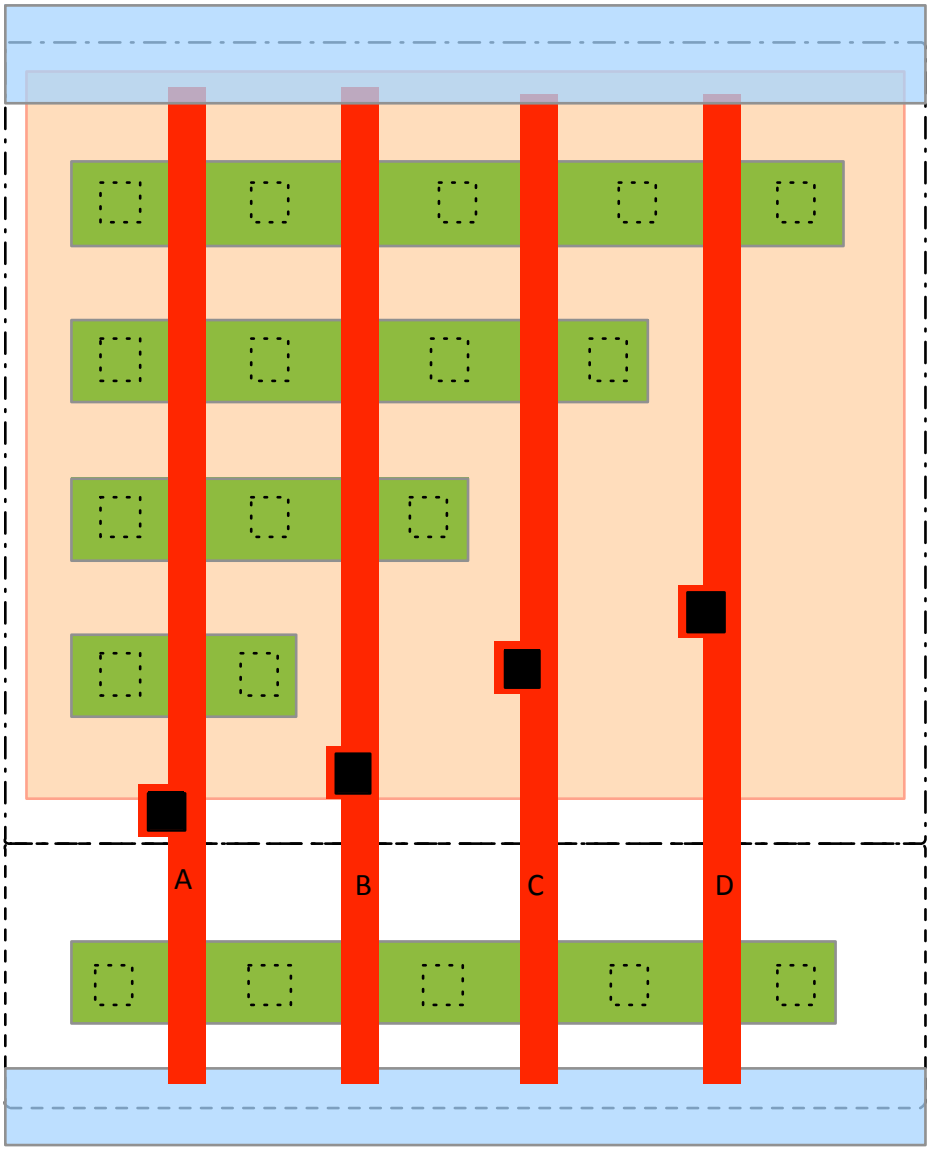

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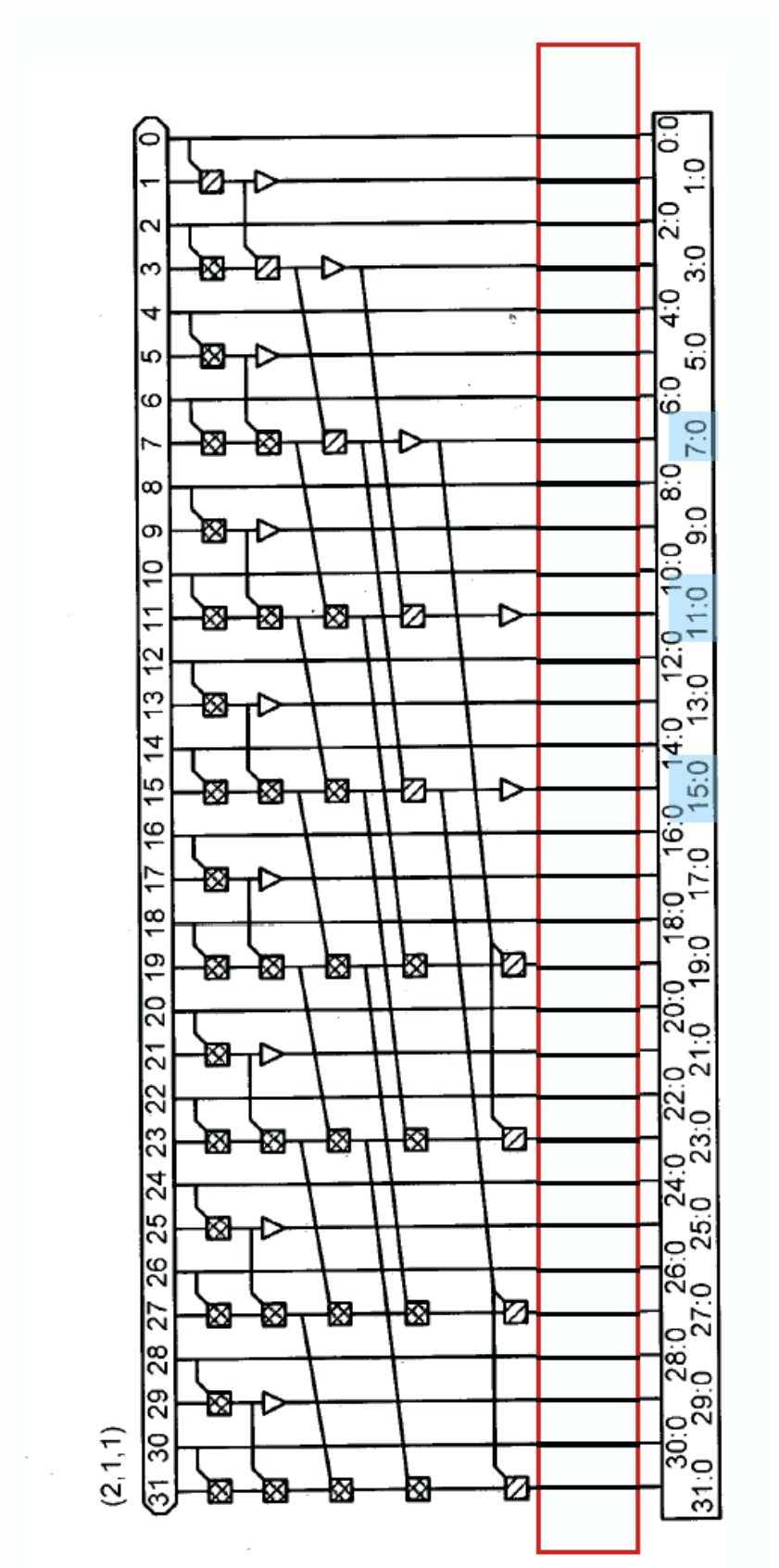

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