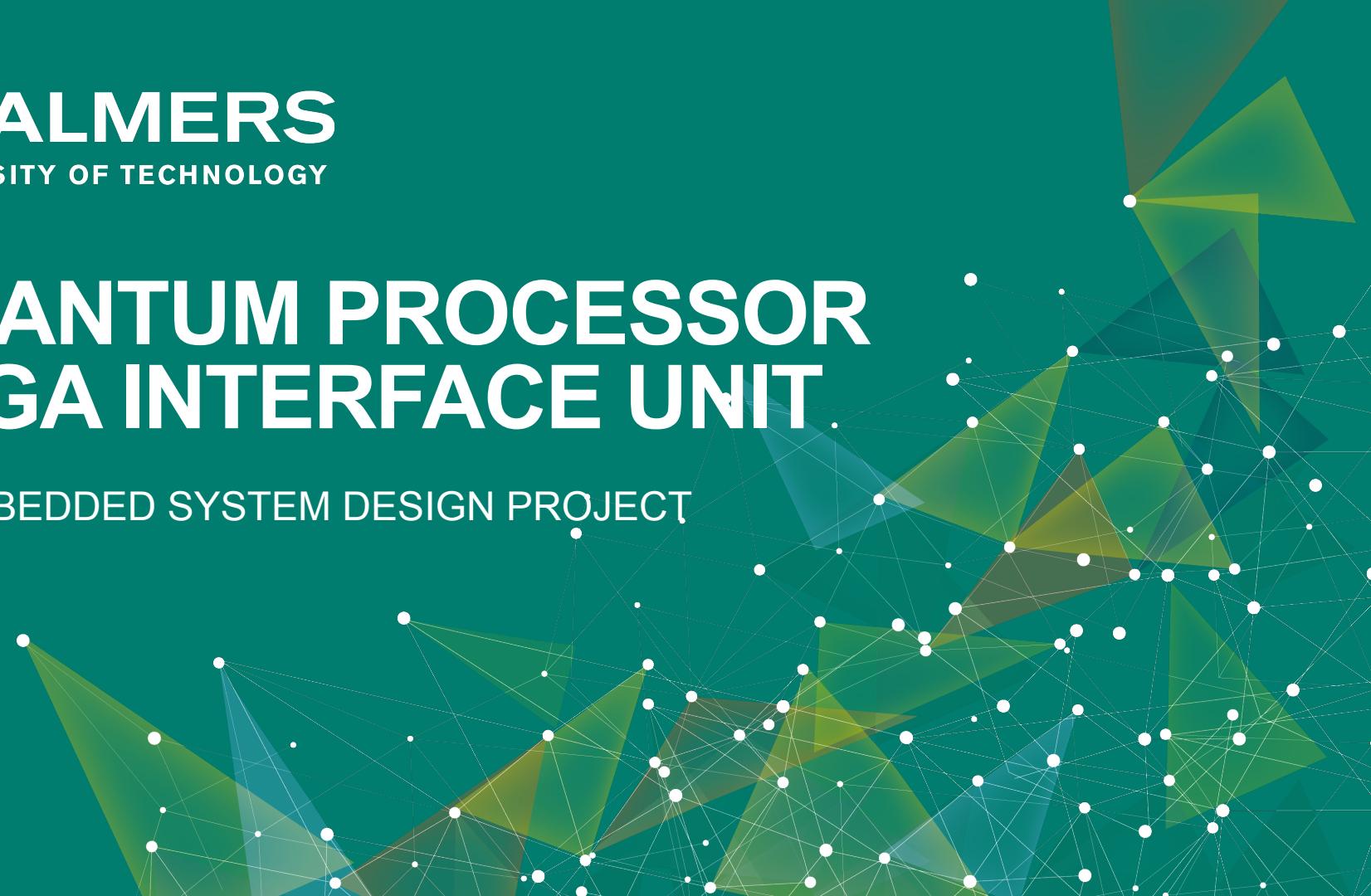


QUANTUM PROCESSOR FPGA INTERFACE UNIT

AN EMBEDDED SYSTEM DESIGN PROJECT

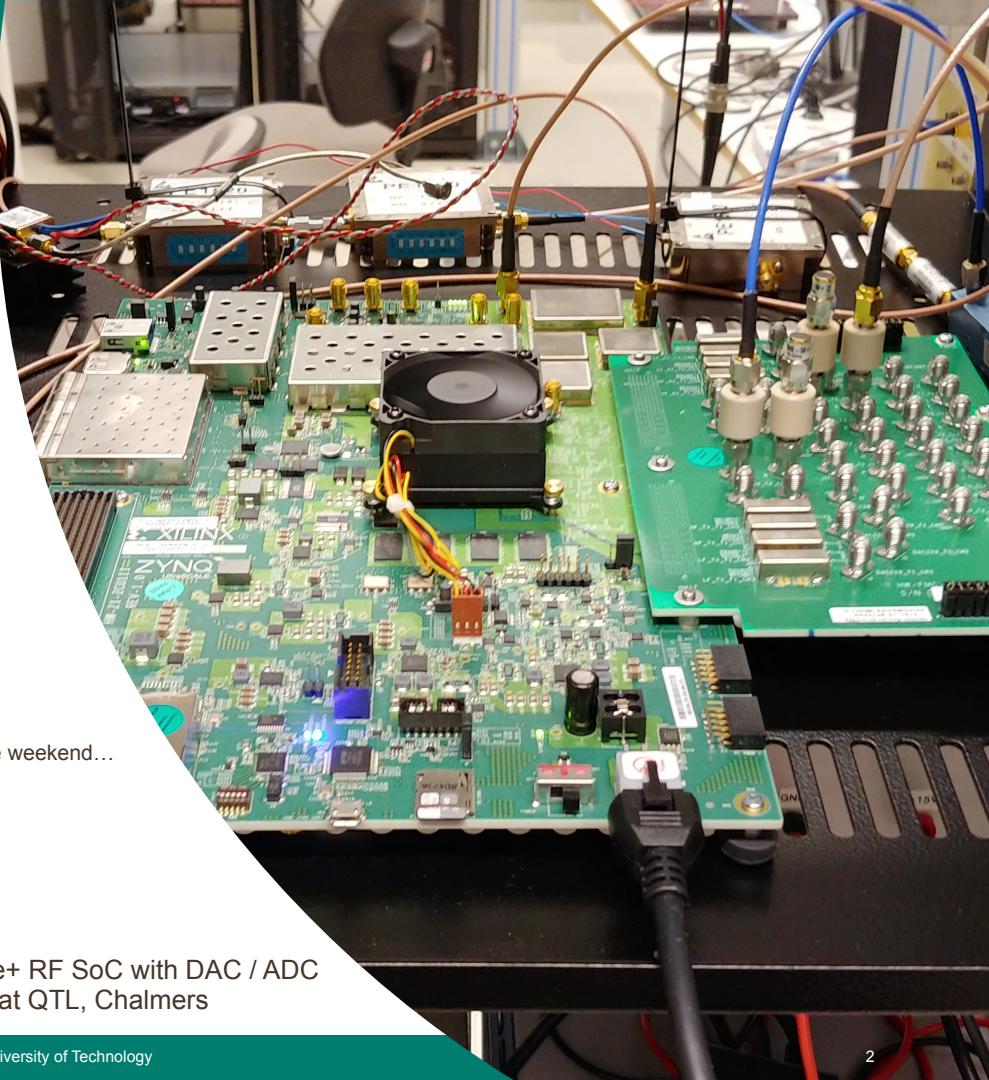


THE PROJECT

- An FPGA-based QPU interface unit for fast qubit control and readout.
- ... meant for operating one of the QPUs at MC2, Chalmers, by an operator who wishes to run large experiments.*

* fast enough to avoid having to dial the QPU control computer from home during the weekend...

Illustrated:
Xilinx Zync Ultrascale+ RF SoC with DAC / ADC
connected to a QPU at QTL, Chalmers





WHAT IS THIS THING?

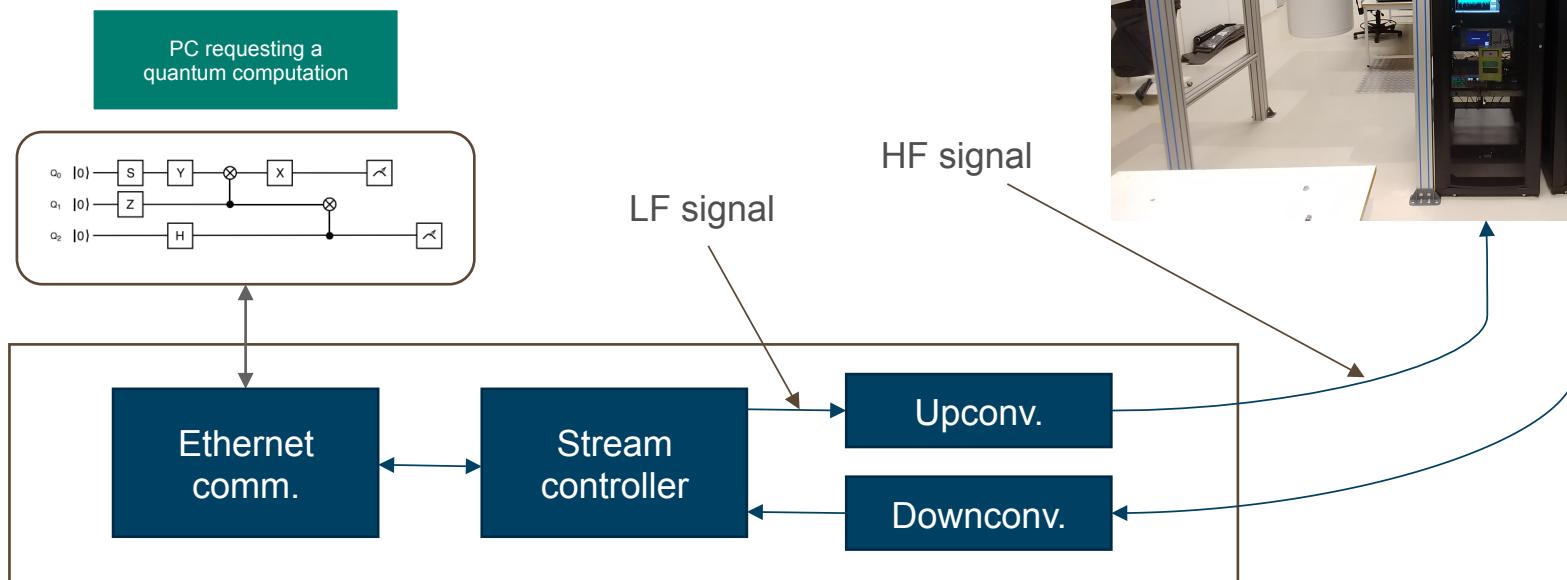
- Quantum processors are analogue devices. You feed them with a calculated RF signal, and get a modified RF signal back.
Typically 3-7 GHz.
- A vast array of properties in the received RF signal determines the outcome of the quantum experiment.
- Such an experiment is typically repeated thousands of times, yielding some averaged result. Because, once you read a *qubit*'s logical state, it becomes tainted by your readout signal ("observed").

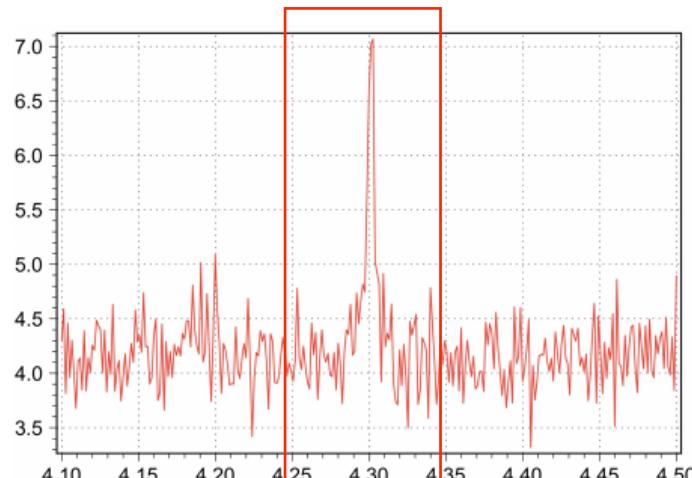


CONTINUED...

- A typical RF pulse is in the order of many μs long.
At 4 GSa/s, 16 bits resolution, >1 channel with 2 digital streams per signal ("I and Q"), merely a single *qubit* can generate a lot of data.
- This heavy parallel flow is almost unanimously dealt by interfacing to the QPU with FPGAs. Interfacing to the FPGA from a host, such as a PC, also puts high speed demands on the PC-FPGA interface.

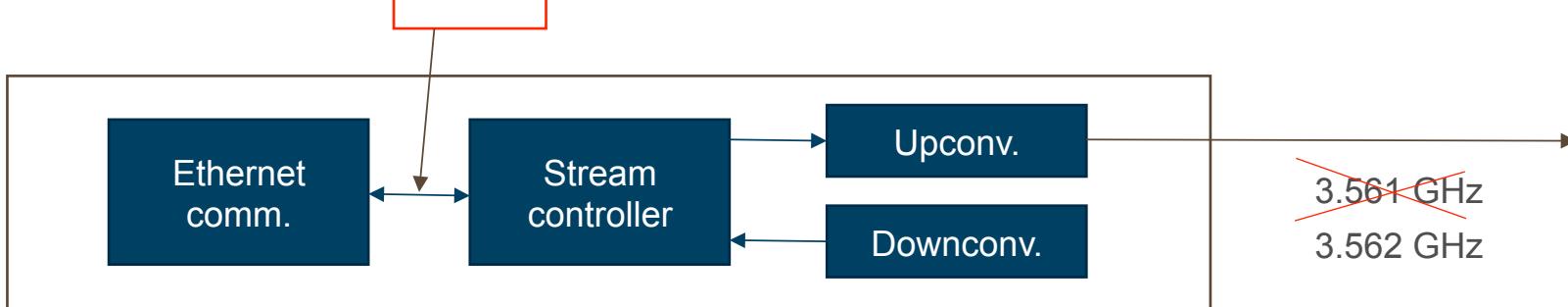
THE DEVICE'S FOUR MAJOR COMPONENTS

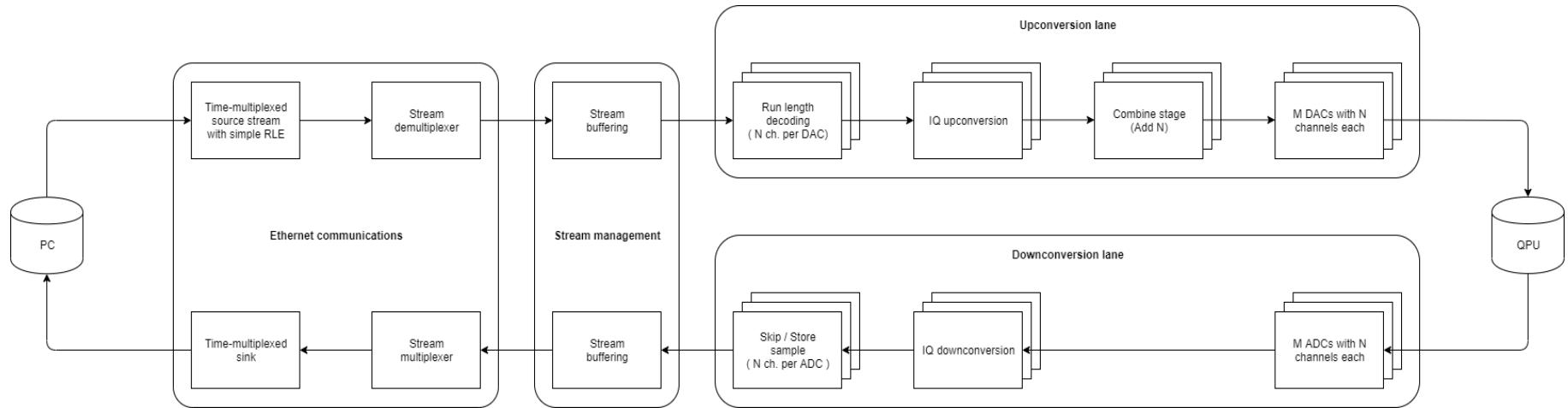




The data acquired will contain interfering data. Often, the operator may want to apply windowing.

Also, output frequencies may need in-situ adjustment. Thus the up- and downconversion should be adjustable on the fly if possible.





Block diagrams of all major components are available.
 Detailed descriptions of many parts of the system will be provided.
 For now, you are encouraged to look up **IQ mixing**, **AXI bus**, **ARP protocol**.



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