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FPGA-based QPU interface unit for fast qubit control and readout

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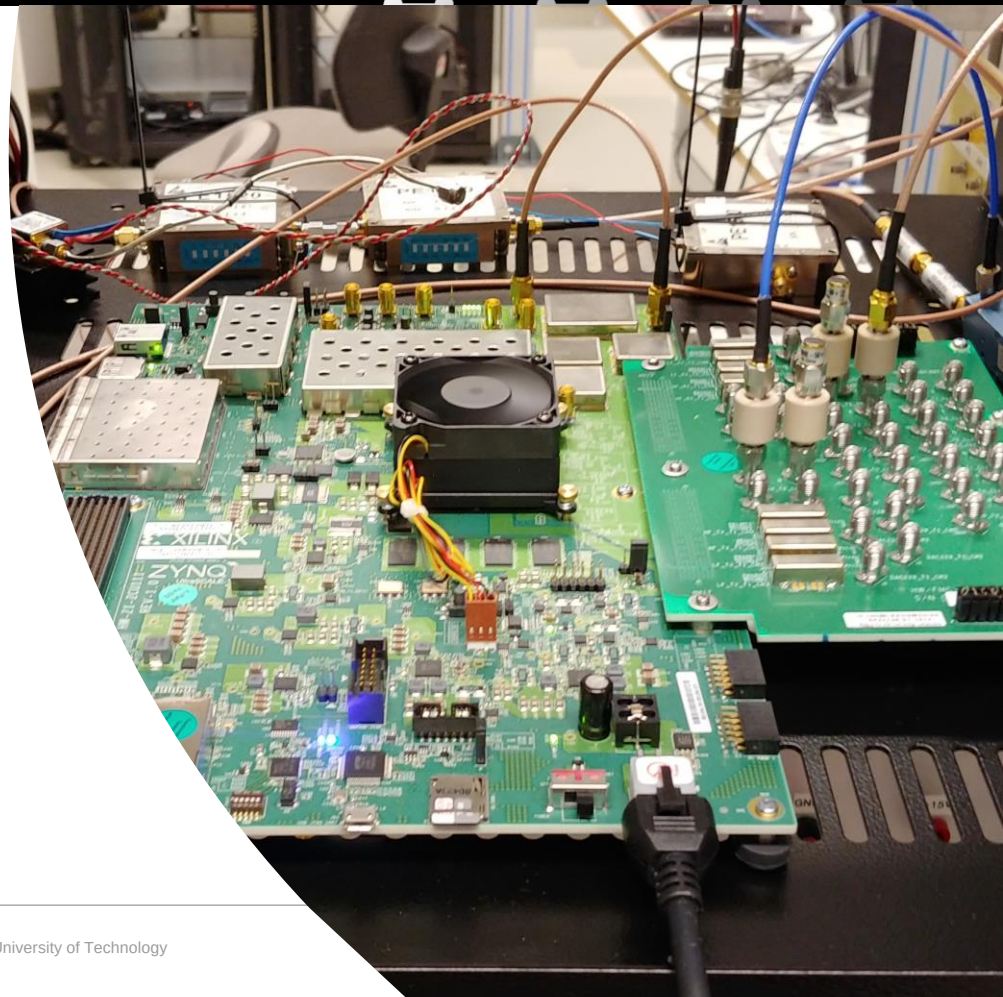
What is it for?

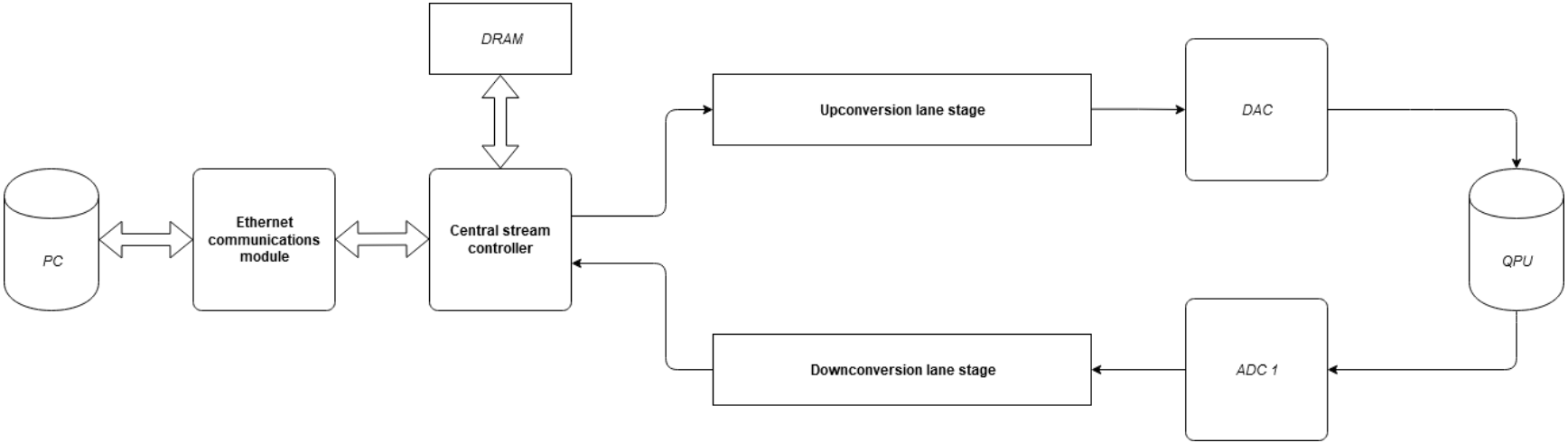
What is it for?

- Qubit control
- Qubit readout
- Signal processing (to some extent)

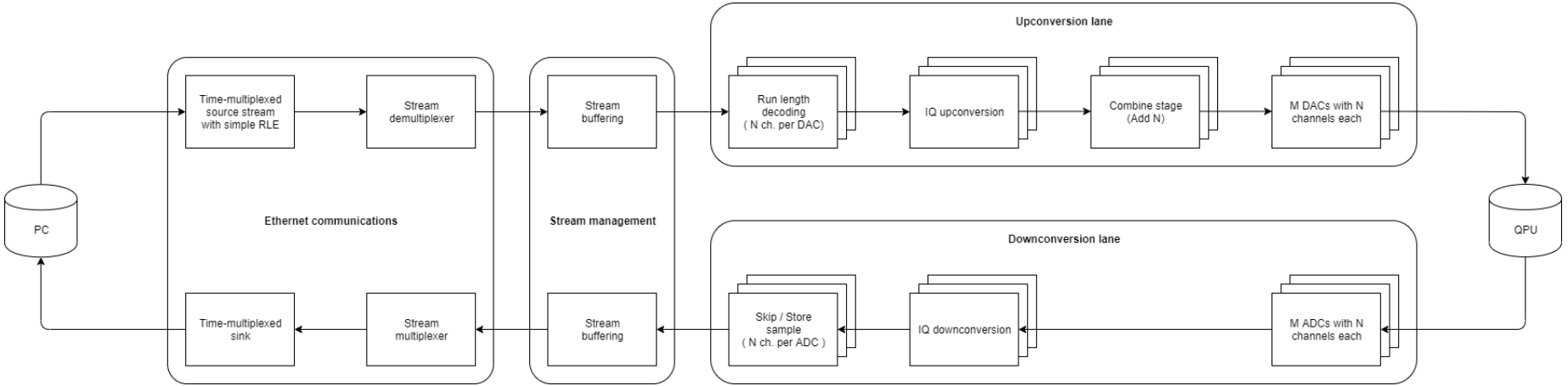


You'll run it on one of these

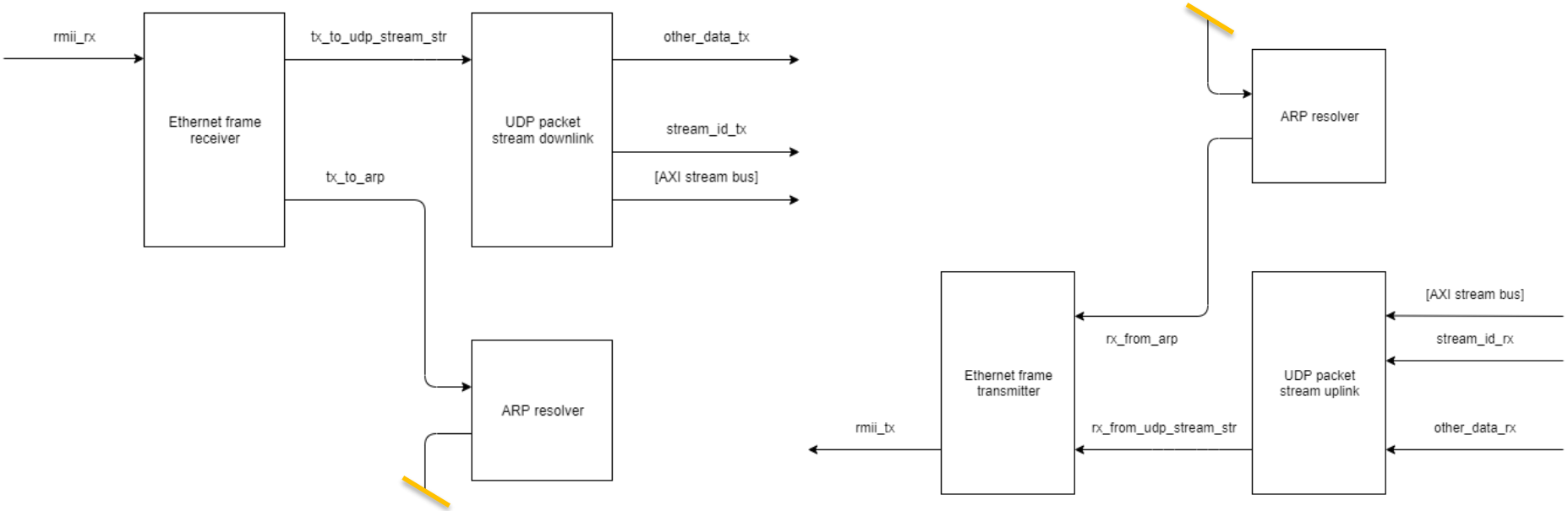
The very big picture



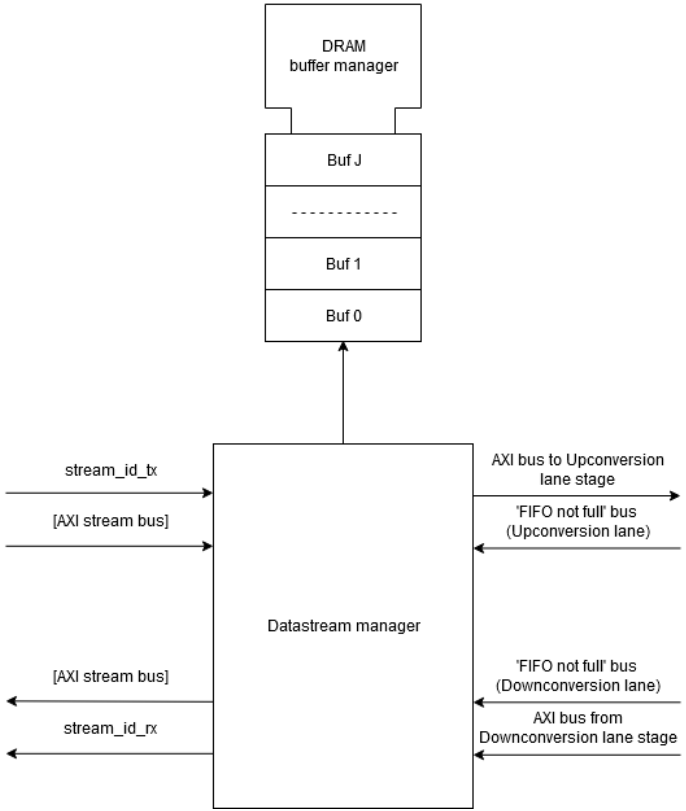
Dataflow diagram



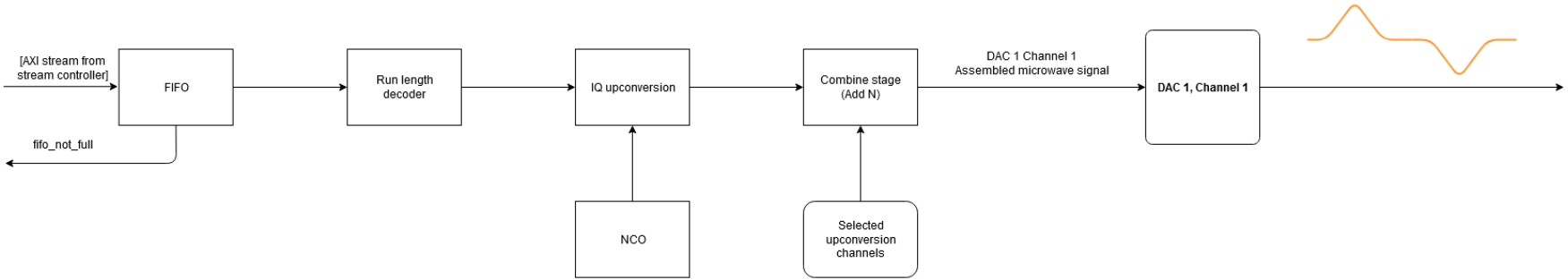
Ethernet communications module

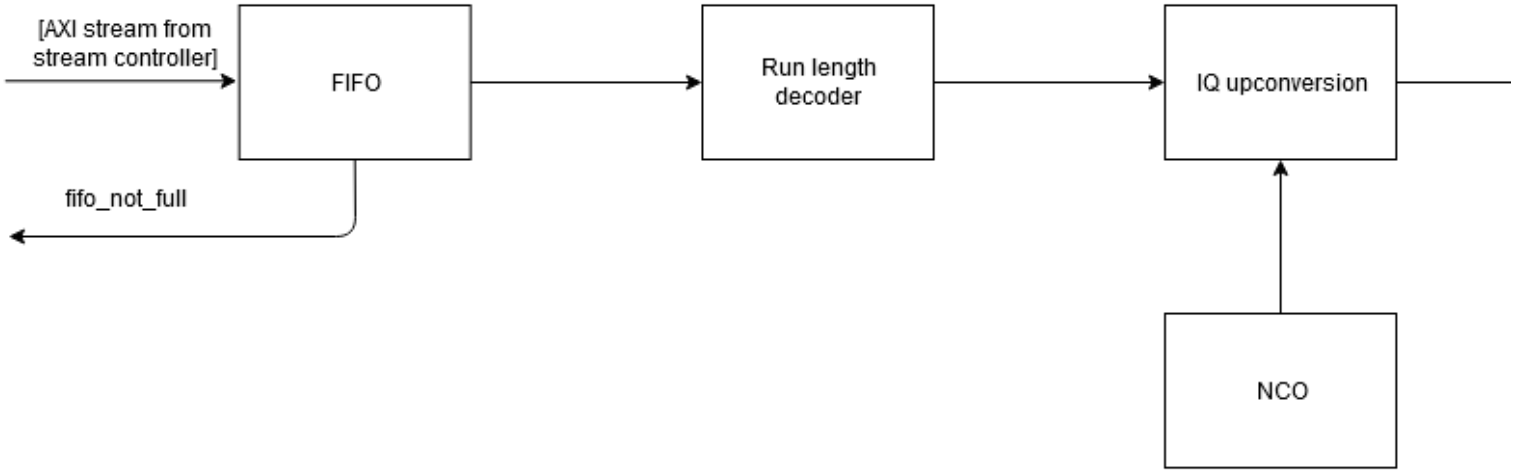


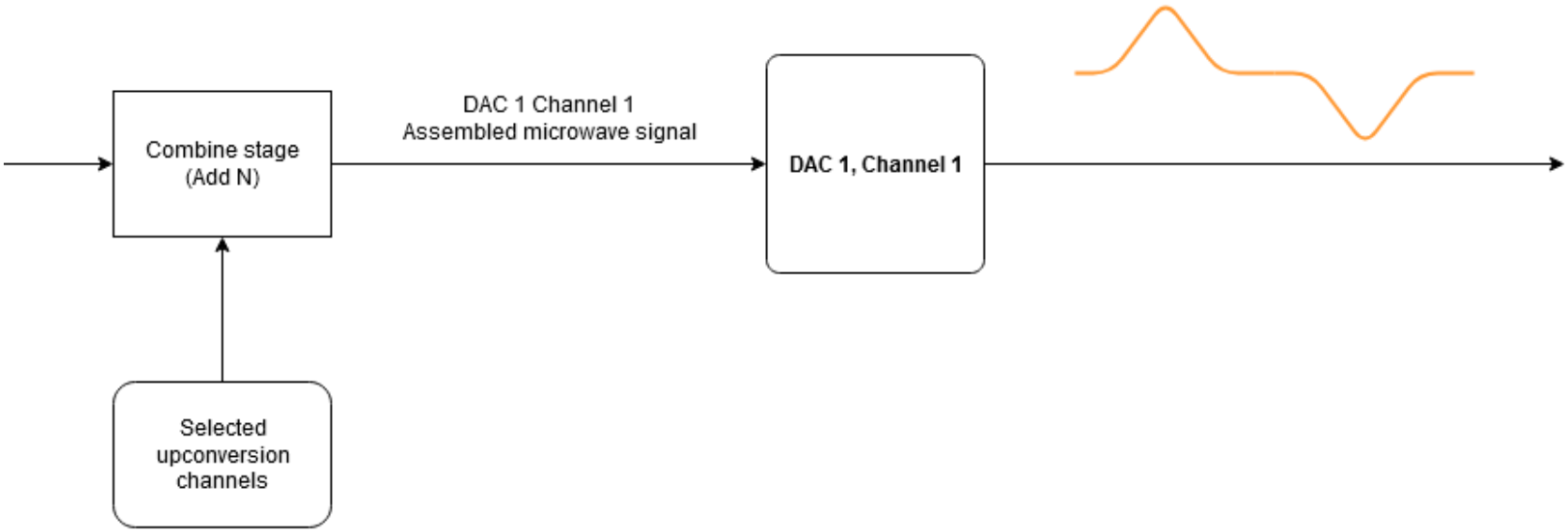
Central stream controller



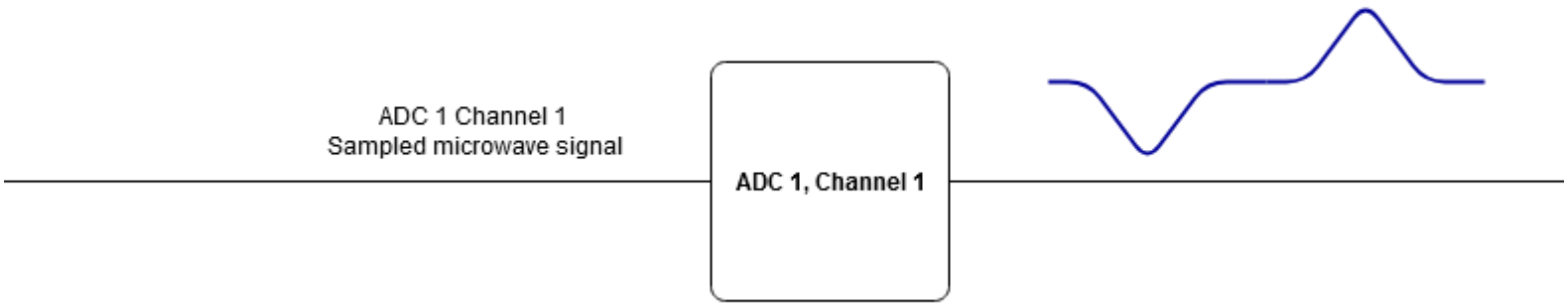
Upconversion lane

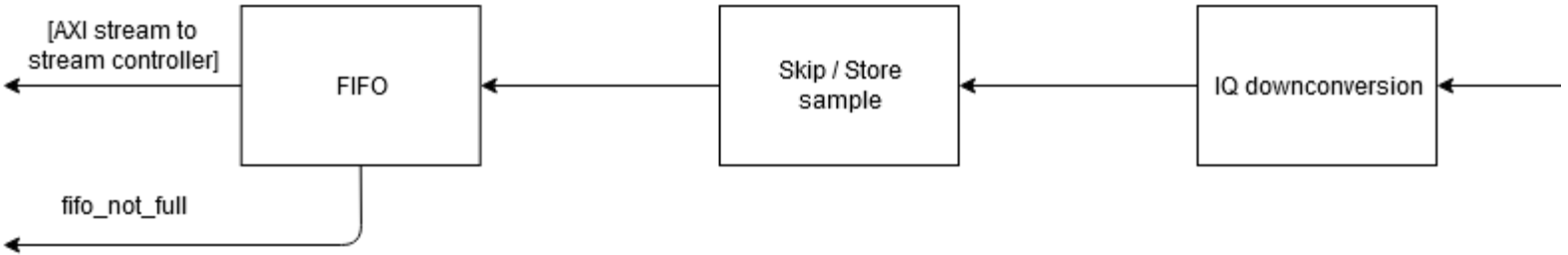



[AXI stream from stream controller]
FIFO
Run length decoder
IQ upconversion
fifo_not_full
NCO


Combine stage
(Add N)
DAC 1 Channel 1
Assembled microwave signal
DAC 1, Channel 1
Selected
upconversion
channels

Downconversion lane


ADC 1 Channel 1
Sampled microwave signal
ADC 1, Channel 1


[AXI stream to stream controller]
FIFO
Skip / Store sample
IQ downconversion
fifo_not_full

Important notes on frequency conversion

- The sinusoid generator sub-block can easily become your greatest adversary if not taken seriously.
- Troves of academic matter exist on how to produce the perfect sine wave.
- Same goes for IQ mixing, you should get to know the equations (not very hard).

Quick notes on testing

- Loopback is king
- Generating test waveforms can be done on the fly
- Even though ‘broken’ qubits can be faked using C-LC filters, your focus should lie on digital development techniques, actual DAC/ADC-work is best performed on the final FPGA platform.

Documentation to get you started

- Project introduction
- Module map
- Module map specification document
- Hints on testing
- Dataflow diagram
- … likely more content

People

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Intermodulation Products AB

Handles specification to product owner

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Product owner

DAT096
Project teams

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