Text examples DAT096 feedback

Sentences are selected DAT096 half-time reports from previous years. There may also be other problems in the text examples for a specific problem.

Examples of dangling modifiers

Example 1:

The amount of decrease in amplitude of the wave after cut-off frequency should be -40 dB per decade for a second order low pass filter [21]. The amount of decrease in amplitude for the 1316 Hz waveform from the one before cut-off is a decrease of about 50%. By using equation 6.10 it gives that 50% corresponds to -6 db of gain.

Example 2:

The initial design for the digital module can be seen in figure 3.1. The "blackbox" FPGA takes the three **I2S** signals as input and outputs two signals, forming a pulse-train, to the analog module. Diving into the black-box, the digital module consists of 4 main sub-modules: the **I2S** decoder, the delta-sigma modulator, some logic which controls the pulse-train outputs and a test module for generating test-inputs to the converter.

Example 3:

The CORDIC (COordinate Rotation Digital Computer)[2] was developed by Jack Volder in 1959 for trigonometric functions i.e. sine and cosine, and has since then been used for example in the 8087 math coprocessor, HP-35 calculator, radar signal processors and robotics. Its advantage when implemented in hardware is that as an iterative algorithm it is only using shift, add and subtract operations to convert between polar and Cartesian coordinates. By using the method or mode of circular rotation the Cartesian coordinates of the vector V_n can be found by rotating an input vector V_0 by an angle $\Theta = Z_0$.

Example 4:

The pulse encoder works in the way that it has two signals that specifies what the current state of the encoder is by sending out gray code. When rotated, the state changes and the output from the encoder will also change. By looking at the gray code, which way the pulse encoder rotates are derivable and then the parameter can be changed accordingly. How the rotary pulse encoder moves between its different states can be seen in figure 5.

Example 5:

This depends on that the sine wave only contains one frequency and the square wave contains some harmonics with higher frequencies, this are described in length in section 2.2.
When changing the frequency offset between the two oscillators a higher pitch could be heard.

When the offset are zero the two waves are in sync with the same frequency. When adding a non-zero value on the offset the two waves will no longer be in sync and the frequency of the

sum of the waves will change leading to a different pitch in the tone.

Until now, we have fixed the size of the signal carrying bus to 12 bits. We need the output to be 12 bits but the components driving the signal midway could exploit the length of the bus. For example, if needed, we can increase the size of the LUT or use other algorithms to implement the sine function to increase the precision of the signal and the calculations. This is useful since better approximation will lead to a clearer tone.

Our implementation is now somewhat done in the sound generating part and is generating a decent output but there is still some things to implement and improve in our design as discussed.

Example 6:

Design decisions for developing embedded systems differ depending on application, resources and constraints. The same system could be done either through software, hardware, softcore or a balance between these. Design decisions affects area, speed, latency, performance, cost and reliability. By exploring resources, requirements and tradeoffs between these approaches justified design decisions can be made. After identifying the exact balance in trade-offs, the tool support needs to be identified.

Example 7:

To determine the different values for the filter we performed several calculations, which can be viewed in Appendix A. In our case, using a cutoff frequency of 20 kHz, the values of the capacitor would then be 0.7 µF and the inductor would have a value of 45 µH for a load of 4 Ω. For a load of 32 Ω we need a inductor with 360 µH and a capacitor with 87.92 nF. As these values are not available at vendors we had to compromise with the closest values which were available. The different values for our components can be viewed in Table 5. After reading a paper from Texas Instrument[12] two extra capacitors will be added to the schematic to provide high-frequency decoupling.

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Examples of plural / singular problems

Example 1:

The sine wave generator takes in required frequency and asks the values from the LUT. Input data to the LUT, (Θ), represents the angle and the output represents the amplitude of the sample. The value stored for each input angle in the table is pre-calculated and stored. At every sample clock one output is generated from the oscillator. Since sample clock is fixed at 40 kHz the step size is calculated according to the frequency. The step size indicates how many periods of the sample clock the sine waves period should be reduced with.

Example 2:

4.1 Oscillator

The two oscillators in the synthesizer generates a periodic signal with a frequency between 131 Hz and 4699 kHz. The specifications, section 3, says that the frequency range should be from 200 Hz to 3.2 kHz but also that one of the oscillators should have an offset of -8 to 7 halftones which results in the frequency range mentioned above. As the two oscillators in the implementation are the same both oscillators are able to have this offset but it is only used for one of them. As seen in Fig. 11, the offset module has, as input, which key on the keyboard that is pressed and the frequencies for both oscillators as output.

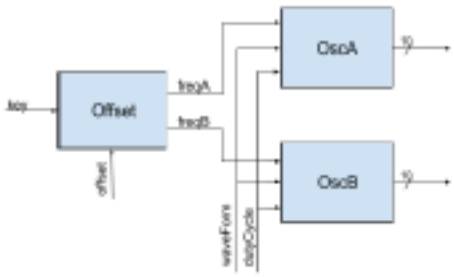

Figure 11. The two oscillators connected to the offset module.

Example 3:

4.7 I2S

The clock, data and channel selection are serially transmitted to the analog part. 12 bits are received as input signal to I2S at 40 kHz and need to transmit it with 13 other null bits to make it 25 as specified in the specifications section 3. Although the requirement is 24 but we transmit 25 since it is closest to requirement which can exactly divide system clock to create even clock. The 25 bits should be transmitted during one sample period so that no samples are missed. It is possible to make total number of bit variable but for our design the number of bits are fixed to 25. As specified in acceptable standards [25], the MSB are sent first trailing with null bits. This is because it is easy to adjust and retrieve variable sized data packet at the receiver end. The transmission also carries a word select (WS) signal which is high-low alternatively for each 25 bits. It indicates left or right channel of a stereo signal. Odd samples are sent when the WS signal is high and even samples are sent when the WS signal is low.

Example 4:

A synthesizer is an electronic musical instrument. In recent years many different types of synthesizers have been developed by engineers. Analog Synthesizers using vacuum tubes were introduced in early 1920's [2]. By 1960's vacuum tubes were replaced by operational amplifiers. The introduction of digital synthesizer was in 1980's, and they largely replaced analog synthesizers. A digital synthesizer is a combination of a synthesizer engine and a class-D amplifier.

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Examples of equations not being part of the text

Example 1:

The amount of decrease in amplitude of the wave after cut-off frequency should be -40 dB per decade for a second order low pass filter [21]. The amount of decrease in amplitude for the 1316 Hz waveform from the one before cut-off is a decrease of about 50%. By using equation 6.10 it gives that 50% corresponds to -6 db of gain.

$$Gain\ in\ db = 20\log\left(\frac{V_{out}}{V_{in}}\right) \tag{6.10}$$

The step size for -6 db is 1.41 which is an increase of 41% in frequency when using equation 6.11 [22].

$$step\ size = 10^{\frac{-6}{-40}} \tag{6.11}$$

The frequency change from cutoff to 1316 is a percentile change of 32.6% which is a bit less than it should be. This could be because if looking at Figure 6.4 it can be seen that at 1004 Hz it already decreased more than it should making the cut-off be a little bit before where it should be. Why this happens can be because of numbers being rounded down when taken from doubles to integers which can influent a lot when some coefficients are quite small.

Example 2:

The coefficients are represented as b_n or a_n whereas z^{-1} describes a delay. The equation for this 2nd order implementation in the time domain is shown in the equation below.

$$y(n) = b_0 \cdot x(n) + b_1 \cdot x(n-1) + b_2 \cdot x(n-2) - a_1 \cdot y(n-1) - a_2 \cdot y(n-2)$$

A simple z-transform of this equation can give us the frequency response of such an equation and show how the coefficients affect the frequency domain of the filter implementation. The z-transform gives the below equation.

$$Y(z) = b_0 \cdot X(z) + b_1 \cdot X(z) \cdot z^{-1} + b_2 \cdot X(z) \cdot z^{-2} - a_1 \cdot Y(z) \cdot z^{-1} - a_2 \cdot Y(z) \cdot z^{-2}$$

Knowing that the impulse response is defined as $H(z) = \frac{Y(z)}{X(z)}$ yields the below result as the frequency domain equation represented with the coefficients that we wish to manipulate in order to change the behavior of the filter. The impulse response equation is shown below.

$$H(z) = \frac{b_0 + b_1 \cdot z^{-1} + b_2 \cdot z^{-2}}{a_1 \cdot z^{-1} + a_2 \cdot z^{-2}}$$

Example 3:

2.3 Determining the OSR for the (DIF)

For getting to know what will be the Oversampling Ratio the methodology used is shown in the steps below:

1. The Delta-Sigma toolbox, created by Richard Schreier was used in order to determine Noise Transfer functions, how the Delta-Sigma modulator will generate the pulses, how would they look and whichSNR they will have according to the OSR.

2. We propose the range of the Oversample Ratio where the SNR will be evaluatied. OSR = {4, 8, 16, 64, 128, 200}

3. Obtain the Noise-Transfer function (NTF), we propose to have a 2nd Order Loop since it is necessary to have the same order of loops as the order of the passive filter in the output, according to Kulka and Schreier they have mentioned that if a higher order in the DSM it will be hard to couple the output signal to the filter.
   $NTF = \frac{z^2-2z+1}{z^2+1.225z+0.4415}$

4. We review how the PWM will look after being generated based on the OSRs. ADD Picture 2, 32 and 128 Oversample

5. FFT of the signals generated was obtained, so the SNR can be calculated.

6. We realize a comparison on SNRs obtained at different ranges of the signal.